Calibration Techniques for Millimetre-wave On-wafer S-parameter Measurements

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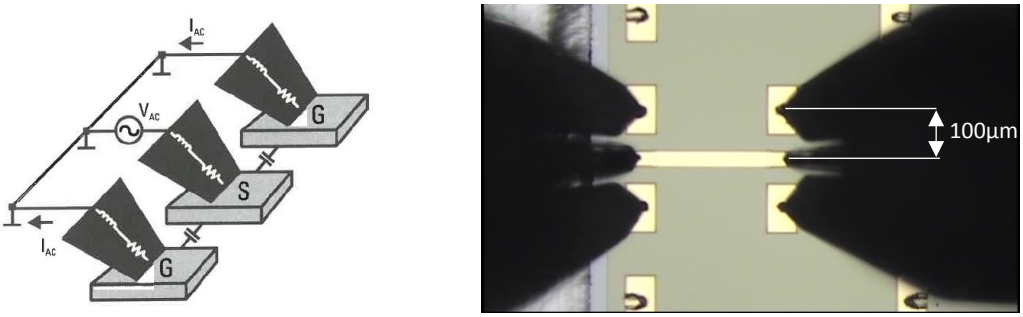
I. Summary

Accurate characterisation of *S*-parameters (scattering parameters) at chip level is of great importance to the development of next generation electronic devices. Such measurements are usually carried out on a Vector Network Analyzer (VNA), subject to an on-wafer calibration. Calibration techniques play a key role in determining the accuracy of on-wafer measurements. This paper is intended to provide an overview of conventional calibration techniques, including TRL (Thru, Reflect, Line), Multi-Line TRL, SOLT (Short, Open, Load, Thru), LRM (Line, Reflect, Match), and LRRM (Line, Reflect, Reflect, Match). Advantages and limitations of these different calibration techniques are discussed briefly and summarised. This paper also gives an insight into important factors that influence on-wafer measurement quality. These factors include design of calibration standards, testing environment (boundary and nearby structures), probes pitch sizes, etc.

II. Conventional Calibration Techniques for Planar Measurements

Most RF and microwave probes are designed to have probe tips suitable for probing on coplanar waveguide (CPW) structures. Fig. 1 shows the typical CPW ground-signal-ground (GSG) probe tip configuration. Calibrations using reference devices in the on-wafer domain are usually performed prior to further on-wafer measurements so as to remove the systematic and drift errors from measurement results. Basic calibration standards include OPEN, SHORT, LOAD, and THRU, as shown in Fig. 2, with each having electrical characteristics that are very different from each other, which is preferable for the calibration. These standards are however not ideal, due to parasitic capacitance or inductance, see Fig. 2. Such parasitic capacitance and inductance associated with standards need to be taken into account when performing an on-wafer calibration to the probe tips. Probe manufacturers usually specify calibration coefficients obtained using a commercial Impedance Standard Substrate (ISS).



(a) (b)

Fig. 1. (a) Illustration showing signal excitation at coplanar GSG probe tips [1]. (b) Photograph of the GSG probes tips of the D-band (110-170 GHz) probes at NPL. These probes have a pitch size of 100 µm.

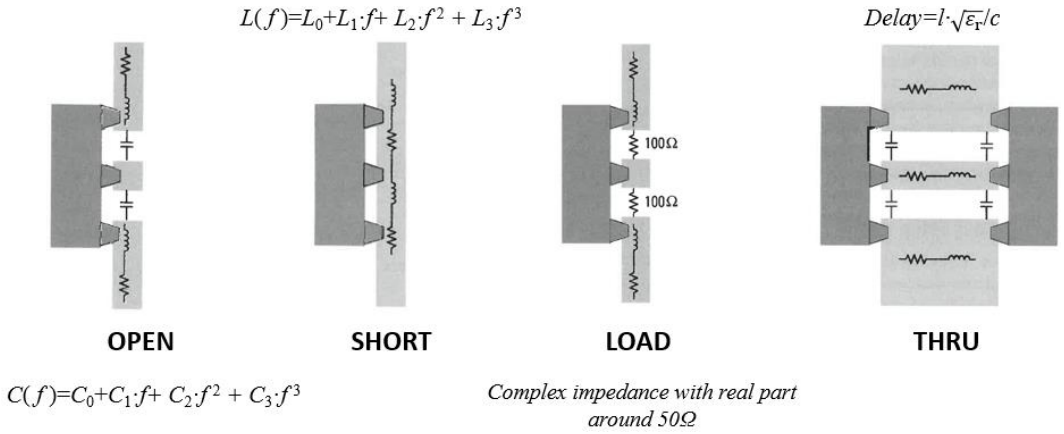


Fig. 2. Typical calibration standards with parasitic capacitance and inductance. [1]

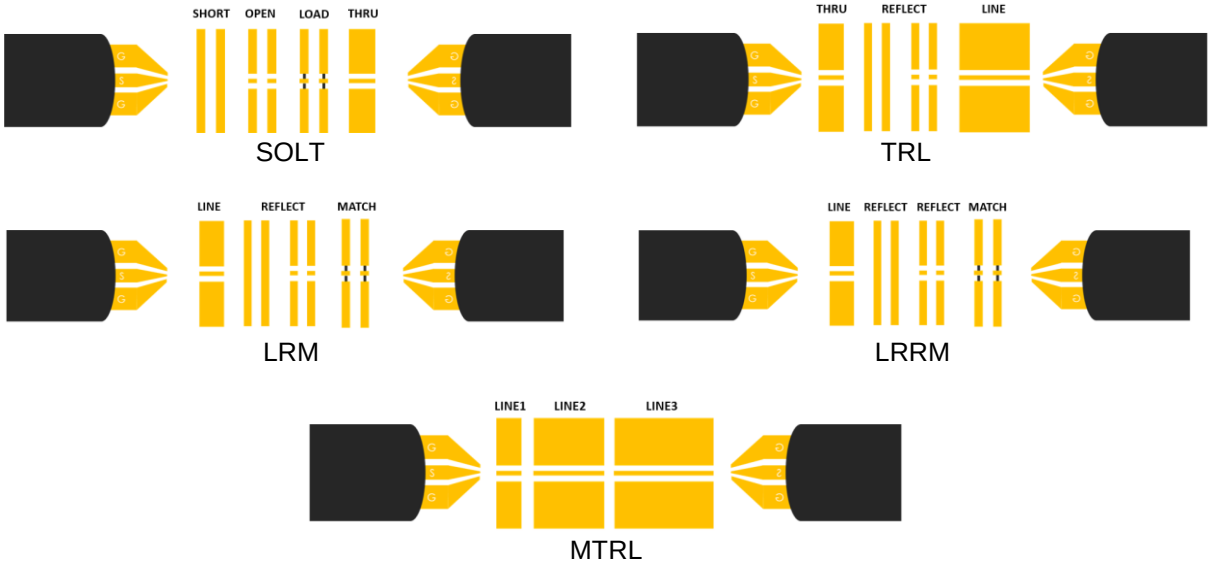


Fig. 3. Diagrams of five conventional on-wafer calibration techniques.

Fig. 3 illustrates five conventional on-wafer calibration techniques using these basic standards. These are briefly described below [1].

- SOLT requires rigorous definitions of calibration standards. SOLT is robust, as long as all calibration standards are perfectly known. Calibration coefficients for standards are defined for a particular probe placement, therefore the resulting SOLT calibration is relatively sensitive to probe placement errors that are inherent in microwave probing.

- TRL requires minimal knowledge of electrical behaviour of standards. The reference plane is usually set at the centre of the THRU standard. REFLECT standard can be either SHORT or OPEN, but identical reflects are required on both ports. LINE standard (with electrical phase around 20° ~ 160° at test frequencies) provides information about the characteristic impedance of the CPW transmission line. Each LINE standard can only cover a limited frequency range, hence multiple lines are required for broadband measurements.

- Similar to TRL, characteristic impedance of LRM is determined by the MATCH standard (equivalent to an infinitely long reflectionless line). The reference plane is set at the middle of the LINE standard. REFLECT standard can be either SHORT or OPEN, however it should again be

identical on both ports. LRM does not need knowledge about parasitic capacitance of OPEN or parasitic inductance of SHORT. However, the behaviour of the MATCH needs to be well understood.

- Reference plane of LRRM is usually set at the middle of LINE. REFLECT does not require known OPEN or SHORT, however it must be equal at both ports. MATCH standard could have known resistance and unknown inductance (assumed constant with frequency). MATCH inductance is calculable using OPEN. LRRM requires one MATCH standard, whereas LRM needs two. LRRM requires the same set of standards as SOLT but requires less information about the standards. This can give better results than SOLT and is less sensitive to small errors in probe placement.

- Multi-Line TRL (MTRL), developed by NIST, has become established as a reference calibration technique. MTRL involves multiple lines and uses all lines, to some extent, at all frequencies. Varying weighting is applied to all the LINE data to resolve the problem of band breaks of conventional TRL.

It is important to understand strengths and limitations of each calibration technique. Table I gives a comparison between these techniques. Note that the optimum calibration technique depends on the exact measurement requirements. Verification standards can be used to compare different calibration techniques.

Table I: Comparison between conventional calibration techniques. [1]

Calibration	Most Critical Standards	Accuracy
SOLT	SHORT, OPEN, LOAD, THRU	+
LRM	LINE, MATCH	+ +
LRRM	LINE, MATCH	+ +
TRL	LINE	+ +
Multiline TRL	LINE	+ + +

There are two common calibration approaches:

- Probe tip calibration using ISSs (off-wafer) + de-embedding using additional on-wafer structures (optional)

- On-wafer calibration using standards fabricated on the same wafer as the Device Under Test (DUT).

III. TRL Calibrations Using Different Reflect Standards

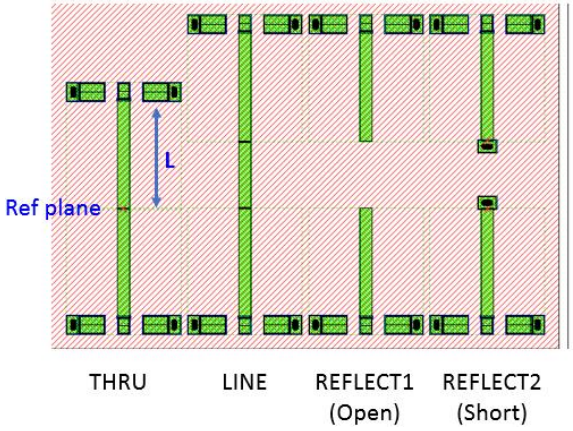
TRL is a popular on-wafer calibration method, with the minimal requirement on prior knowledge of the standards. In addition, the desired reference plane for calibration can be set the same as the DUT. Therefore, TRL is ideally suited to on-wafer measurements for DUTs with the same reference plane and lead structure.

A TRL calibration was applied to the measurement of some D-band (110-170 GHz) integrated circuits. The circuits and the TRL calibration standards were fabricated on the same GaAs substrate with a thickness of 50 µm. Two sets of TRL standards were produced, and the layout of one set of these standards is shown in Fig. 4 (a). The first set has launches from the GSG pads to the reference plane of 300 µm length (i.e. L=300 µm), the second set has 100 µm long launches. The launches should be

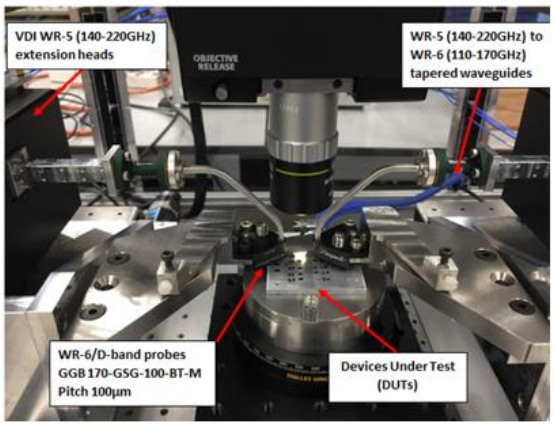
sufficiently long so that the microstrip mode can be fully established by the time it gets to the reference plane. EM full wave modelling of the launch can be carried out to calculate the optimum length. On the other hand, the launch length should be no greater than $\lambda_g/8$ [2], otherwise the LINE standard would behave like a $\lambda_g/2$ resonator and bring in resonance to the transmission response. In this work, the 100 µm long launches fulfil this requirement, and the 300 µm long launches are considerably longer than $\lambda_g/8$.

For TRL calibration, the REFLECT standard can be either a SHORT or OPEN. In this work, both types of circuits have been implemented and utilised for de-embedding the raw measurement results of the verification device.

The measurement was carried out at NPL on a manual probe station. The setup shown in Fig. 4 (b) was used to obtain uncorrected raw data for the TRL calibration standards and the DUT (verification line). This was then postprocessed by implementing the four different TRL calibrations (i.e. L=100 µm or 300 µm, and OPEN or SHORT as REFLECT standard). This approach minimises the uncertainty due to contact repeatability. The corrected results are shown in Fig. 5. It was found that better agreement with the physical structure of the verification line was obtained using the 100 µm launches because the 300 µm calibration set yielded transmission responses close to 0 dB at the high end of the frequency band which does not agree well with theory. The processed results using calibrations with different REFLECT standards are also shown in Fig. 5. There is not any noticeable difference between the results based on SHORT and OPEN.



(a)



Test setup at NPL, for 140-170GHz

(b)

Fig. 4. (a) Diagram of the TRL calibration standards fabricated on the same wafer as the devices. (b) Test setup at NPL, for D-band on-wafer measurements.

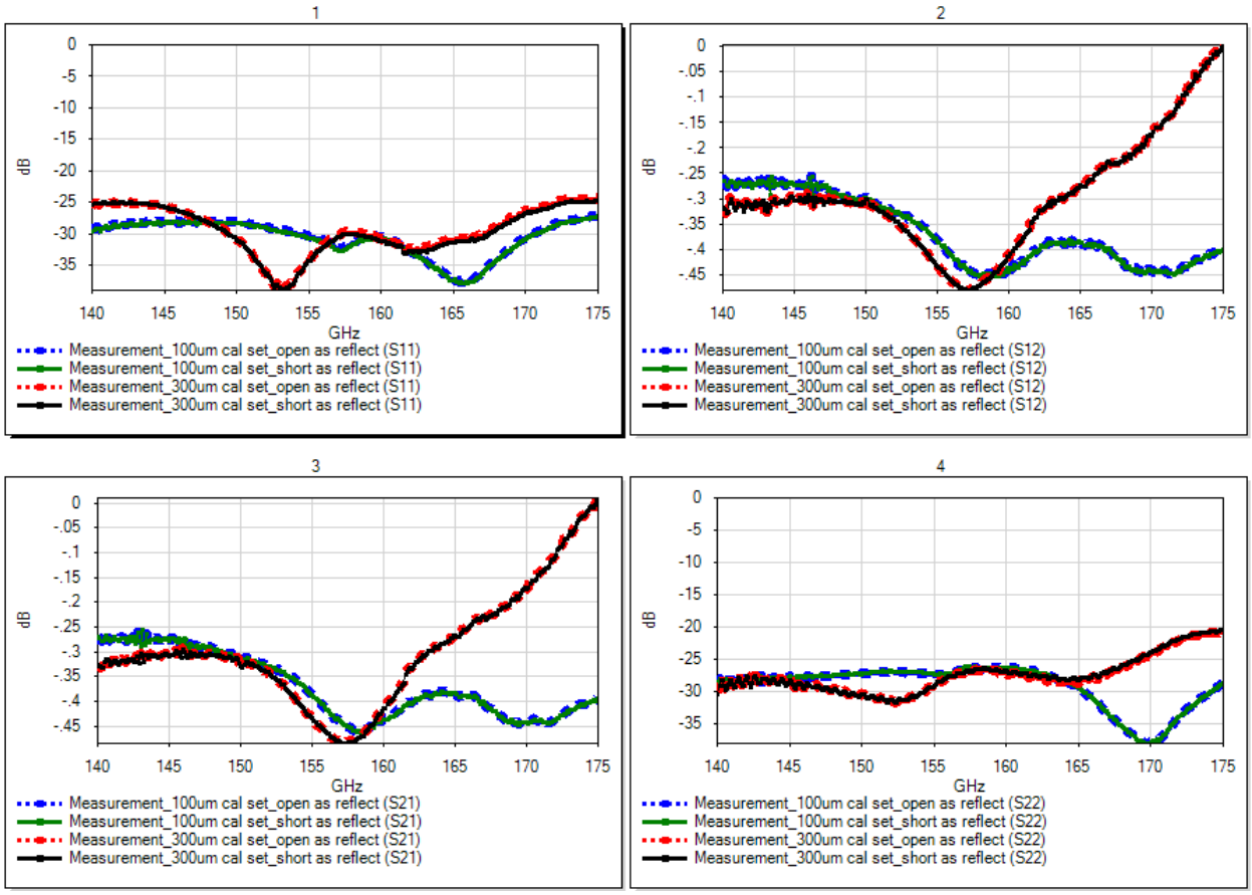


Fig. 5. Measurement results of the verification line subject to TRL calibrations using 4 different sets of standards (i.e. L=100 µm or 300 µm, and OPEN or SHORT as REFLECT standard).

IV. Impact from Neighbouring Structures

For on-wafer measurements, the probe shadow region should be kept free of structures, to avoid coupling between probes and the nearby structures surrounding the DUT or calibration standards, as shown in Fig. 6. Otherwise, there will be noticeable dips (or resonances) in the measured transmission responses, regardless of the calibration techniques employed. This is also discussed in detail in [3] and [4].

The impact from neighbouring structures has also been studied in [5]. Full wave simulations have been carried out for a microstrip line with a short microstrip line nearby. The modelled structures together with the simulation results are shown in Fig. 7. It can be observed that the frequencies of these dips in the transmission responses are related to the lengths of the neighbouring lines. More dips could occur in the transmission responses if there were more than one neighbouring structures. This would degrade the accuracy of measurement and calibration.

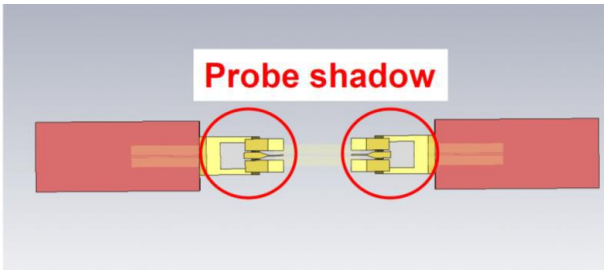


Fig. 6. Illustration diagram showing the probe shadow, where couplings between the probes and neighbouring structures may exist. This figure is reproduced from [4].

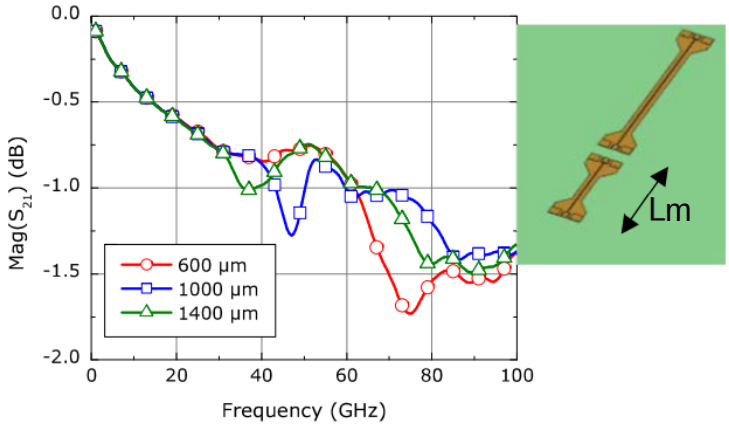


Fig. 7. Simulated S_{21} of a microstrip line together with a nearby short microstrip line with three different lengths Lm. The frequency of dip in S_{21} response changes when Lm varies from 600 µm to 1400 µm. This figure is reproduced from [5].

Fig. 8 (a) shows the layout of TRL calibration standards for on-wafer measurements at E-band (60-90 GHz). A line was measured after TRL calibration, and there is a dip (resonance) in the measured S_{21} response, as shown in Fig. 8 (b). Similarly, the measured S_{11} of an OPEN exhibits an unwanted resonance, whereas the S_{22} seems normal, as can be observed from Fig. 8 (c). This is due to the calibration standards being too close to each other, resulting in coupling and parasitic from the neighbouring structures underneath the probes. To address this problem, the metal layer was removed from some areas of the calibration standards, as shown in Fig. 8 (d), so that the probe coupling to neighbouring structures was considerably reduced. A TRL calibration based on these modified standards was performed and the same devices measured. The corrected results are given in Fig. 8 (b) and (c). The unwanted resonances have been eliminated. This demonstrates that the calibration standards need to be properly separated on the wafer and no other standards or test structures should be underneath the probes during the calibration and measurement.

The impact from neighbouring structures on on-wafer measurements can also be reduced by utilising special probe-to-pad transition, as shown in Fig. 9 (a). The closed and shielded probe-to-pad design has proved to be very effective, in terms of suppressing the influence from crosstalk, higher-order modes and neighbouring structures. This is demonstrated at D-band (110-170 GHz), using a set of calibration standards and DUTs that are placed close to each other on the same wafer, as shown in Fig. 9 (c). Both the closed and shielded probe-to-pad design and the conventional design [see Fig. 9 (b)] have been implemented and measured. The former offered better performance and greater consistency in results from different organisations, as described in detail in [6].

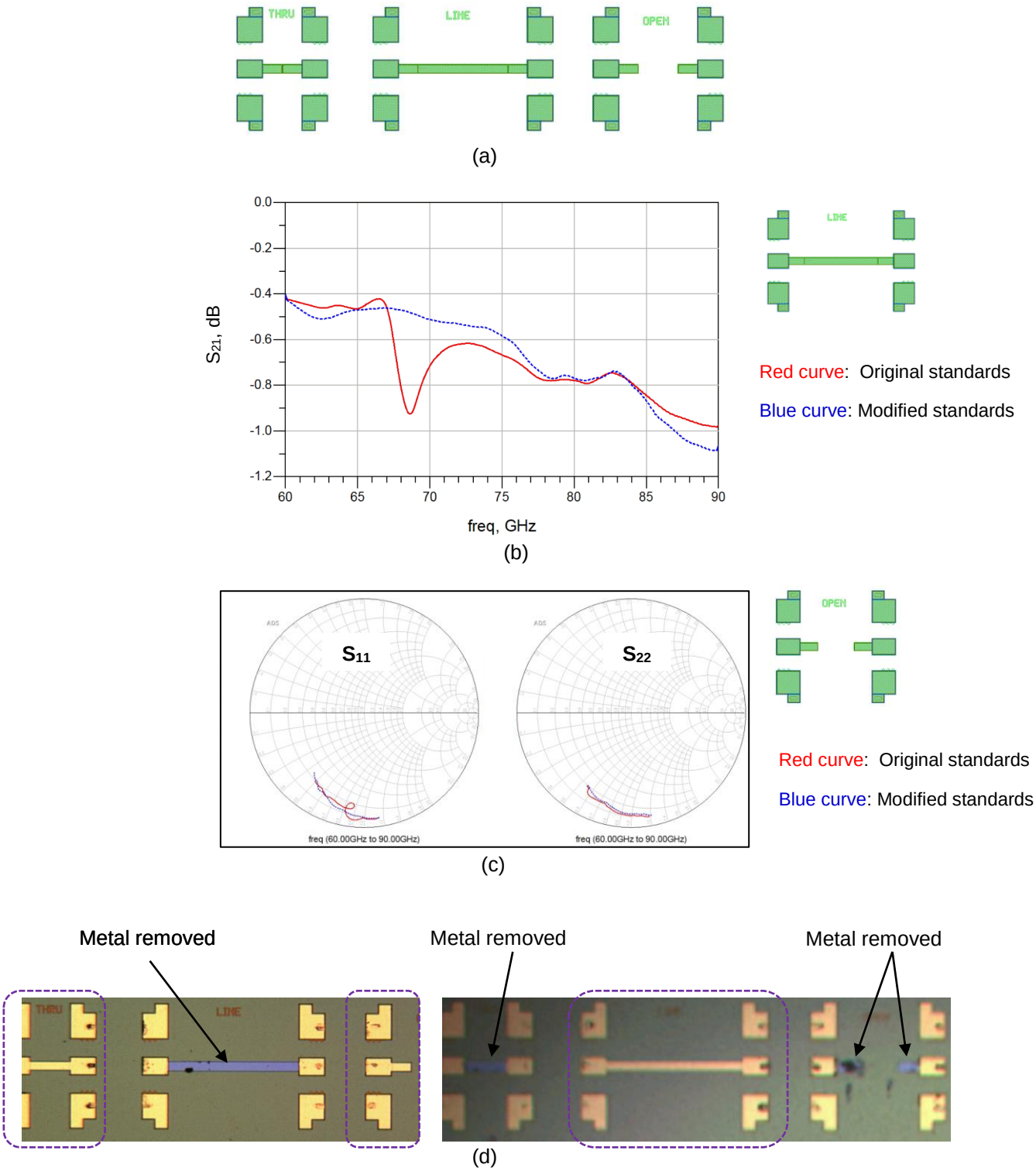


Fig. 8. (a) Layout of the TRL calibration standards for on-wafer measurement at E-band (60-90 GHz). (b) Measured S_{21} responses of the Line subject to two calibrations, one using the original calibration standards, and the other using the modified standards with metal selectively removed. (c) Measured S_{11} and S_{22} responses of the OPEN, subject to two different calibrations. (d) Photographs showing the modified calibration standards after selectively removing metal from some areas. Purple rectangles indicate the standards used during the TRL calibration.

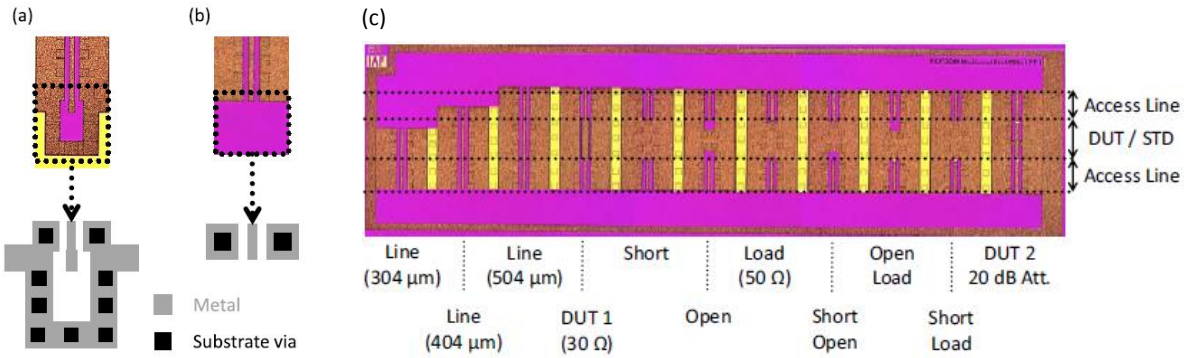


Fig. 9. A set of CPW calibration standards and DUTs fabricated on a 50 µm thick wafer. Two different types of probe-to-pad transitions are shown. (a) Closed and shielded pad configuration, capable of offering lower crosstalk, less higher-order mode interference, and less neighbouring effects. (b) Direct probing contact configuration without any special probe-to-pad design. (c) Layout of the calibration standards and DUTs only. Both types of probe-to-pad transitions were implemented and characterised. This figure is reproduced from [6].

V. Testing Boundary Conditions

At millimetre-wave frequencies, the testing environments (e.g. boundary conditions) have a significant impact on measurement quality. Fig. 10 shows the experiment setups for the same device that was placed on two different types of sample holders, one is a Cascade absorber holder (PN 116-344) and the other is glass. Their corresponding return loss performance can be found in Fig. 11, in which the response without sample holder under the substrate is also given for comparison. It is evident that the absorber holder has reduced the ripples in the measured responses effectively. These ripples are introduced by unwanted spurious modes usually excited at frequencies higher than 50 GHz [7]. If the device is placed on a metallic chuck, a small fraction of the signal can propagate as microstrip modes in that the chuck acts as the ground plane. The absorber holder is capable of suppressing these modes and ultimately reducing the ripples. Note that the DUT is effectively a different structure (electromagnetically) with and without the absorber. Therefore, boundary conditions need to be specified during measurement comparisons.

The absorber effectively acts like a lossy boundary during measurements, which has an impact on the loss and relative phase constants as well as the characteristic impedance of the CPW lines [8]. This may result in an inaccurate definition of the calibration reference impedance at high frequencies. More discussions on this topic can be found from [8], which reports on a detailed investigation into different boundary conditions and their impacts on calibration accuracy. Note that there is still active research in the testing boundary conditions, particularly at millimetre-wave and terahertz frequencies.

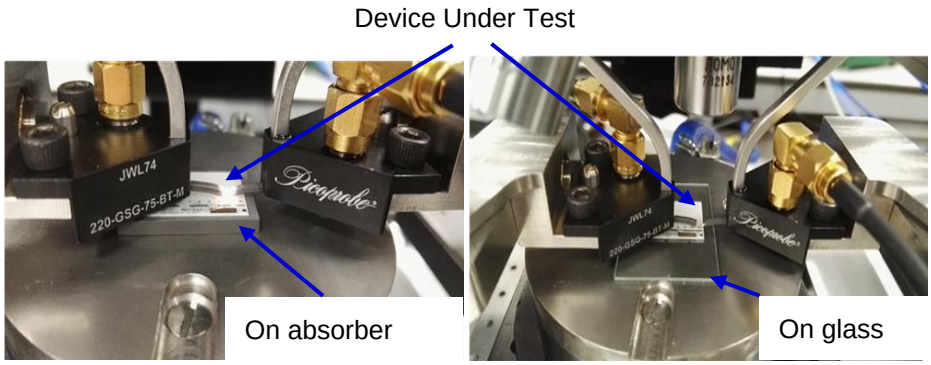


Fig.10. Photographs of two different experiment setups with different boundary conditions.

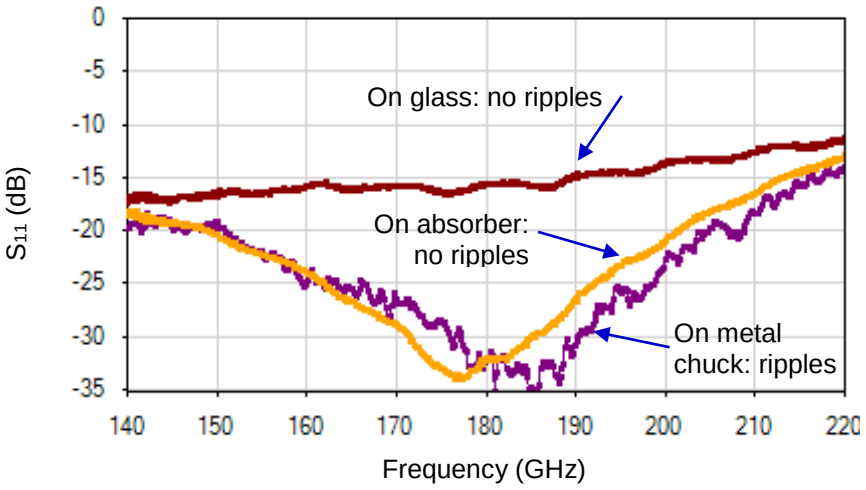


Fig. 11. Measured S_{11} of the DUT with different experiment setups shown in Fig. 10.

VI. Other Considerations for Planar Measurements

There exist many other factors that impact the accuracy of on-wafer measurements, these factors include design of CPW, probes with different pitch sizes, contact repeatability [9], cross-talk between probes [10], etc. This section includes a brief discussion on the first two factors. The investigation was carried out by colleagues across Europe and was described in detail in [3] and [4].

Design of CPW

Measurement quality also depends upon the design of CPW, particularly the ground width and the ground-to-ground spacing. Dips may occur in the transmission responses (i.e. S_{21} and/or S_{12}), as shown in Fig. 12, and this is attributed to radiation from the CPW and the ground plane. Full-wave simulations indicate that the total CPW width (W_{tot}) determines the frequency where the dip occurs, and the ground-to-ground spacing influences the significance of the dip behaviour [4], as shown in Fig. 12 (b) and (c). Minimizing ground-to-ground spacing is helpful in terms of eliminating the dips.

Fig. 12 (d) exhibits the relationship between the CPW width and the dip frequency. To avoid the appearance of such dips, the recommended total CPW width can be calculated as follows [11].

$$W_{tot} < \frac{2 \times c}{f_{max} \times \sqrt{2 \times (\varepsilon_r - 1)}}$$

where c is the velocity of light in free-space, ε_r is the relative permittivity of substrate, and f_{max} is the upper frequency limit. There is excellent agreement between this equation and the full-wave simulation results, as shown in Fig. 12 (d).

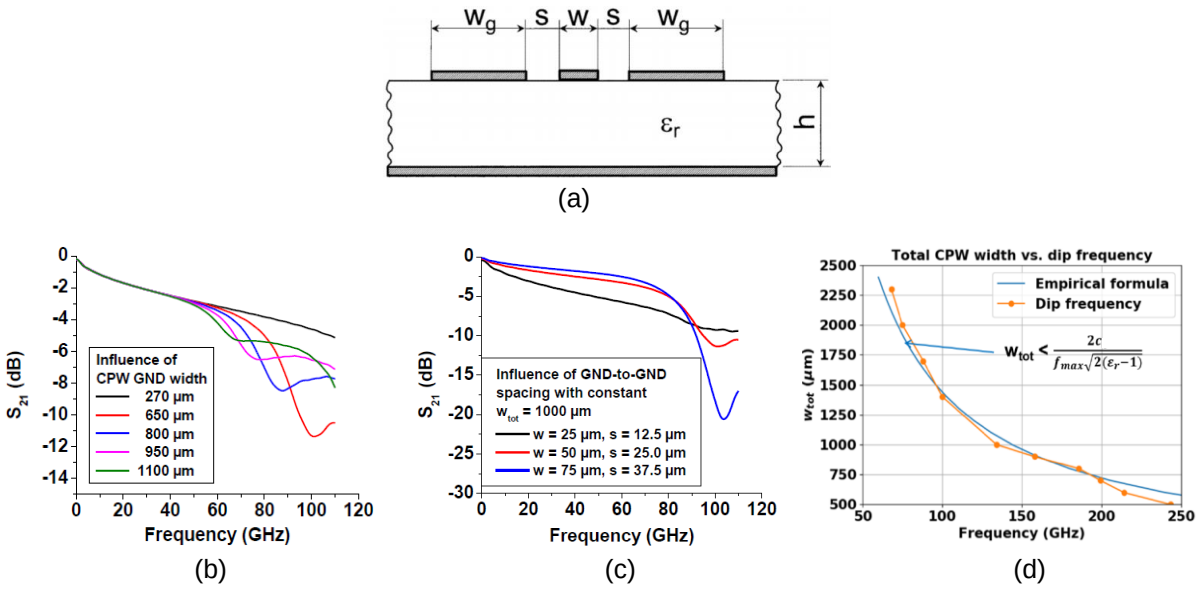


Fig. 12. (a) Illustration diagram of the CPW. The total CPW width, W_{tot}, equals to W_g+S+W+S+W_g. (b) Simulated transmission response as a function of frequency, for different CPW ground width W_g. (c) Simulated transmission response as a function of frequency, for different ground-to-ground spacing S, whilst maintaining a characteristic impedance of 50 Ω and a width W_{tot} of 1000 µm. (d) Relationship between W_{tot} and dip frequency. The orange line was extracted from full-wave simulations whereas the blue line was plotted using the equation. These figures are reproduced from [4].

Probes with different pitch size

Probes of different pitch sizes can result in noticeable difference in on-wafer measurement results. Fig. 13 shows the error-corrected measured transmission responses of an attenuator using GGB probes with two different pitch sizes (100 µm versus 150 µm). The experiment was performed at PTB in a closely controlled environment, with the same measurement setup, calibration structures, chuck material (testing boundary), and the same operator. It can be observed from Fig. 13 that, there exists a systematic deviation for frequencies above 50 GHz, this can be attributed to the difference in probe geometries. It is expected that probes from different vendors could lead to even larger deviations in *S*-parameter results.

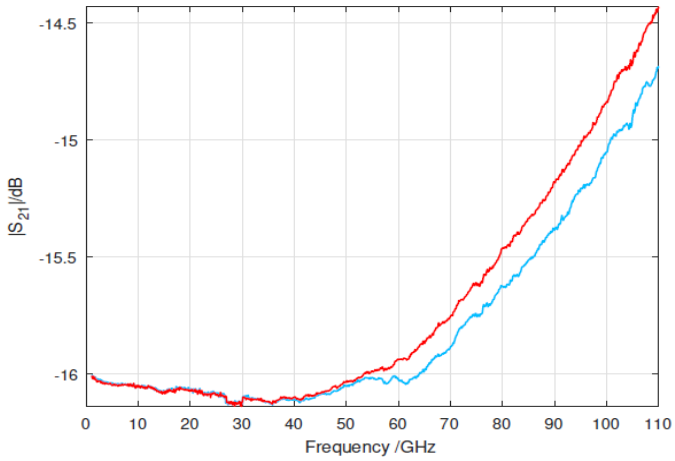


Fig. 13. Influence of probe pitch width (blue – 100 µm, red – 150 µm) on transmission measurement of an attenuator. This figure is reproduced from [3].

VII. Conclusions

This paper has briefly reviewed conventional calibration techniques for on-wafer measurements. Some recent research activities in on-wafer measurements, at millimetre-wave frequencies, have been reviewed. Other considerations, e.g. repeatability of calibration, definition of reference plane, test environment, parasitic mode effects, etc, have not been covered in this paper. However, these also play an important role in the on-wafer measurement quality and should be taken into account for precise measurement.

Acknowledgements

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