WHAT ARE THE LIMITS TO INCREASING THE DYNAMIC RANGE OF RF ADCS?

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1. Introduction

The dynamic range of an analogue to digital converter (ADC) can be specified in several ways which are application dependent. This problem has been addressed in industry by the International Electro-technical Commission (IEC) standard for dynamic specifications for ADCs [1]. The most often used specification for RF applications is Spurious Free Dynamic Range (SFDR). This is specified in the frequency domain through analysis of a suitable test signal such as two tones of equal amplitude. SFDR then indicates the range in amplitude between the maximum test signal amplitude and the amplitude of any unwanted or spurious signal. These spurious signals may be related to the presence of the test signal or they may be from other sources.

They represent a lower limit to the ability of the RF ADC based system to measure low level signals in the presence of high amplitude signals. Typically, RF ADC manufacturers specify SFDR and effective number of bits (ENOB). ENOB is calculated from the signal to noise and distortion ratio (SINAD) of the ADC by comparing it with the SINAD in dB of an ideal ADC. For a sine-wave:

ENOB = (SINAD -1.76)/6.02 bits.

Perhaps surprisingly, an ADC with a low SINAD figure can actually have a high SFDR if it is sufficiently linear. There is therefore a need to produce a dynamic range figure of merit that can be applied to ADC data sheet results. This will be covered in the following sections of this paper and will describe methods that can extend the dynamic range of ADCs beyond the data sheet limits.

2. The importance of RF ADC spurious free dynamic range

Ideally, an RF ADC would have sufficient dynamic range to allow all the analogue circuitry between it and the signal source to be eliminated. All signal processing would then take place in the digital domain. This is the ultimate goal of a software defined radio system.
The SFDR of the ADC is a key factor that restricts how much additional analogue signal processing circuitry must be used between the devices and the antennae [2],[3],[4]. This issue is recognized as a key problem in the defence research area internationally. SFDR limits the useful range and resolution of RADAR [5] and the service area of communication systems. Some results of defense funded projects in the UK, Australia and the USA have been published [6],[7],[8],[9],[10].

In addition, commercial development and competition to produce higher SFDR ADCs has increased dramatically [11], [12], [13] owing to the rapid increase in the number of consumer digital cellular (or mobile) telephones. Commercial developments have been primarily in circuit designs that take advantage of advances in semiconductor processes. Improved mathematical modelling of ADCs to better predict SFDR generation is also a concern

[14],[15]. The specification of mobile handsets and base stations drives commercial designs. Digital mobile systems have evolved from second generation voice and limited bandwidth data (2G) to 2.5G with wider bandwidth data services and now much wider bandwidth 3G and 4G with multi-media services [16]. The evolving 5G network specifications and standards are expected to be even more demanding of SFDR and bandwidth.

The SFDR of the cellular base station is important as it is one of the factors that limits the number of handsets that can be serviced within a given area [17],[18]. Increased data rate requires wider bandwidths and battery operation requires lower power circuits. The circuit designer faces conflicting challenges as for a given circuit, both increased bandwidth and increased SFDR require increased power. This has resulted in commercial research and development of new circuit topologies and semiconductor processes that reduce the power required [19].

Defence research has also addressed this problem but the bandwidths and SFDR goals are beyond those of commercial systems. The use of some signal processing techniques to improve SFDR often involves a penalty in terms of cost and power consumption. It is for these reasons that they are not used routinely in commercial designs. This has resulted in a misunderstanding of the advantages and disadvantages of the techniques, which has resulted in companies being slower to adopt them. What is required is a figure of merit that puts into perspective the importance of the data sheet specifications.

3. RF ADC Figure of merit

The quality of the analogue-to-digital and digital-to-analogue conversion process is related to the extra 'noise' and unwanted spectral products introduced by quantization and non-linearities in the quantizer characteristics. For a linear PCM encoder / decoder, the quantization noise is determined by the number of bits in the ADC and this determines the resolution. The deviation of the quantizer characteristic from the ideal staircase transducer gives rise to non-linearity distortion and additional quantisation noise. In general this deviation may have both a static and a time varying component and may be caused by inaccurate components and imperfections in the manufacturing process. The dynamic range of the conversion process is determined by the maximum input level before overload and the level of unwanted spectral products contributed by quantization and non-linearity.

For all realizable quantizers, the threshold levels between quantization intervals are liable to be displaced from their nominal positions. This deviation from the ideal characteristic can be considered as a source of distortion added to the output together with the quantization noise. We can therefore express the performance of an ADC in terms of the effective number of bits and signal to noise ratio in dB. As the bandwidth increases, usually more power is required to maintain the same effective number of bits. It can be shown that this is related to the aperture error or aperture jitter in the sampling process inherent in an ADC system and is independent of the architecture of the ADC. Assume that for an n bit ADC, the maximum allowable error e of a sine wave of peak value A is one quantising interval hence

$$e = A/2^{n-1}$$

It can be shown that the maximum slope of a sine wave of frequency f is $A.2.\pi f$. Hence the maximum allowable aperture time t for an n bit ADC is approximately

$$t = 1/(2^n.\pi f.).$$

If f represents the maximum bandwidth of the ADC then the sampling frequency is 2f.
Clearly, to be architecture independent a figure of merit must take into account the number

of bits of the ADC and its sampling rate. Doubling the sampling rate requires one less bit to maintain the same aperture time. Belcher [20,21] proposed that this figure should be:

$$\text{FOM} = \text{ADC bits} + \log_2 \text{ADC(sampling frequency)}$$

Furthermore, doubling the power will usually enables one more bit or twice the bandwidth to be obtained so a more complete version of the FOM was proposed [22]:

$$\text{FOMp} = \text{ADC bits} + \log_2 \text{ADC(sampling frequency)} - \log_2(\text{power relative to 1 watt})$$

Beginning in 1985, a survey was undertaken [20] of the state of the art of ADC FOM over time for 8, 12 and 14 bit ADCs. This covered commercially available and devices reported in research papers. The survey was updated regularly for commercial reasons [23]. In contrast with other surveys this presents only devices that have the highest FOM for each year so is technology and application independent. For the first time, the result of this survey is presented in Figure 1. A line drawn on the figure with a slope of 0.5 FOM per year shows that ADC technology has progressed at roughly that rate in the early days of ADC development.

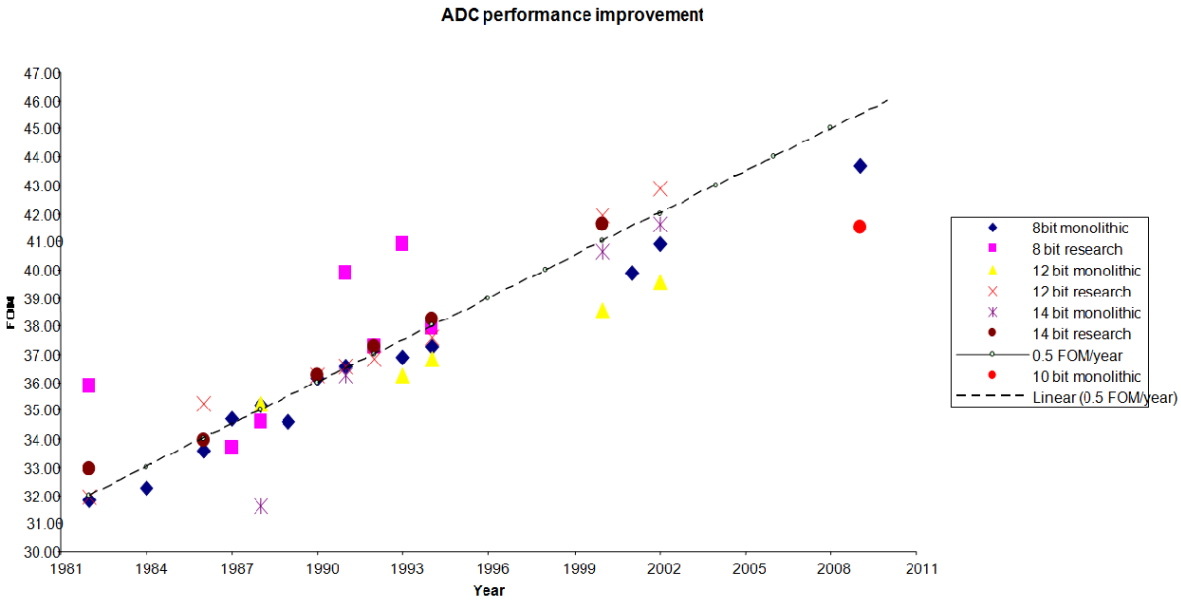

Figure 1 ADC FOM state of the art progression

It is possible to undertake a completely different survey that includes all ADCs and this shows where manufacturers are concentrating their efforts but not what is technically possible. Such a survey was undertaken by Walden for the US Defence Advanced Research Projects Agency (DARPA) in 1997 and the results published in 1999 in Figure 2.

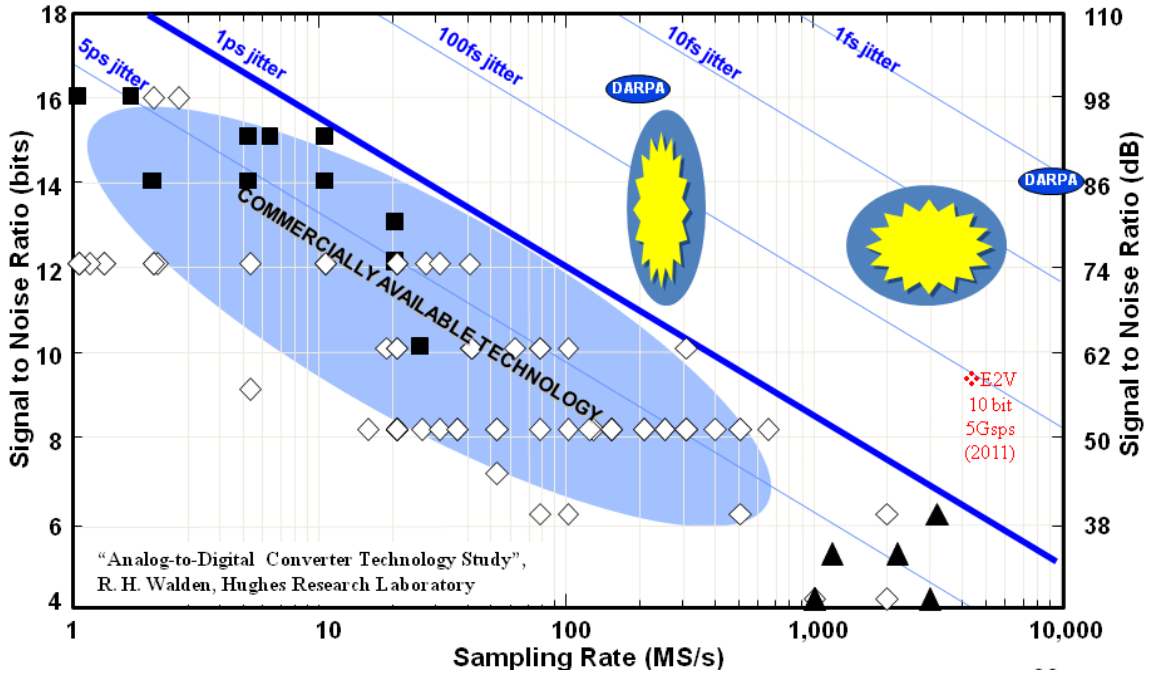

Figure 2 Walden survey presented at IEE ADDA99 international conference

In Figure 2, the figure of merit is rms aperture jitter and is related to the log of the sampling frequency and the ADC number of bits or signal to noise ratio. This approach is based on aperture error so has the same starting point as the FOM. It shows that in 1997 the commercially available ADC technology had an aperture jitter limit of about 1ps or an FOM of about 39. This is in close agreement with the survey by Belcher in Figure 1. It is clear from Figure 2 that one of the DARPA requirements was in the region of 100fs jitter or an ADC FOM of 42 to 43. It has taken commercial ADC manufacturers at least 10 years to achieve this FOM and one example from the European company E2V is shown in red.

Belcher has proposed a variation of his FOM that includes 'bits' of ADC spurious free dynamic range, instead of resolution. This is

$$FOM_{SFDR} = (SFDR(dB)/6) + \log_2 \text{sampling frequency}$$

It was produced to highlight the fact that in RF systems, often the ENOB is not the primary performance figure.

As an example of the present state of the art, National have a 10 bit 3Gsps ADC with 9 ENOB and 70 dB SFDR.

The ENOB based FOM is 31.5 + 9 = 40.5
The linearity based FOM_{SFDR} is 31.5 + 11.66 = 43.16

Advances in semiconductor process technology provide increased f_t and f_{max} but not generally an increase in the precision of analogue components. These parameters relate to the bandwidth and power consumption of the ADC. An ADC of up to 8 bits resolution usually has poor linearity or SFDR. The world leading companies in test and measurement instrument manufacture are able to maintain their position by investing in leading edge proprietary IC processes as this enables them to produce ADCs that have a higher FOM than any commercial of the shelf (COTS) ADC. These instrument manufacturers have taken the step of making available their ADCs to customers that can accept a high unit cost and

who not compete with their instrumentation market. Typically these customers are in the defence industry. Analogue circuit designers strive to do the best ADC design for a given specification and this may represent the state of the art for a particular number of bits and SFDR. The following section will demonstrate that this need not be a limit to the dynamic range of an RF ADC system. It is possible to use signal processing to increase dynamic range in exchange for a reduction in sampling frequency. This approach is particularly relevant to software defined RF receivers. In contrast to methods that use oversampling, such as sigma delta modulation, the method to be described next works with conventional ADCs without oversampling the input signal i.e. at the Nyquist rate

4. Going beyond the limits of RF ADC dynamic range

When ADC designers have reached their dynamic range performance limits, signal processing in the ADC system can enable this limit to be increased by a significant amount. Unfortunately the use of signal processing techniques to improve SFDR often involves a penalty in terms of cost and power consumption. It is for these reasons that they are not used routinely in commercial designs. This has resulted in a misunderstanding of the advantages and disadvantages of the techniques, which has resulted in companies being slower to adopt them. The increase in design time and risk is clearly a factor in the decision to use signal processing to provide a commercial edge. ADC and DAC circuit designers now generally make use of publicly available semiconductor foundries. The final performance therefore depends on the detailed circuit design and choice of signal processing. During recent years there has been an increase in the number of papers published in this area and the key signal processing methods that increase SFDR will be covered here. These methods fall generally into the categories of SFDR improvement by ‘code-mapping’ or by ‘dynamic correction’. A brief description of the methods will be presented next.

‘Code mapping’ is used to describe a signal processing technique that takes the digital input word, which represents the signal with distortion, and then uses it to address a look-up table, which generates an output word with less distortion. Reducing the distortion results in an increase in the SFDR.The look-up table can be multi-dimensional: this enables the amplitude, frequency and history of the test signal to be used. The look-up table is generated by using a reference test signal with signal processing to measure the distortion and calculate the table entries needed. This signal processing technique is, in effect, calibration. A periodic re-calibration process can be used if enough ‘dead-time’ is available, when no radio signal is being received. This can compensate for drift in the ADC characteristic. Test time, accuracy and repeatability of testing or characterization methods are therefore key issues in the design of code-mapping systems. Some of the instrumental difficulties in using this for very high speed ADCs can be overcome by including a test core on the ADC chip [24].

In practice, code mapping is limited in its success. It is difficult to produce a code map that tracks the variation of distortion with localized circuit heating effects. This is produced by signals that invariably have different amplitude density functions and bandwidths to the test signal. For example, a flash ADC with a sine wave signal will turn on comparators used at the extremes of the reference range and cause localized heating and drift only on that part of the chip. If noise is used it will turn on comparators mainly in the middle of the reference chain causing selective heating in a different region. These effects become significant in the high (> 50dB) SFDR required for radio systems. If insufficient history is included in the code map SFDR improvement may reduce over time and with signal frequency. The large digital memory required therefore limits the upper sampling rate at which this type of correction can be used.

One example of dynamic correction is statistical averaging which changes the statistics of the encoded signal so that distortion components introduced by the ADC or DAC become de-correlated with the wanted signal. Subsequent averaging can then reduce the amplitude of the distortion relative to the wanted signal and thus increase the SFDR. One recognized technique is known as 'dither' [25] and a block diagram of this is shown in Figure 3. One example of this involves the addition of a pseudo random noise signal to the wanted signal so that distortion products introduced by the ADC are spread over a wider bandwidth. In principle, the pseudo random noise can then removed by subtraction, leaving only the wanted signal and de-correlated distortion. Although the total energy of the distortion is not reduced its energy per unit bandwidth is reduced and this increases the SFDR.

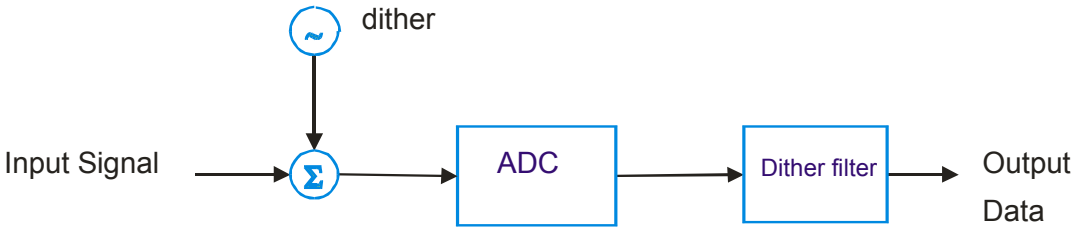

Figure 3 Dither

A key advantage of dither is that its effect is always present. Consequently, if the magnitude of the ADC distortion changes with time, dither may still be able to increase the SFDR. However, adding a dither signal can in some circumstances make the SFDR worse. For example, if an inappropriate amplitude of dither is used, distortion components from the dither may actually reduce the SFDR as they cannot be removed by cancellation. This problem can be overcome to some extent by using narrow band dither signals chosen so that dither distortion is out of band. These can then be removed by filtering. When subsequent averaging is required to increase SFDR, the signal processing may be already present in the form of filtering or Fourier analysis required to detect the wanted signal.

Interpolation is another dynamic correction technique that can be used to improve SFDR. This provides correction of a sample by averaging various quantized representations of that sample of the wanted signal. Compensation takes place by using statistical averaging over several quantizing points with one sample of the wanted signal. In effect, the amplitude of the deviation of one step from the ideal uniform staircase response (integral linearity error or ILE) is reduced by sharing the error over the other steps. Correction of the ILE of one sample then requires that averaging is performed over a fixed number of quantized results where the wanted sample value is the same in each case but where the amount of distortion varies. In this case a specific averaging function is used. A severe error in only one step of the staircase must be modelled by high order terms of a power series. When the error is spread over several steps it is not only the total rms error that is reduced but also the amplitude of the higher order terms in the ILE power series, which now contains mainly low order terms.

In general, for a given ILE error, lower distortion energy will be produced with an ADC that has an ILE characteristic that can be represented by a power series with low order terms. The extra quantized values used for interpolation may be provided by using a faster ADC or by using more ADCs operating in parallel on delayed versions of the input signal. When multiple transducers with delayed versions of the wanted signal are inherent in a communications system, e.g. with phased array aerials, then SFDR improvement may be obtained with a minimal increase in complexity. As interpolation increases linearity it may be possible to provide a further improvement by using dither. Without linearity improvement

dither may actually reduce SFDR and so is not always a viable option. Unlike code-mapping, the SFDR improvement provided by interpolation adapts to changes due to drift, signal frequency and signal amplitude probability density function and therefore always provides an SFDR improvement. A 'Direct Interpolation' method has been devised that has been shown to increase ADC SFDR beyond the limits of any other technique and works in conjunction with these other methods. It will be described in the next section.

5. Direct Interpolation: a Nyquist ADC system with software selectable dynamic range

An increase in FOM is technology driven so the FOM for a state of the art ADC is an indication of what FOM is technically possible. The availability and actual specification of a commercial off the shelf (COTS) ADC with a particular number of bits, bandwidth, spurious free dynamic range (SFDR) and power is determined primarily by market demand so only a limited combination of bits and bandwidth are available. History has shown that the performance of state of the art ADCs increases at the rate of 1 bit or a doubling in bandwidth every two to three years. A Direct Interpolation (DI)-ADC configuration [26] enables an increase in one bit for each halving of the sampling rate and it therefore preserves the FOM and offers a potential solution to increasing the dynamic range in an ADC problem.

Figure 4 depicts the main components of a DI-ADC system

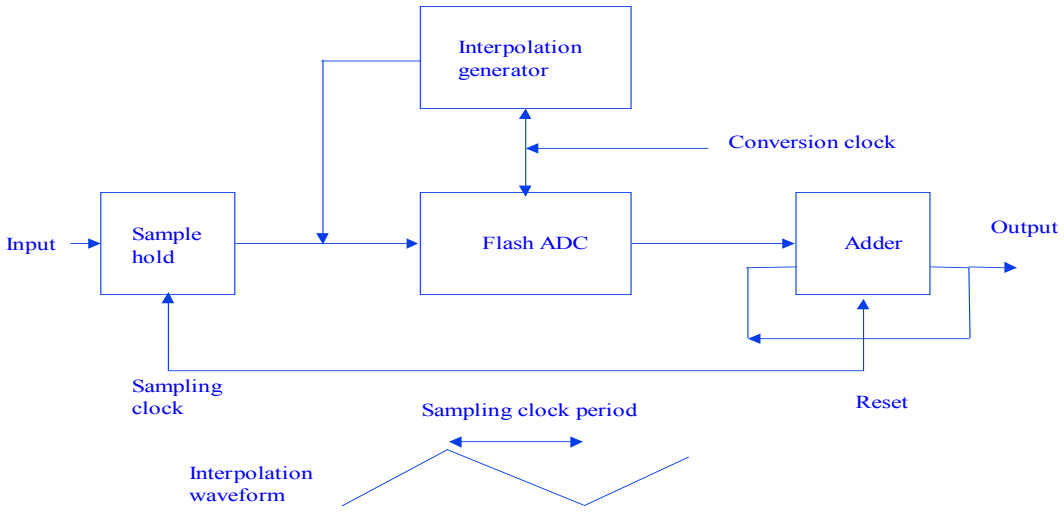

Figure 4 Direct Interpolation

It is important to note that the input signal is sampled at a Nyquist rate determined by the frequency of the sampling clock for the sample-hold. During the hold time, a staircase interpolation waveform is added to the ADC input. The ADC makes one conversion for each tread on the staircase. A digital accumulator (or Sinc filter), provides the average value of the ADC output code over the hold period and low pass filters ADC and sampl-hold noise. Discontinuities in the linearity error characteristics are reduced by averaging several ADC results during one sampling period of the analogue input signal. Linearity errors due to drift

etc are therefore compensated for on a sample by sample basis. This DI-ADC system therefore enables the linearity or spurious free dynamic range to be increased beyond the limits of the internal ADC. As the internal ADC converts at a rate greater than the Nyquist rate the ratio of these two rates is an 'oversampling factor'. It is important to note, however, that oversampling of the input signal does not take place. For an ideal ADC the averaging process can be used to increase the resolution of the ADC by one bit per octave increase in 'oversampling factor'. A Direct Interpolation (DI) ADC system therefore enables an exchange between bandwidth and resolution/linearity to be achieved while preserving the Figure of Merit (FOM). One state of the art ADC in a DI-ADC system can therefore provide state of the art FOM for narrower bandwidth applications requiring a higher number of bits and SFDR. In comparison with other possible ADC methods for exchanging dynamic range and bandwidth, DI avoids the problems of feedback loop instability and power required by intensive digital signal processing. SFDR improvement by DI is a dynamic effect that can track changes in the ADC non-linearity without need for re-calibration.

The principle source of accuracy limitations in the DI system is the internal ADC. Two types of internal ADC have been evaluated for the DI system: flash and successive approximation converters. These converters generally exhibit both random and systematic linearity errors. In general the degree of performance enhancement of the DI conversion system depends on the detailed distribution of the linearity error (position and magnitude of each threshold deviation). Therefore, it is not sufficient to assume an arbitrary distribution of error magnitudes for the analysis of the system. It can, in principle, be used in combination with dither, conventional code-mapping and phase-plane error correction.

One implementation of the DI system included an 8 bit 2.5 Gsps flash ADC manufactured by Rockwell in GaAs. The SFDR for the basic ADC and the resulting 40dB increase [6] when DI is included is shown in Figure 5.

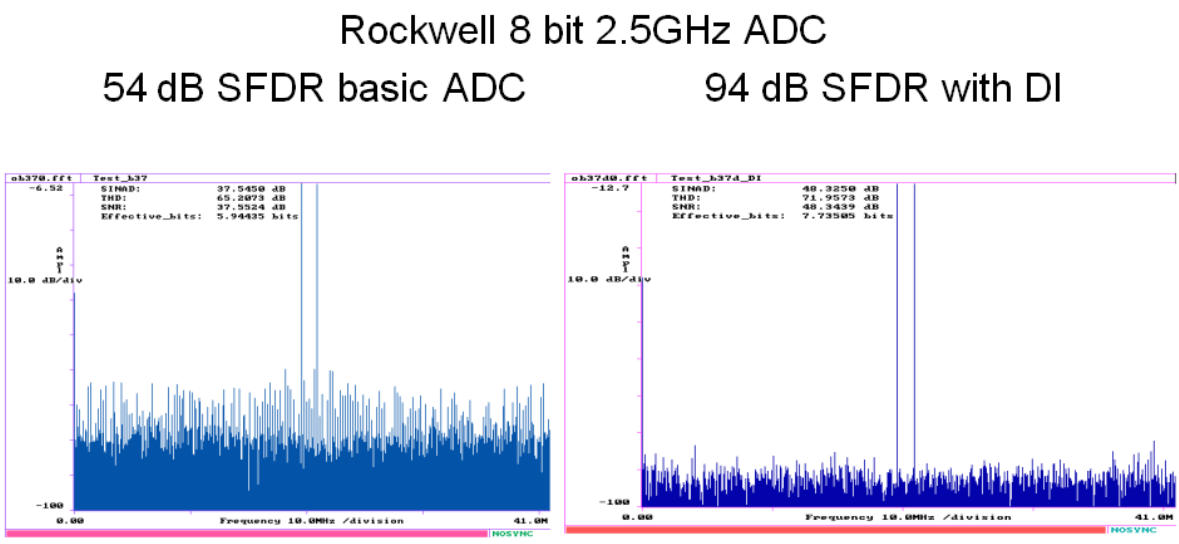

Figure 5 DI ADC SFDR results

In Figure 2 the availability of a 10 bit 5 Gsps from E2V was highlighted. It has been used with significant success in a DI-ADC experiment for a direct RF receiver at Cardiff University. The left hand side of picture below in Figure 6 shows the E2V ADC evaluation board inserted in an Xilinx FPGA evaluation card as part of a DI-ADC laboratory demonstrator. On the right hand side of Figure 6 is the GHz bandwidth track-hold. The laboratory demonstrator is essentially an experimental system using a combination of off the shelf parts and bench top equipment.

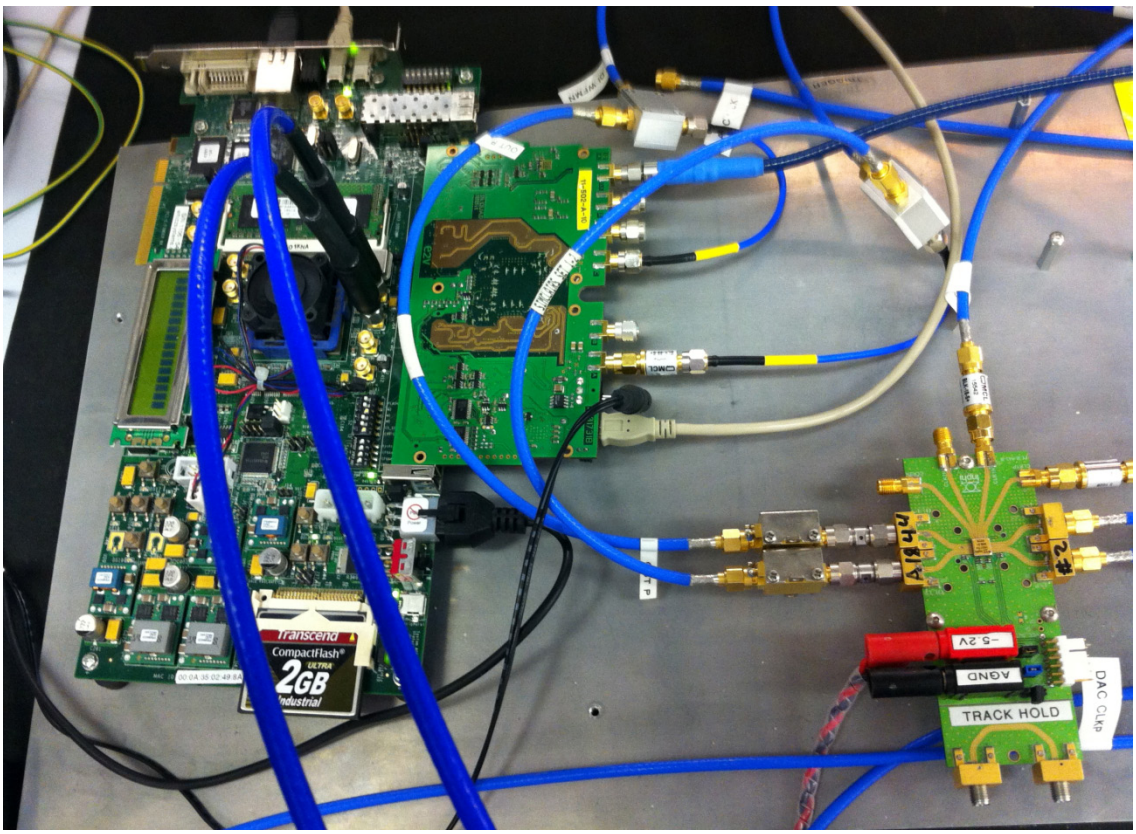

Figure 6 Experimental RF/Microwave DI-ADC including Track-hold

For clarity, the Interpolation waveform, and timing signal parts of the experiment are not shown here. These waveforms and signals were generated with a Tektronix 10 bit 12 Gsps dual channel arbitrary waveform generator under GPIB control. An NI card cage based system was also part of the experiment. The complete DI-ADC test system control and automated testing software was written using National Instruments LabView [27]. Signal Conversion Ltd WinSATS [28] proprietary ADC signal processing and analysis functions were included in Labview as Virtual Instruments (Vi's) through the Microsoft .NET environment. Figure 7 shows a partial screen capture for the main front panel display. Only the experimental setup and sequencing options are shown. The right hand side of the screen is a separate set of displays that can enable the results to be viewed in several ways. A description of the detailed features of this Labview base test solution is beyond the scope of this paper but broadly the front panel display has the following control areas:

External ADC: chose direct capture from an ethernet connection to an FPGA card or via a shared data file

Single tone tests, Swept tone tests, Two tone tests: provides interactive choice of test configurations and generates a test plan shown in the Test Plan window.

Test plan window: enables single test point or multiple test points to be run.
Run time menu: enables FPGA/ADC timing calibration, real time data capture, sinle step, pausing capture, saving to WinSATS file format, spectrum capture from FSEB

Status window: Show the current and past command sequences running in the control system

Hardware settings: Selects default values for arbitrary waveform generator, ADC (NI or external ADC based) , GPIB and NI PXI based signal generators

AWG waveforms: displays all the waveforms generated for the DI-ADC system and enables timing to be changed graphically

Direct Interpolation settings: sets default values for the amplitude of the interpolation waveform, input test signal amplitude and interpolation factor

Analysis settings: sets the FFT record length and other FFT related analysis parameter values as well as DI filter configuration options

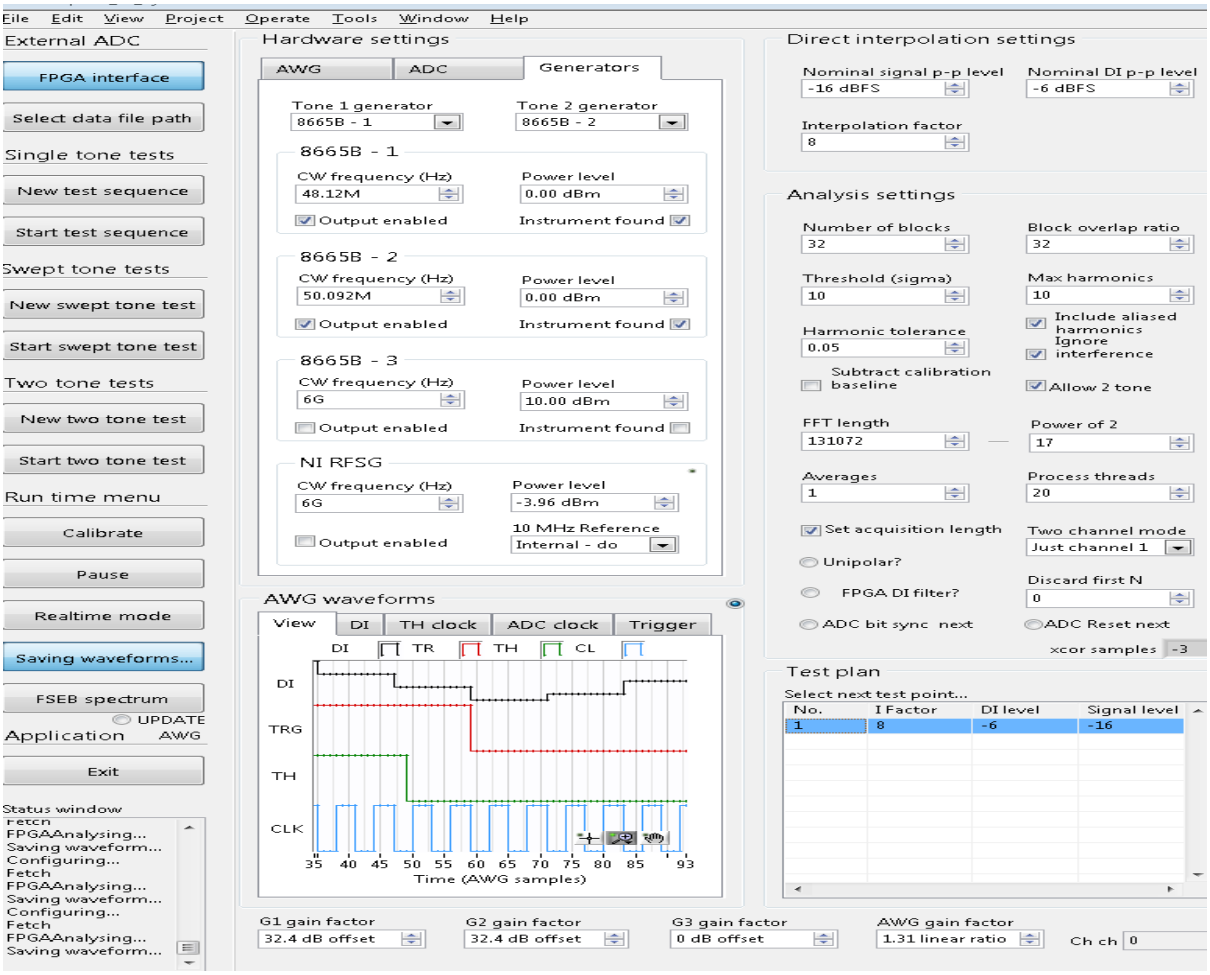

Figure 7 Partial Front Panel display: Experimental DI-ADC automated test system using Labview

The detailed results obtained by this experimental system will be the subject of future publications but in summary, two-tone SFDR was increased to a point where it was below the system FFT noise floor of 85 dBc. FFT noise floor was limited by the maximum size of waveform buffer that could be implemented in the FPGA evaluation card. A waveform buffer

was necessary in order to enable Labview to keep up with the real time data stream from the DI-ADC system.

6. Conclusions

This paper has presented a figure of merit approach that assists in interpreting data sheet information to select an RF ADC with a state of the art dynamic range. It also enables a system designer to take into account likely future technology trends in that could increase RF ADC performance. Signal processing techniques that can enable the ADC circuit limited dynamic range to be exceeded, at the expense of increase power and complexity, are described. These techniques may be of most value in system integration applications where an increase in dynamic range beyond that available from the stand alone ADC is of benefit. Example applications may be software defined radios or software configurable virtual instruments. One example of a potential application is presented: a Labview based software defined RF/microwave receiver demonstrator with a constant FOM and software selectable dynamic range.

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