Direct S-Band Communication Using Xilinx's RFSoC and Design-In of its Microwave Interfaces

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Abstract

Xilinx's RFSoC is a single-chip solution combining RF ADCs and DACs with a 16 nm, Zynq UltraScale+ MPSoC capable of implementing a complete software-defined radio including direct IF/RF sampling at the receiver and direct IF/RF re-construction at the transmitter.

12-bit, 4 GHz ADCs are available capable of sampling up to 2.058/4 GSPS allowing direct digitisation of UHF, L and S-band carriers within this input bandwidth, as well as 14-bit, 4 GHz DACs sampling up to 6.554 GSPS allowing reconstruction of IF/RF signals and direct up-conversion to the second Nyquist zone within this output bandwidth.

Portable, ground terminals for satellite communication and M2M applications are baselining RFSoC because it offers the potential to produce small, low-power, highly-integrated transceivers.

Many companies struggle with designing the analogue, microwave interfaces before and after the RF ADCs and DACs respectively. Broadband impedance matching, passive or active, single-ended or differential circuitry before and after the mixed-signal convertors, as well as RF simulation and synthesis, are key challenges for today's digital-centric engineers.

Introduction

RFSoC integrates RF ADCs and DACs with a 16 nm, Zynq UltraScale+ MPSoC capable of implementing a complete software-defined radio including direct IF/RF sampling at the receiver and direct IF/RF re-construction at the transmitter.

Xilinx offers five RFSoC parts with different mixed-signal options based on the selected device. Multiple 12-bit, 4 GHz ADCs are available capable of sampling up to 2.058 or 4 GSPS allowing direct digitisation of IF/RF carriers within this input bandwidth. The ADCs can be configured for real data or paired for I/Q operation.

After each ADC, there is a decimation filter to reduce the output data rate and digital down-conversion (DDC), realised using an NCO and a digital mixer, to allow for a specific bandwidth of frequencies to be selected and moved to baseband for processing. Before each ADC, an external, analog anti-aliasing filter will be required to remove out-of-band interference and noise to prevent this corrupting the digitised carrier information.

Multiple 14-bit, 4 GHz DACs are available capable of sampling up to 6.554 GSPS allowing reconstruction of IF/RF carriers and direct up-conversion to the second Nyquist zone within this output bandwidth. The DACs can also be configured for real data or paired for I/Q operation.

Traditional DACs have a zero-order hold time-domain response which fixes the analog output between successive sampling instants as shown below. This results in amplitude roll-off in the higher Nyquist zones, zero nulls at integer multiples of the sampling frequency and a reduction in the output power of 3.92 dB at the Nyquist frequency (Fs/2). RFSoC's DACs contain an inverse sinc filter to provide a flat response over the output bandwidth of interest and gain, phase and offset correction are also provided for I/Q modulation.

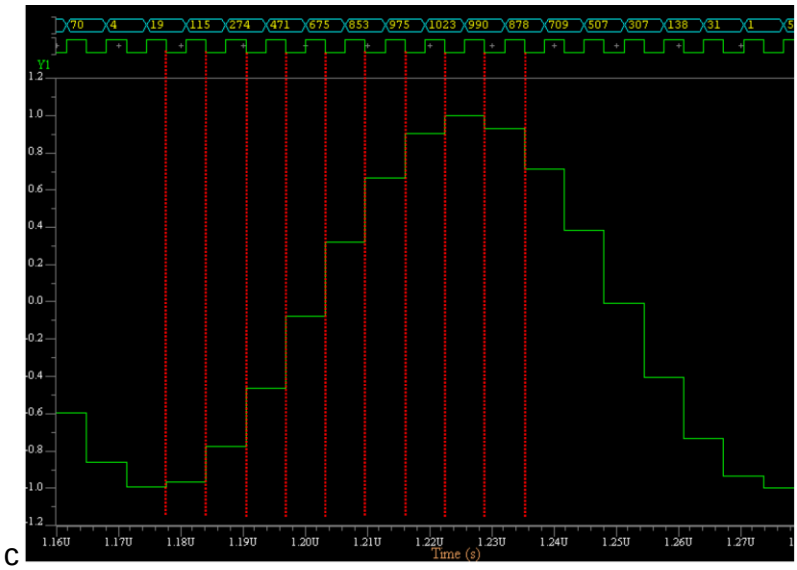

Figure 1 : Zero-Order Hold, Time-Domain Analog Output. [Source Spacechips]

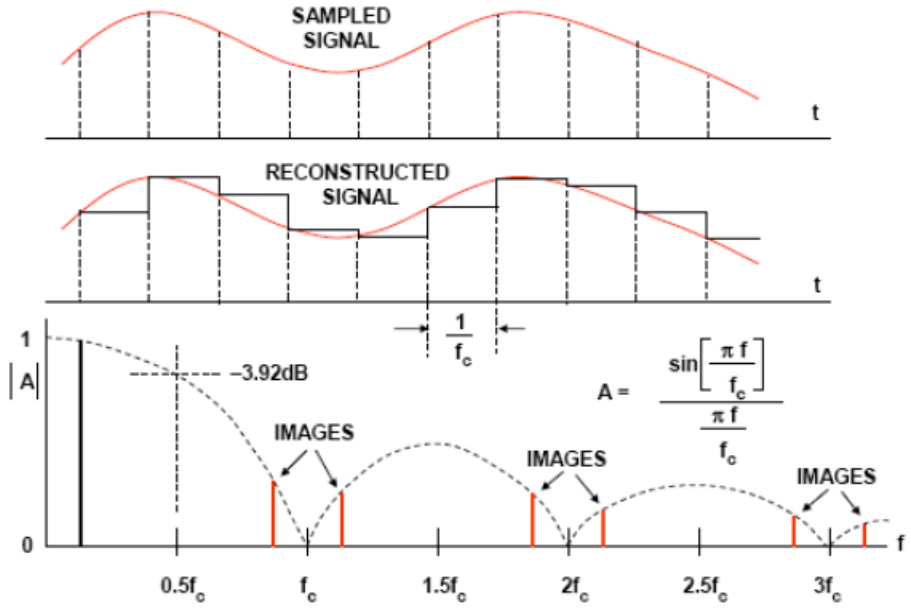

Figure 2 : Sinc Roll-Off in the Frequency Domain [Source ADI]

Before each DAC, there is an interpolation filter to increase its effective input data rate as oversampling reduces the impact of sinc roll-off within the bandwidth of interest and moves the images and nulls higher in frequency. Digital up-conversion (DUC), realised using an NCO and a digital mixer, allows for a specific bandwidth of baseband frequencies to be selected and up-converted to IF/RF. After each DAC, an external, analog anti-imaging filter will be required to remove out-of-band interference and noise to prevent this corrupting the re-constructed carrier information.

Figure 3 illustrates the main blocks of RFSoC highlighting the multiple mixed-signal tiles.

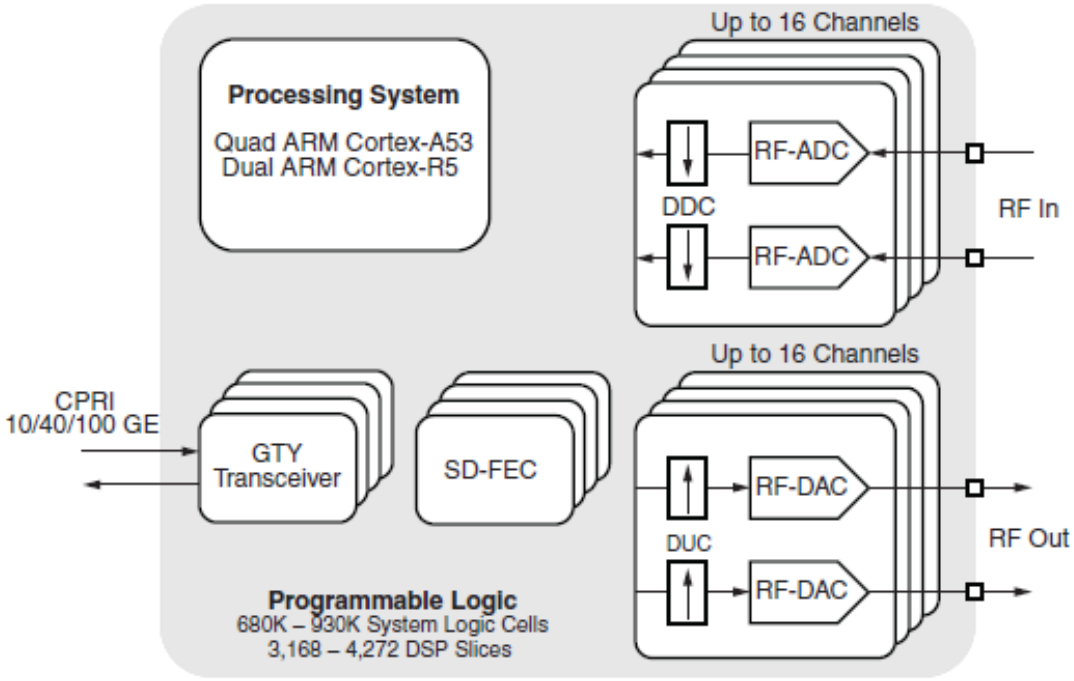

Figure 3 : Zynq UltraScale+ RFSoC. [Source Xilinx]

RFSoC also contains multiple soft-decision, forward error correction (SD-FEC) engines for decoding and encoding data to control errors in data transmission over unreliable or noisy communication channels. The SD-FEC block supports low-density parity checks (LDPC) and Turbo decode for 5G, backhaul, DOCSIS and LTE applications.

The table below lists the five RFSoC parts summarising the mixed-signal and SD-FEC options:

	XCZU21DR	XCZU25DR	XCZU27DR	XCZU28DR	XCZU29DR
12-bit, 4GSPS RF-ADC w/ DDC	0	8	8	8	0
12-bit, 2.058GSPS RF-ADC w/ DDC	0	0	0	0	16
14-bit, 6.554GSPS RF-DAC w/ DUC	0	8	8	8	16
SD-FEC	8	0	0	8	0

Table 1 : RFSoC Mixed-Signal and SD-FEC Feature Summary. [Source Xilinx]

Dr. Rajan Bedi is the CEO and founder of Spacechips, a UK SME which builds and sells advanced on-board processing and transponder products for satellites and spacecraft. The company also offers Design-Consultancy in Space Electronics, Technical-Marketing, Business-Intelligence and Training services to the global satellite industry, having delivered over 120 projects to 70 clients in 23 countries.

Spacechips won ***New Company of the Year 2017*** *and* ***High-Reliability Product of 2016, 2017*** *and* ***2018****. Spacechips is currently designing-in Xilinx FPGAs for space and ground-segment applications, and teaches courses on Mixed-Signal and FPGAs, comparing parts from all suppliers allowing OEMs to make independent and informed technology selections. Please email, info@spacechips.co.uk, to discuss your requirements!*