MEASUREMENT AND OPTIMIZATION OF FREQUENCY MULTIPLIERS USING AN AUTOMATED TEST BENCH

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***Abstract*-This paper describes the measurement and optimization of Schottky varactor frequency multipliers at 80 and 160 GHz. An automated frequency multiplier test bench was implemented using the National Instruments LabVIEW program. The test bench is fully automated with a frequency synthesizer, power meters and bias supplies all controlled using the common SCPI commands via a GPIB interface. This system has been implemented and tested on a range of frequency multipliers with the aim of enabling greater understanding of the performance of these devices than would be possible using manually controlled measurements. The system is being used as a tool to experimentally validate a thermal model for waveguide based frequency multipliers. Initial thermal simulation results will also be presented.**

Index terms - Schottky varactor frequency multiplier, thermal model, waveguide based frequency multipliers.

I. INTRODUCTION

Extensive research taking place in the terahertz region (0.1-1 THz) has made the use of Schottky varactors quite important [1, 2]. Schottky varactor frequency multipliers have been successfully used as signal sources e.g. local oscillators in receivers for space-borne radio astronomy and atmospheric remote sensing [3]. Advances in this technology have seen their use extended to security imaging [4, 5], medicine [4] and Non- Destructive Test (NDT) [5]. Over the years, frequency multiplier technology using Schottky diodes has advanced from whisker Schottky contacts [6] through discrete diodes with planar air bridges [7, 8] to integrated membrane structures for high frequency applications [9]. Much of the improvement in frequency multiplier performance pertains to enhancing the Schottky diode parameters such as series resistance, junction capacitance, and breakdown voltage as well as improving thermal management of the device [10, 11]. In order to understand how these parameters affect performance, detailed characterization of devices is necessary. Greater understanding of these devices can also be gained by characterizing multiplier circuits; it is common that the performance of a single device is presented in papers, and by measuring with sufficient resolution to detect standing waves due to port mismatch. Manual measurement of frequency multipliers to include large number of data sets can be a tedious experiment even to a skilled professional. Not forgetting the time consumed in measuring a number of these devices.

This paper describes an automated test bench setup for measuring frequency multipliers. This simplified approach of automated measurements is a quick, accurate and efficient way in interpreting device performance. The following system has been implemented and tested to facilitate a greater understanding of frequency multipliers. The test bench illustrated in Section II is a fully automated setup using LabVIEW instrument control from National Instruments. Parts of the LabVIEW code are explained in this section to provide an appreciation of the automated setup. Section III shows some initial work on the thermal optimization of frequency multipliers using a thermal solver. This will follow with a discussion of the measured results obtained from the automated test bench in Section IV. A brief conclusion summarizing the important of these measurements is presented in Section V.

II. AUTOMATED TEST BENCH

A. Test Setup:

The following section describes the test bench setup for measuring frequency multipliers. Fig.1 shows a frequency synthesizer driving a preamplifier/active multiplier whose output is coupled from the first coupler and measured using an Agilent N19112A power meter [12] for power reference doing multiplier measurement.

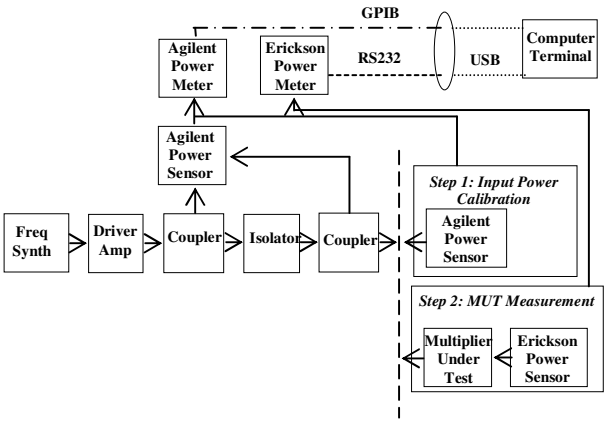


Fig.1: Block diagram showing automated test setup.

The second coupler is used for measuring the reflected power to calculate the input return loss of the multiplier. The first step in calibration is calculating the coupling ratio using the coupled port of the first coupler and the output port of the second. This ratio is used to set the required input powers to the frequency multiplier. Next the couplers are calibrated to measure the reflected power under total reflection. Finally, during multiplier measurement the correct coupled power is set on the first coupler using the ratio calculated during calibration. The isolator prevents any power being reflected from the second coupler to the first so that the ratio is unchanged. The output power from the multiplier is measured using a PM4, Erickson power meter from Virginia Diodes [13]. All the instruments except the PM4 are controlled using Standard Commands for Programmable Instruments (SCPI) using a General Purpose Interface Bus (GPIB) interface. The PM4 is controlled using a RS-232 standard for serial communication.

B. Automated System:

The LabVIEW program is a visual programming language from National Instruments [14]. The front panel in Labview has a user interface while the program is written in the backend called the block diagram. The program is written in parts called sub-VI's (Virtual Instrument) and later merged into one complete VI. The following sections will illustrate how the individual VI's work.

- Effective Input Power Control:

In order to set the correct power levels into the multiplier the program had to be iterative since the relation between synthesizer and preamplifier/active multiplier is non-linear. To achieve this, the synthesizer power is varied until the correct power is set. This is done using a PID (proportional-integral-derivative) function which measures the error between the current power and the desired power. The function then feeds back these errors into the input in an attempt to reduce the error. A loop is incorporated to set the synthesizer power and measure the power split from the coupler. This data is fed into the PID function and the feedback is translated into a form which can be used to change the synthesizer settings. Fig.2 shows the block diagram for controlling synthesizer power using a PID controller.

- Coupler Calibration:

Input calibration is divided into two parts. The first part consists of setting correct input powers to the multiplier by calculating the coupling ratio. In the second part, reflected power under maximum reflection is measured. The block diagram shown in Fig.2 is used to set a fixed power at the output of the second coupler (input to the multiplier). Then a ratio is calculated by taking the difference between output power from second coupler and coupled power from first coupler at each frequency in dB. The program then loops through the range of frequencies and saves the calibration data into a spreadsheet which can then be used by the main program.

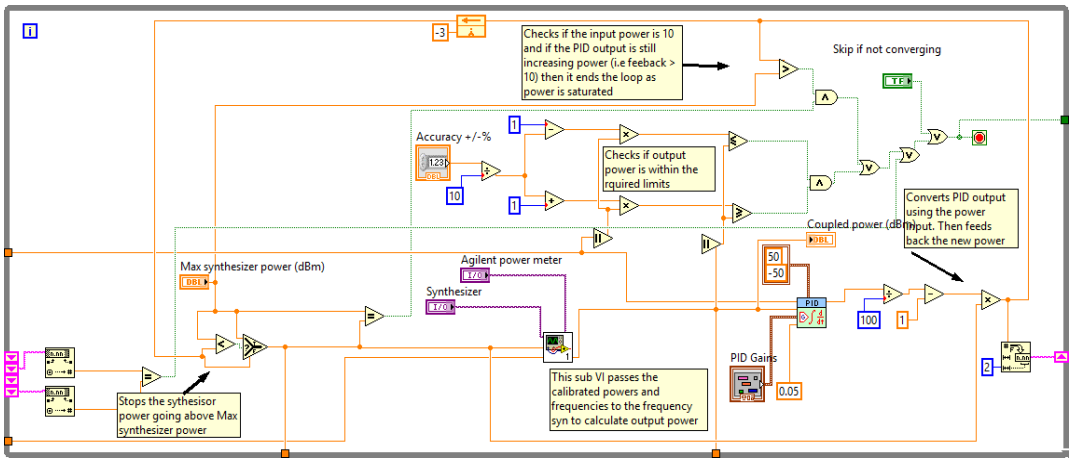


Fig.2: Sub-VI showing input power control using PID controller.

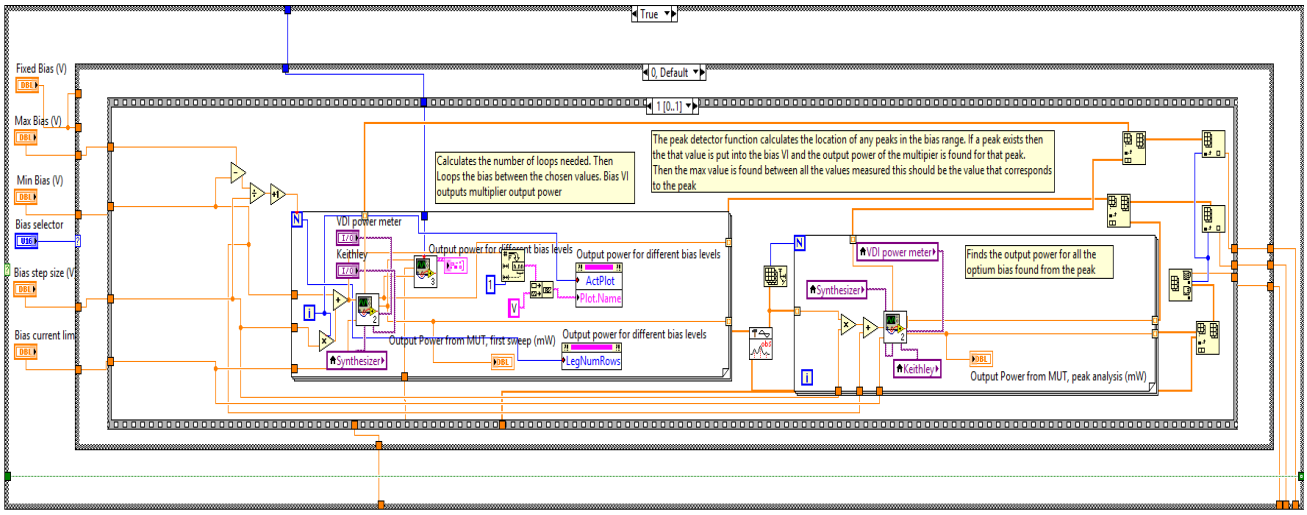


Fig.3: Sub-VI showing frequency multiplier bias optimization.

In the same way the reflected power is calculated for all sets of frequency points by setting the required input powers to the multiplier and recording the reflected power on the second coupler from a perfect short load. Now when the multiplier is measured, the coupled power at the second coupler will indicate the reflection from the multiplier. On subtracting the value of reflection during calibration from this value, the input return loss of the multiplier is obtained.

- Optimizing Multiplier Bias:

For multiplier measurements the same power control program used during calibration is used for setting appropriate input powers to the multiplier using the coupler ratios. Now that the system controls the input power into the multiplier, a program was required to obtain the optimum bias and measure the output power. The bias optimization is done in two parts using a Keithley 2604A Source Measure Unit (SMU) [15]. The bias program is shown in Fig.3. The program starts by measuring the output power across a range of bias levels and enters this data

into an array. The data is then entered in a peak function which returns a peak value. On interpolating this peak, a maximum value is obtained which is logged into the initial array and checked again to find a maximum from among all the points. On finding such a value, the maximum output power is entered into a spreadsheet along with its efficiency, optimum bias and current at this bias.

IV. THERMAL OPTIMIZATION OF FREQUENCY MULTIPLIERS

Thermal optimization of multipliers was performed using a 3D thermal solver from CST Multiphysics Studio [16]. For the simulations all surfaces of the waveguide block except the input channel area are assumed to have an isothermal boundary i.e. temperature remains constant. An adiabatic boundary is selected for the channel area. A heat source is applied directly below each anode area to indicate the amount of power dissipated by the respective anode. At the far end of the filter a metal surface is attached to resemble the actual waveguide block into which the filter is fixed in place with epoxy. A steady state thermal simulation is performed on this structure.

A discrete diode with 6 anodes, used in the 80 GHz frequency doubler, is examined in the following discussion. The diode is fabricated on a conventional Gallium Arsenide (GaAs) substrate with 50 µm thickness. The discrete diode is mounted on the filter using an indium based solder in a flip-chip configuration. The diode is connected to the waveguide block using bondwires. Fig.4 illustrates a 6 anode flip-chip Schottky diode mounted on an Aluminum Nitride (AlN) filter. The top view of the discrete diode is shown in Fig.5.

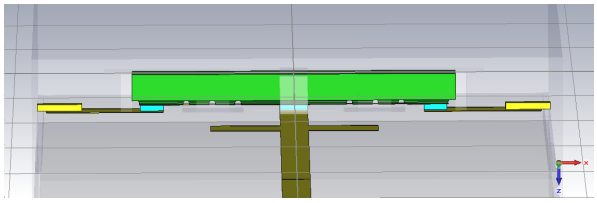


Fig.4: Flip-chip 6 anode discrete Schottky diode mounted on an AIN filter.

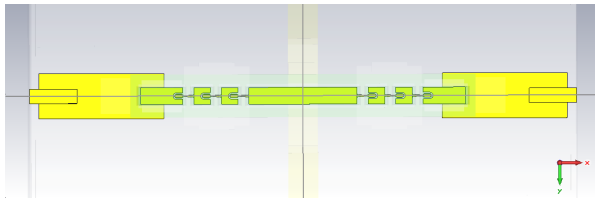
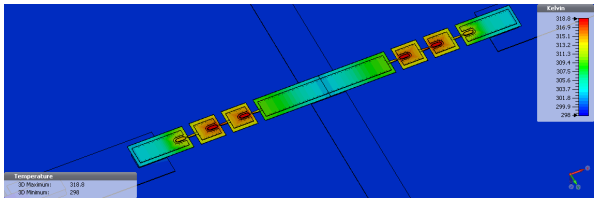


Fig.5: Top view of 6 anode discrete Schottky diode.

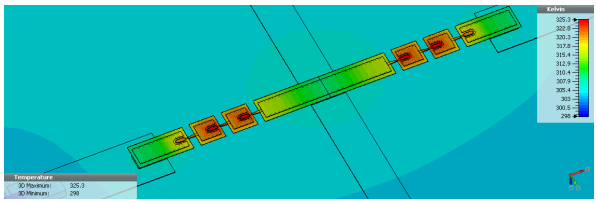
Heat generated in the diode conducts through the GaAs substrate, waveguide block via the bondwire and the filter. Initial examination shows that the filter substrate has a profound effect on the heat dissipation. To highlight this effect the diode structure shown in Fig.4 is simulated with three different substrates. Thermal conductivity along with simulated maximum anode temperature is given in Table 1. Owing to the high thermal conductivity of diamond, more heat is conducted by the waveguide block due to lower thermal resistance. The use of diamond in these circuits is not common due to higher material and processing cost. On the other hand, AlN with its modest thermal conductivity performs better than quartz. However, electrically quartz is less lossy than AlN. Seen in Fig.6 a, b, c is the heat distribution on the diode. The power dissipated in each anode from measurements is estimated to be 12.5 mW for an input calibration power of 100 mW. Blue colour on the temperature bar indicates room temperature while red shows maximum temperature.

Filter substrate	Thermal conductivity (W/m/K)	Maximum anode temperature (K)
Pure Diamond	~1000	300.8
Aluminium Nitride	~200	325.3
Fused Quartz	~1.3	390.8

Table1. Thermal conductivity and corresponding maximum anode temperatures for various substrate materials.



(a)



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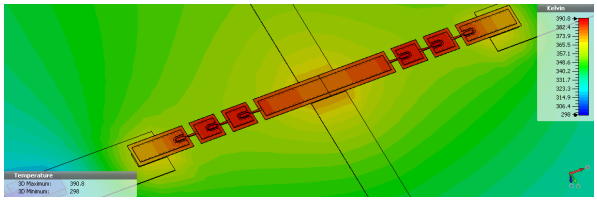


(c)

Fig.6: Heat distribution for different filter substrates (a) Diamond (b) AlN (c) Quartz.

To verify if there is any change in efficiency of the doubler circuit without having to undertake a completely new design and assembly, it was decided to apply epoxy at the sides of the GaAs substrate. EPO-TEK H20E, a high thermal conductive silver filled epoxy from Epoxy Technology was used since this was the only available option with reasonable thermal conductivity of 29 W/m/K. Fig.7 shows the location on the diode where the epoxy was applied. The automated test bench results for the 80 GHz frequency multiplier before and after using epoxy is shown in Fig.8 a, b. Fig.8 a shows a power sweep of the corrected efficiency versus the dissipated power. The correction is applied by using the input return loss data. A comparison of the return loss data for both the cases is given in Fig.8 b. Before applying the epoxy, the efficiency starts to reduce as the dissipated power goes above 50 mW but after using epoxy this power continues to increase beyond 50 mW. However, the absolute efficiency after using epoxy has dropped considerably. This drop could be due to the electrical detuning of the circuit due to H20E which is an electrically conducting epoxy. Further test using an electrically insulating and thermally conducting epoxy are being planned.

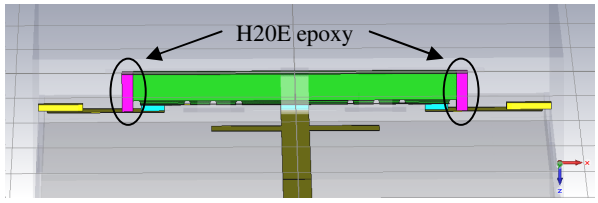
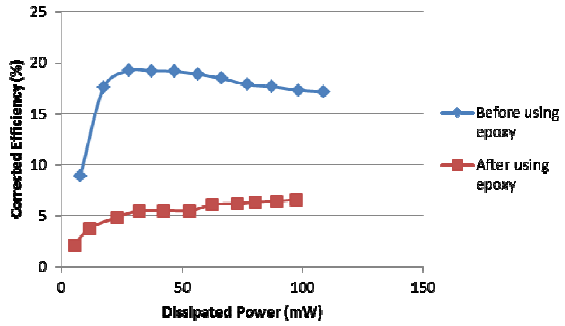
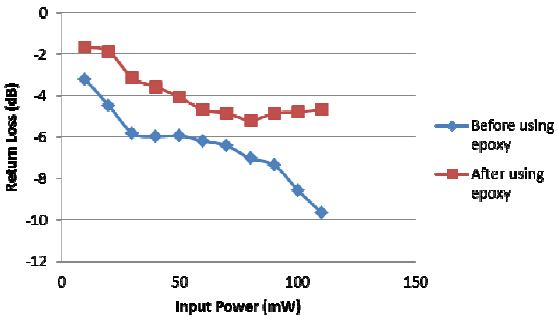


Fig.7: Epoxy location on the diode structure.



(a)



(b)

Fig.8: Measured results using automated system before and after using epoxy (a) Corrected efficiency (b) Input return loss.

IV. TEST BENCH RESULTS AND DISCUSSION

Design of the frequency multipliers were carried out with HFSS, a 3D electromagnetic simulator from Ansys [17] while the linear and non-linear analysis was untaken by the ADS software from Keysight (formerly Agilent) [18]. The results shown in the following section include simulated

and measured output power, efficiency and input return loss data for frequency doublers at 80 and 160 GHz.

A. 80 GHz doubler:

The program allows the user to fix one or more parameters; input calibration power, frequency or bias point. A frequency sweep for output power and input return loss was generated at a fixed input power of 100 mW. The bias level was allowed to vary between -14 and -2 V. Fig.9 and Fig.10 show a comparison between the manual and the automated test bench data for a 80 GHz doubler. As indicated by the results there is a good agreement between the manual and automated measurments. By measuring the input return loss the actual power going into the muliplier can be calculated. This gives an indication of the power dissipated in the anodes.

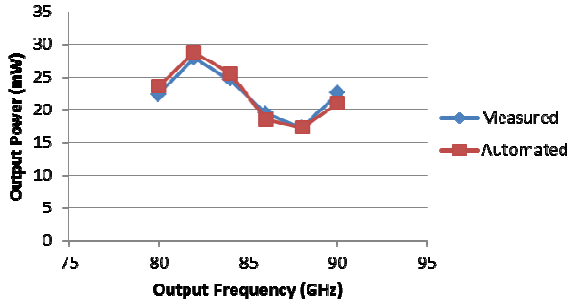


Fig.9: Output power for the 80 GHz doubler with a fixed input power of 100 mW.

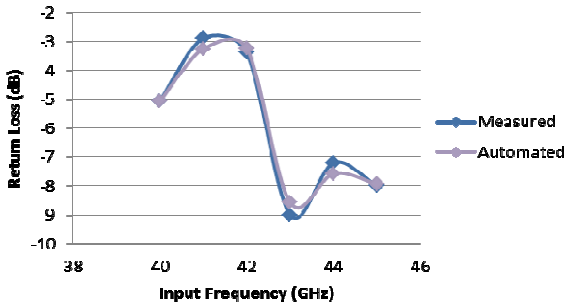


Fig.10: Input return loss for the 80 GHz doubler with a fixed input power of 100 mW.

Considering that the setup requires two couplers and an isolator, this could be a limitation to the maximum input calibration. However, this was necessary for accurate calibraton of higher input powers. Hence the number of calibration points depends on the maximum available source power. Fig.11 shows the measured efficiency plotted against a frequency sweep for different input powers. This can be compared with the simulated result presented in Fig.12. The measured 80 GHz peak has shifted to 82 GHz when compared to the simulation. The measured results show an improvement in output power which indicates a change in the junction capacitance and series resistance from the assumed values during simulation. This increase could also be due to the optimization of bias level during measurement. The simulated results are plotted for a fixed bias.

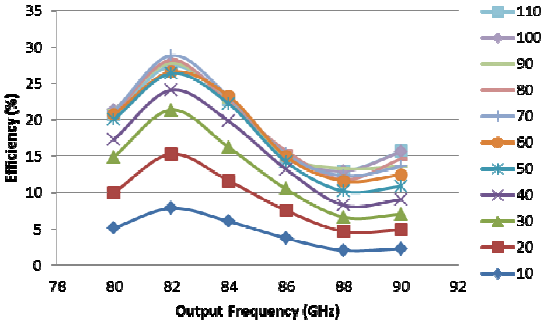


Fig.11: Measured efficiency for the 80 GHz doubler at different input powers.

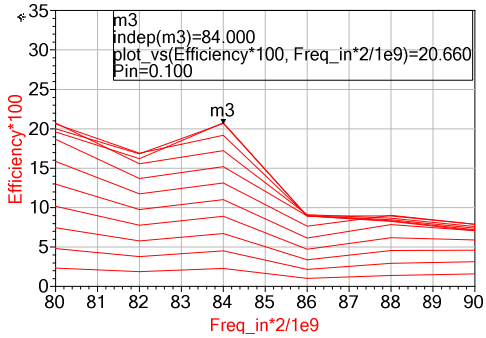


Fig.12: Simulated efficiency for the 80 GHz doubler at different input powers.

B. 160 GHz doubler:

A 160 GHz frequency doubler was measured with an input power of 100 mW. The output power and input return loss for this device is presented in Fig.13 and Fig.14 respectively. The bias level was set to vary between -12 and -4 V.

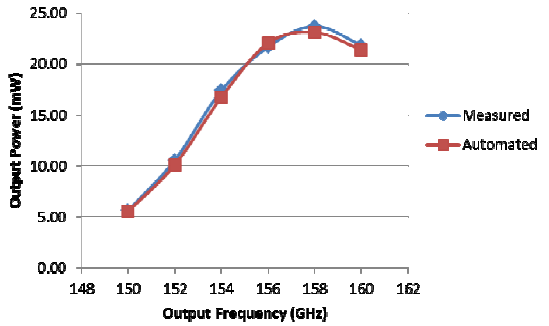


Fig.13: Output power for the 160 GHz doubler with a fixed input power of 100 mW.

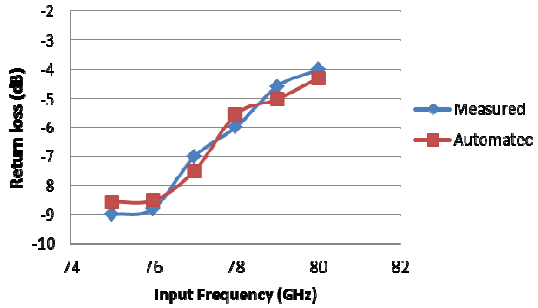


Fig.14: Input return loss for the 160 GHz doubler with a fixed input power of 100 mW.

The measured and simulated results for the 160 GHz frequency doubler are shown in Fig.15 and Fig.16 respectively. The measured result has its peak centered at 158 GHz rather than 160 GHz as indicated by the simulation. This variation again can be due the shift in the parameters assumed during simulations or even alignment errors during assembly. The measured results indicate a good resemblence to the simulated results, however, with a lower efficiency.

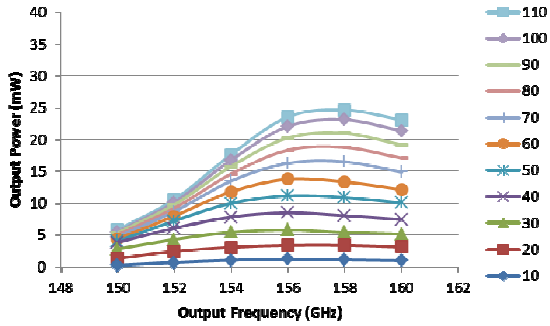


Fig.15: Measured output power for the 160 GHz doubler at different input powers.

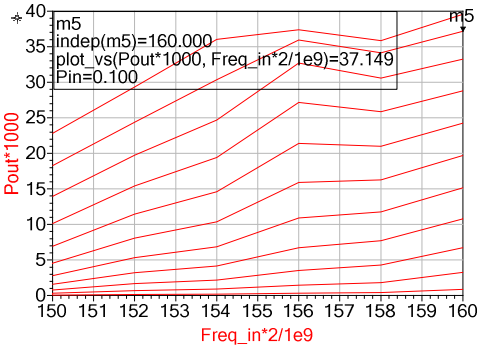


Fig.16: Simulated output power for the 160 GHz doubler at different input powers.

V. CONCLUSION

The work presented here demonstrates a close correlatation between measured and simulated electrical performance for doubler circuits. In addition thermal analysis has been demonstrated to estimate diode anode (channel) temperatures for various dissipated power levels. Finally, a robust and comprehensive automated measurement system has been demonstrated which can rapidly characterise components over a wide range of conditions. Further work will focus on the measurement of different component types, and the correlation of these measurements with simulations to refine varactor diode and circuit models for more accurate component modelling – including over different temperature ranges.

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