# High Efficiency Class E MMIC Oscillator for X-band Medical Applications - Part A

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***Abstract*— This paper presents high efficiency class E oscillator for X-band and Ku-band surgical devices for the treatment of various medical conditions that include: tumours, gastro oesophageal reflux disorder, and spider veins. The MMIC oscillator has been developed using 4x150 µm GaAs pHEMT transistor from the WIN PP10-15 foundry process with the design, EM simulations and layout being performed using Keysight's Advanced Design System (ADS). EM simulated results show 24.3 dBm output power with 48 % peak efficiency at 14.5 GHz under optimal bias conditions, while initial on-wafer measurements show clean oscillations on the spectrum analyser with a peak of up to 20.4 dBm output power at 10.7 GHz under reduced bias conditions. Further measurements are ongoing and will be published at a later stage.**

***Index terms*— GaAs pHEMT, Electrosurgery, High Efficiency Oscillators, Class E AmplifierMicrowave, MMIC.**

## I. INTRODUCTION

RF and microwave devices have effectively found applications in the field of medicine and electrosurgery due to the non-ionizing nature of RF and microwave energy. Microwave power sources and amplifiers can be combined with suitably designed antenna and applicator structures to produce highly focused and controlled heating on tissue structures; while minimizing distributed tissue heating and its effect on neighboring tissues [1]. This is called Microwave Ablation. Electrosurgical devices operating at C-band and X-band frequencies have been reported in [2] for applications including treatment of benign and cancerous lesions, reshaping the cornea, male sterilization, and the treatment of menorrhagia.

Oscillators are essential elements of a microwave system with applications in communications, radars, instrumentation and RF and microwave surgical and therapeutic devices. Solid state oscillators are nonlinear circuits that convert DC to steady state RF sinusoidal signal by utilising an active nonlinear transistor or diode devices alongside passive circuit elements. Ideal oscillator circuits generate pure RF or microwave sinusoidal signal with fixed frequency, phase and amplitude. However, practical implementation of oscillators generally involves frequency and output power variance with time, which is an important design aspect. Early development of oscillator circuits was performed using Gunn and IMPATT diodes, which showed decent performance in terms of higher frequency and output power; however, transistor oscillators provide several advantages that include: higher compatibility with other elements in the microwave system, suitability for monolithic microwave circuit integration, low phase noise, independence from threshold current requirements and higher power efficiency performance; making the latter a popular choice for microwave systems [3]. Robertson (2001) in [4] discusses the suitability and low phase noise performance of HBT and HEMT based microwave oscillators in MMIC technology. A popular design choice is quasi MMIC circuits that simplify the fabrication process, improve reliability and noise performance, by having a negative resistance (or reflection) amplifier on a single chip along-with the corresponding bias and decoupling circuit elements, and off chip high quality factor resonators.

The reported efficiency of oscillator circuits is fairly low and much of the power is dissipated as heat during DC to RF conversion. Switching mode oscillators have been discussed in the literature to improve efficiency of oscillator circuits. These include class E or class F amplifier topology and a feedback network that provides the required phase shift and the conditions of oscillation. Ebert et al. (1981) in [5] presented initial theoretical concepts of the optimal conditions of oscillations for class E tuned power oscillators. Tsang et al. (1994) in [6] utilized large signal s-parameter design techniques to demonstrate high power class E oscillator at 900 MHz to provide 27.56 dBm output power with 57.54 % collector efficiency. However, more recent developments in switching mode oscillators include: C-band class E MMIC oscillator designed on standard 0.6 µm Triquint TQRXs MESFET GaAs process, where the variation of supply voltage demonstrated efficiency of up to 43 % with 6.5 dBm output power at 4.4 GHz with 1.8 V supply voltage [7]. Chang et al. (2017) in [8] presented K band class E high efficiency oscillator which was developed on 0.15 µm GaAs pHEMT process from WIN semiconductor foundry. The oscillator demonstrates 19 % peak efficiency with 21 dBm maximum output power from 23.5 to 24.5 GHz.

Presented herein is a high efficiency class E oscillator that has been developed using WINPP10-15 process from WIN semiconductor foundry, which is a 100 nm gate length InGaAs pHEMT process with substrate thickness of 4 mil. The design and EM simulations have been carried out using the foundry's process design kit in Keysight's ADS and Momentum Microwave, respectively. EM simulations of the oscillator show 24.3 dBm output power with 48 % peak efficiency at 14.5 GHz under deep class AB bias conditions. Initial on-wafer measurements at reduced drain current bias conditions were performed; clean oscillations on the spectrum analyser with up to 20.4 dBm peak output power, while, stable oscillations with 16.4 dBm output power at 10.7 GHz were

observed. Further measurements are ongoing and will be published at a later stage.

This paper is organized as follows. Section II presents the design flow of switching mode oscillators while introducing composition of the circuit. Section III presents the design of class E amplifier and includes: discussion about optimum bias conditions, load pull to ascertain optimum load termination network, input matching network, comparison of voltage and current waveforms at various input power drive levels, and large signal simulations incorporating EM simulated networks, to achieve over 20 dBm output power with high efficiency at the design frequency. Section IV presents the design of feedback network to provide the necessary startup conditions of oscillation, and the final layout of class E oscillator. Finally, section V presents initial on-wafer measurements of the oscillator MMIC.

## II. SWITCHING MODE OSCILLATOR DESIGN FLOW

Fig. 1 Shows a generalized class E oscillator structure which includes large transistor device in common source configuration with a shunt capacitance ($C$ ) to the drain terminal, conjugately matched input network, load termination network that includes an LC tank at the fundamental frequency and an output transmission line, and the feedback network. Bias networks may include RF choke or quarter-wavelength transmission lines and decoupling capacitors. The voltages and currents ($V_{in}$, $V_{out}$, $I_{in}$ and $I_{out}$) at the two reference planes (A and B) in class E oscillator structure are utilized to design the feedback network.

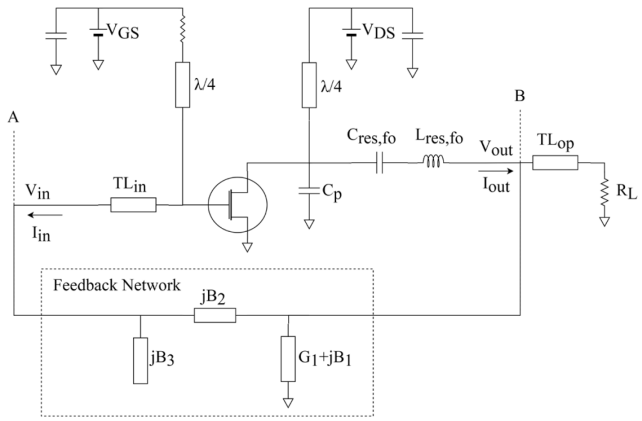


Fig. 1: Structure of class E switching mode oscillator

The first step involves careful selection of deep class AB bias conditions, followed by the selection of optimum load impedance at the fundamental frequency (also the frequency of oscillation) through load pull analysis, and conjugately matched source impedance to provide maximum power transfer to the transistor. Once the amplifier has been optimised for high power and PAE through large signal simulations based on EM simulated networks and circuit elements; voltages and currents at the amplifier's input and output reference planes are obtained. These are then used to design the feedback network required to provide start-up conditions for the oscillations. In the third step, transient analysis is performed, and the oscillator is optimised at the design frequency for the required power and efficiency. These design steps will be discussed in detail in subsequent sections of this paper.

## III. CLASS E AMPLIFIER DESIGN

The theory of class E switching mode amplifiers was first presented by Sokal (1975) in [9], while the underlying design equations were derived by Raab (1977) in [10]. The behavior of transistor in class E mode is considered as a switch with a shunt capacitance to the drain terminal that does not act as a parasitic, nor as a harmonic short circuit. This way, current flows through the transistor (switch) during the 'on-state', and through the shunt capacitor during the 'off-state'. Integration of the voltage waveform starts from 0, which is the point when the switch opens, and the current is transferred from the switch to the shunt capacitor. The voltage waveform crosses the zero point again when the switch closes, and the current is transferred to the switch. This way, current and voltage waveforms do not overlap each other and a theoretical DC to RF efficiency of 100 % can be justified. Grebennikov (2004) in [11] presents various parallel load network configurations for class E amplifiers having a shunt capacitance ($C_p$), and RLC load termination network where $C_p$, $L$ and $C$ are tuned at the fundamental frequency, while the resistor $R$ is required to perform voltage and current waveform shaping. Such a network has been shown in Fig. 2 [12].

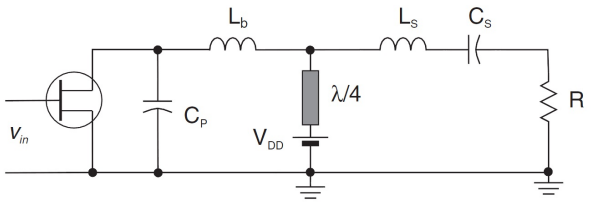


Fig. 2: Topology for generalized class E amplifier with quarter wavelength transmission line in the biasing network

However, operation of the transistor as an ideal switch cannot be extended to high frequency operation in microwave frequencies where non-linear output capacitance of the transistor provides short circuit conditions to higher order voltage components and the transistor cannot be explained as an ideal switch. The current waveform at high frequencies remains unchanged and the voltage waveform is engineered through the load network [12].

### *A. Optimum Bias Conditions and Class E Load Network*

The WIN PP10 process provides $F_t$ greater than 135 GHz and $F_{max}$ over 185 GHz, however, the maximum frequency of operation for class E amplifiers is defined in terms of the transistor's output capacitance, and the drain to source voltage. At the design frequency of 14.5 GHz, small output capacitance and large $I_{max}$ is required. However, the latter comes at the cost of higher device power consumption and reduced efficiency. A large transistor (4x150 µm) has been selected to operate in the saturation region (under deep class AB bias conditions) alongside a high enough input power level to reduce the turn-on ($R_{on}$) resistance. The drain to

source voltage is low (close to 0 V) when the transistor is turned on but increases with an increase in $R_{on}$. However, small value of $R_{on}$ alongside high value of load resistance at the fundamental frequency could be utilized to achieve high output power. Load pull simulations are performed to optimize fundamental load resistance to achieve both high power and efficiency. The load termination network of class E amplifiers is also required to provide high reactive impedance at harmonic frequency components with suppression to a low level compared to the fundamental frequency component. The peak voltage and current across the transistor (acting as a switch) should also comply with the device limitations.

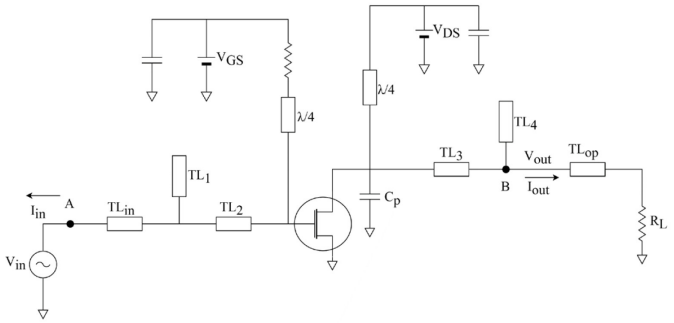


Fig. 3: Circuit schematics of class E amplifier

The input network plays an important role in enabling transistor's operation as a switch and helps to reduce the transition time between on and off states, where the conduction current flows through the transistor and the shunt capacitor ($C_p$), respectively. Ideal input drive waveform for class E amplifiers would thus be a square wave (like class F amplifiers). However, for cases where pure sinusoidal input waveform drives the transistor, maximum power must be transferred to the gate terminal which can be ensured through conjugate matching. Thus, for class E amplifier presented in this paper, conjugately matched input network has been implemented.

Load and source termination networks were designed and optimised using ideal lumped and distributed components to achieve the required class E mode voltage and current waveforms, output power and high efficiency. A shunt capacitance of 0.25 pF was added to the transistor's drain terminal, the value of which was determined through classical design equations reported in [12]. This capacitance alongside quarter wavelength drain bias line acts as a second harmonic blocking filter to suppress the second harmonic component which increases with an increase in the input power level. After optimization of the amplifier, the ideal lumped and distributed circuit elements were converted into microstrip components provided in the foundry's pdk. The amplifier was then optimised and EM simulations were performed down to DC. The lumped and distributed elements showed $Q$-factor greater than 20. The high value of quality factor leads to lower relative damping in the resonators; which is helpful to sustain oscillations when the amplifier is operating as a DC-RF oscillator with a feedback path. Fig. 3 shows the schematics of class E amplifier.

### *B. Class E Amplifier Voltage and Current Waveforms*

The voltage and current waveforms presented in this section explain some important behavioral aspects of class E amplifiers that include: the effect of overlapping current and voltage waveforms, increased switching transition time from on-state to off-state, the difference in on-state to off-state and off-state to on-state transition time, and the effect of on-resistance. These are some aspects that can justify reduced efficiency of the amplifier.

Fig. 4 shows current and voltage waveforms for EM simulated class E amplifier under deep class AB bias conditions for two input power drive levels, i.e. 17 dBm and 19 dBm across 1 dB compression point (occurs for $P_{in}$=17.6 dBm).

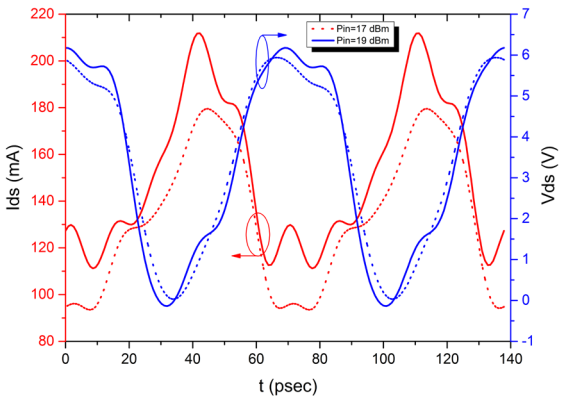


Fig. 4: Drain voltage and current waveforms for class E amplifier for $P_{in}$=17 dBm and 19 dBm

It can be observed from Fig. 4 that the voltage waveform at higher input power drive level ($P_{in}$ = 19 dBm) exhibits negative values which can potentially cause transistor failure. However, this may be prevented by restricting the input power levels where the voltage waveform doesn't show negative values, or by increasing the drain bias voltage. However, the latter comes at the cost of higher DC power consumption or reduced drain efficiency. Another way to prevent negative values is through the optimization of load network, while considering the shunt capacitance ($C_p$) to provide short circuit conditions to the current harmonic components. This discussion validates the role of fundamental load termination network towards voltage waveform shaping.

Time domain current and voltage waveforms shown in Fig. **5** are obtained at 1 dB compression level where the input power: $P_{in}$ = 17.6 dBm. These waveforms are similar to idealized waveforms presented in the literature with discrepancies in terms of overlapping regions between current and voltage waveforms where the transistor switches from on-state to the off-state and vice-versa. Ideally, the current is required to rapidly switch to zero when the voltage waveform is rising. Also, an important factor is the difference in transition time from on-state to off-state and from off-state to on-state. The figure shows that the latter transition time is greater than the former, which contributes towards reduced efficiency. The effect of $R_{on}$ can be observed through ripples in the knee region of the voltage waveform. These appear

during the cycle when the voltage waveform is in the knee region and the current waveform has a maximum, resulting in increased DC power consumption and reduced drain efficiency. Furthermore, the effect of $R_{on}$ (and non-zero knee voltage) increases with an increase in input power drive levels (or saturation) which can be observed by comparing the voltage waveforms for the three input power drive levels ($P_{in}$ = 17, 17.6 and 19 dBm) shown in Fig. 4 and Fig. 5.

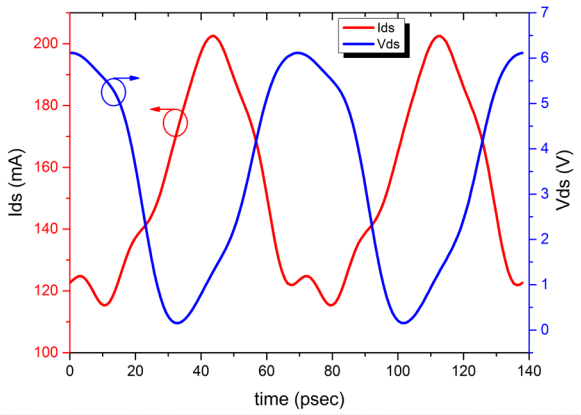


Fig. 5: Drain voltage and current waveforms of class E amplifier at 1 dB input power compression level of $\boldsymbol{P_{in}}$=17.6 dBm

## C. *Large Signal Simulations of Class E Amplifier*

This section presents large signal simulation results, analysis and behavioral performance of the amplifier.

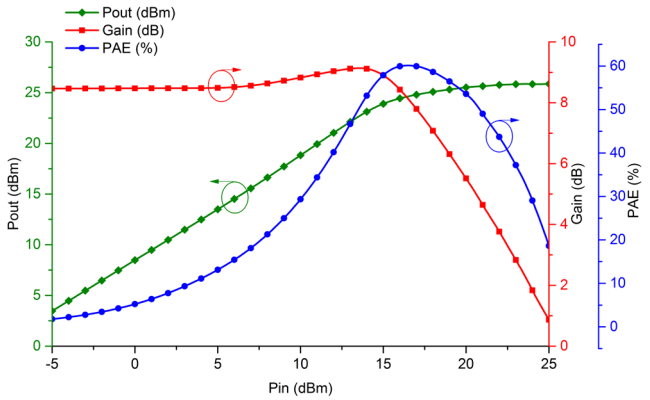


Fig. 6: Large signal simulation results of class E amplifier, the y-axes from left to right represent: output power ($\boldsymbol{P_{out}}$ in dBm), large signal gain (dB), and PAE (%), respectively.

Results presented in Fig. 6 indicate that the compression is achieved at lower input power levels and the corresponding output power level is low compared to other high efficiency amplifiers at 1 dB gain compression. However, the PAE achieves a peak just when the saturation region of the amplifier starts, which is an important characteristic of class E amplifiers. This way the amplifier isn't required to be driven into deep compression levels to achieve high PAE as with other high efficiency amplifiers like class F and inverse class F amplifiers. Decent large signal gain is also achieved. Large signal gain at 1 dB compression ($P_{in}$=17.6 dBm) is 7.38 dB with 24.98 dBm output power and 59.3 % PAE at the design frequency of 14.5 GHz. Another important effect is that of using a larger transistor (4x150 µm) alongside low $R_{on}$ and high fundamental load impedance, the effect of which can be observed with higher linear and large signal gain.

Fig. 7 shows the output spectrum of class E amplifier, where the output power at fundamental frequency component is 24.98 dBm and the effect of second harmonic component suppression (-26.45 dBc) due to transistor's output capacitance, quarter wavelength drain bias line and the shunt capacitor ($C_p$) can be observed. The second harmonic suppression level is acceptable for continuous wave operation, however, further optimization of second harmonic suppression could be performed with an improved estimation of the transistor's output capacitance.

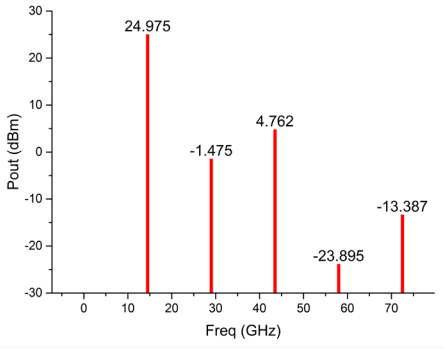


Fig. 7: EM simulated output spectrum of class E amplifier at 1 dB compression level

## IV. FEEDBACK NETWORK AND OSCILLATOR DESIGN

Feedback network for switching mode oscillators is synthesized at the fundamental frequency and can take either T or π network topologies, with both having their advantages which have been discussed in [13]. The feedback network shown in Fig. 1 is a π-network with three reactive and one resistive circuit elements, i.e. $jB_1, jB_2$ and $jB_3$, and $G_1$, respectively. Two port $Y$-parameters discussed by Jeon et al. (2006) in [14] have been given in Eq. 1, which can be solved to calculate the design values for reactive and resistive values of the feedback network. The terminal voltage and currents ($V_{in}$, $V_{out}$, $I_{in}$ and $I_{out}$) correspond to the ones shown at reference planes A and B in Fig. 1 and Fig. 2, which are obtained from the optimised class E amplifier discussed in the preceding section. It is important to mention that Eq. 1 is solvable only if the right hand side is not singular, i.e. the value of $V_{out} \neq 0$ and there exists a phase difference between $V_{in}$ *and* $V_{out}$ [13].

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \begin{bmatrix} j(B_2 + B_3) & -jB_2 \\ -jB_2 & G_1 + j(B_1 + B_2) \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} \quad (1)$$

Eq. 1 was solved using MATLAB to determine the values of: $B_1, B_2, B_3$, and $G_1$, which can be utilised to determine the appropriate reactive and resistive circuit elements. The feedback network includes a transmission line and spiral inductor, MIM capacitor and an open circuit stub to implement: $G_1$+$jB_1$, $jB_2$ and $jB_3$, respectively. After the design and optimization of feedback network, transient

analysis was performed to ascertain that the necessary conditions of oscillations were being generated to operate class E amplifier as an oscillator. Final layout of the oscillator was performed in ADS and all lumped and distributed circuit elements were simulated with EM momentum simulator down to DC. Fig. 8 shows the probed micrograph of class E oscillator.

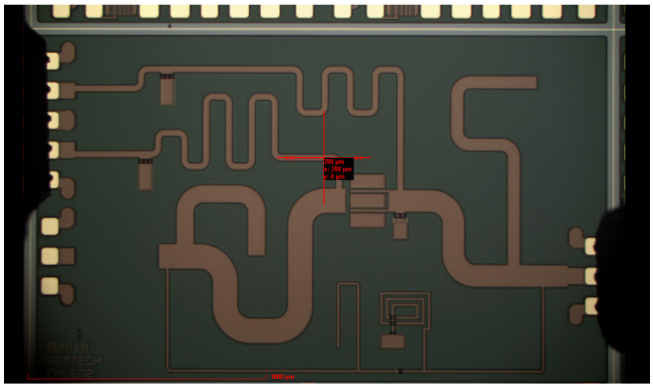

Fig. 8: Micrograph of probed class E oscillator

## V. INITIAL MEASUREMENTS

Initial on-wafer measurements of the oscillator were performed using Keysight's PNA-X N5247 network analyser with the drain and gate terminals biased through GSGSG 125 µm probes.

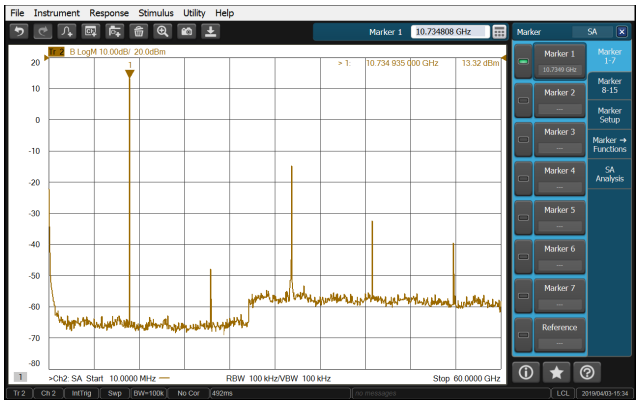


Fig. 9: Measured output spectrum of class E oscillator

The bias sequence involved pinch-off at -1.2 V DC at the gate terminal while the drain was biased at 2.0 V DC. Unstable oscillations were observed when the gate was opened to -0.9 V DC. A second set of measurements was performed at reduced bias conditions to maintain compliance with power handling capability of the bias-tees at $V_{DS}$ = 0.6 V and $V_{GS}$ = -0.78 V. Stable oscillations at 10.7 GHz were observed under this case, and the frequency shift occurred mainly due to different bias conditions. The oscillations touched a peak 20.4 dBm output power, however, they were stable at 16.4 dBm output power showing 27.9 % DC to RF efficiency. The measured output spectrum has been shown in Fig. 9. Further on-wafer measurements could not be performed due to limited power handling capability of the bias tees at the measurement facility. However, the circuit die will be packaged and mounted on a custom designed PCB evaluation board for further measurements and testing for the desired medical applications. This will be presented in an extended version of this paper at a later stage.

## VI. DISCUSSION

Future iterations of the oscillator circuit would include the conversion of lumped component π-network feedback path to a distributed network to provide the necessary conditions of oscillations. Also, the effect of output capacitance and the shunt capacitance on the suppression of second harmonic component, to achieve over -40 dBc suppression level, will be optimised.


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