Miniature Ceramic Thin Film Filters

Gavin A. Ripley Principal RF Engineer (BSC Filters ltd.)

Abstract

This presentation describes the design and manufacture of surface mount miniaturised filters offering performances up to 20GHz+. The process of "prototyping before manufacture" will be described, based on a realisation on high dielectric constant ceramic substrate using a 3D solver together utilising full characterisation of surface conductivity, substrate dielectric constant and carrier circuit board interactions. Manufacturing of these filters uses Industry standard MIC processing techniques which will be illustrated together with preproduction prototype parts and test data.

Introduction

The purpose of the programme described here was to create a design, modelling and fabrication protocol to produce thin film filters using standard MIC fabrication techniques. This is part of BSC Filters future road map of high level integration, agile and adaptive filtering. The end point is devices which can be used as standalone products for customers or to integrate as standard modules into our higher level assemblies. The added advantage is the reduction in size offered by high dielectric constant substrates and a European source of manufacture which avoids any ITAR issues. The small footprint and inherently robust structure of thin film ceramic filters mean they have a wide variety of applications from UAVs to space applications.

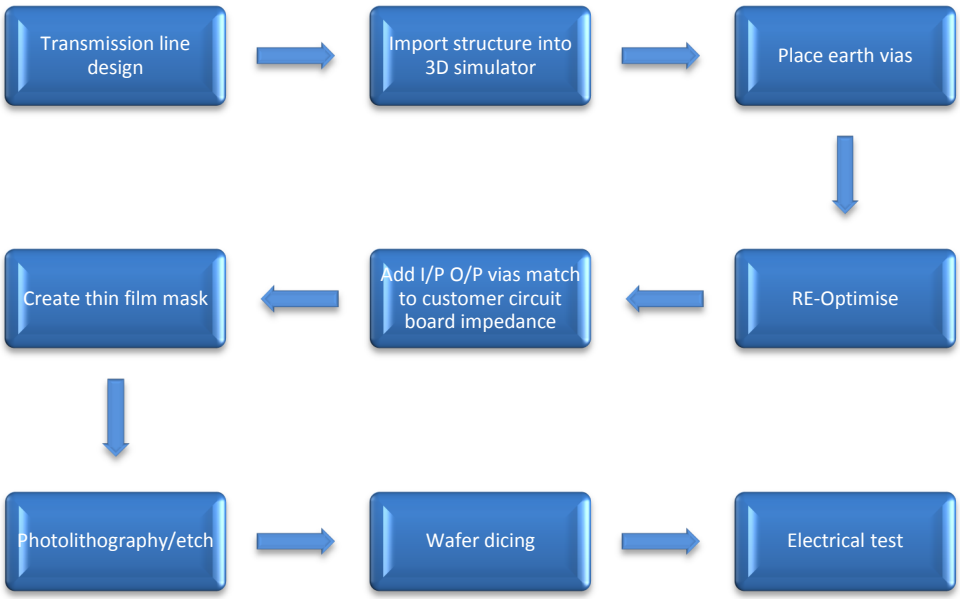

Figure 1 Process flow for thin film filter realisation

Process overview

The major stages in the thin film filter realisation are shown in figure.1. Three of the operations are subcontracted to a wafer fabrication house with the rest being in house BSC Filters design and testing activities.

Design

The initial aim was to use well understood filter topologies used in our current products and to develop a pathway from lumped element and transmission line modelling used for initial determination of the design to a full 3D structures capable of analysis in FEM simulation software.

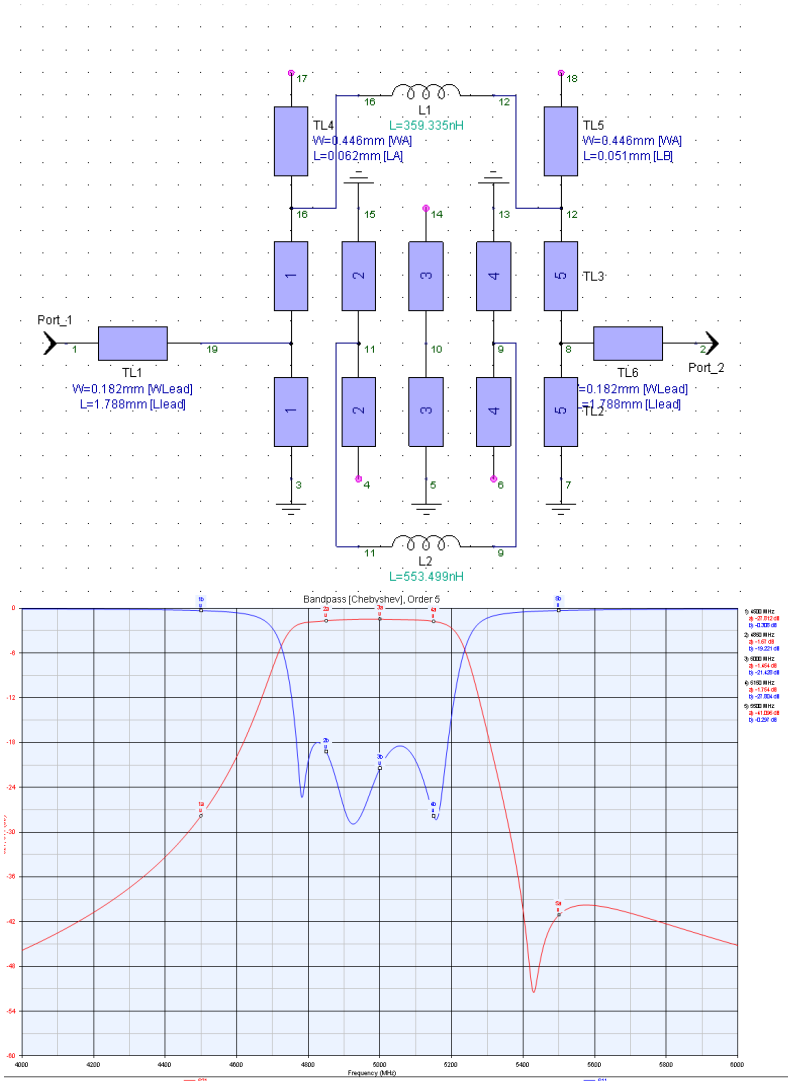

Figure 2 Preliminary model and predicted performance

In fact it was found a good first approximation to a design could be produced by modelling the structure in Genesys using the M–Filter synthesis approach. This required the creation of a model of the ceramic substrate and a set of simple design rules linked to the fabrication capabilities required in the thin film processing i.e. line width, spacing's and the surface conductivity of the deposited gold surface.

Figure 2 shows a typical circuit using an interdigital structure and the simulated response. The circuit requires additional inductors to be added to mimic the effects of none adjacent couplings (not included in the M-Filter transmission line model) which skew the filter skirts and create a notch on the high side of the filter.

This structure can then be transferred using a DXF 2D file directly into CST. Then using modelling techniques already developed for suspended substrate filter structures the 3D structure is built up in layers including air gaps where the lid and sidewalls are used in the final housing.

At this stage the discrete earth connections in the simple M-Filter model are replaced by models of the laser drilled plated via holes required to realise the connection to the back metalisation in the thin film structure. Some re-optimisation takes place at this stage as the via holes change the resonator frequency and so the length is adjusted. The lid height (and to a lesser extent the sidewalls) affects the resonator couplings so these are adjusted as well. For a simple design this work is carried out in the 3D CST environment. For more complex structures this is reimported into M-Filter as an s parameter file and adjustments made on the original model. Reloading the file back into the CST environment allows you to check the adjustments until the design is fully optimised.

Once the model is working the final stage is to add the edge vias directly connecting the thin film structure to the supporting circuit boards. For a wire bonded structure a simple pad could be added but for the soldered approach the edge metalisation is formed by a half via hole (created at the dicing stage). The design of the supporting circuit board is an important part of the design process as matching into this can have a significant effect on the return loss of the finished assembly or system element. In general some tapering of the track in the support board is required to match the edge via size, as is some adjustment of the line connecting the edge via to the first resonator.

Figure 3 shows a typical 3D file in CST and the simulation results. Simulation time for this structure is typically less than 4 minutes so adjustments can be made to the filter elements and analysed in a reasonable time frame.

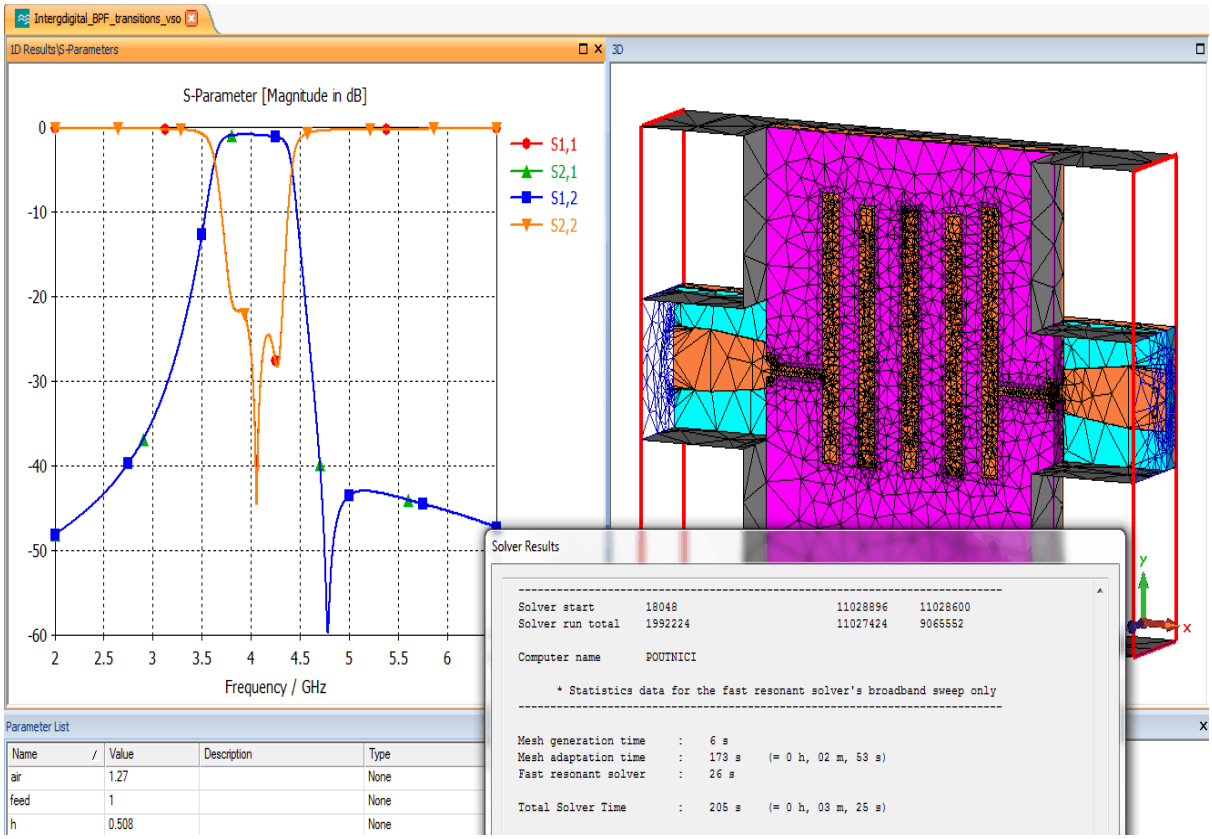

Figure 3 Results and model in CST 3D simulator

There are some important simulation decisions to be made to ensure the simulation results match the final realised design. Firstly was the choice of solver and the meshing regime. In this case early experiments had shown that for hexahedral meshing, analysis times increased dramatically with the complexity of the model and the required convergence to a reliable result.

Selecting tetrahedral meshing with careful choice of local meshing step sizes, adaptive mesh and monitoring of model convergence resulted in good correlation between the simulated insertion loss and passband frequency as seen in the prototype parts. The general purpose solver was found to give a good trade-off between accuracy and analysis times.

Other elements such as modelling the vias as solid blocks rather than holes, the removal of radius edges from the design (such as required by the laser beam diameter used to drill vias holes before the Gold is deposited) and selectively allocating some non-critical parts of the structure as PEC (perfect electrical conductor) in the model all assist in speeding up the simulation without any loss in accuracy in the realised design.

Fabrication

The design was then handed over to a wafer fabrication subcontractor who carried out the layout work, laser drilling via holes, creating the masks, depositing the Au layer, etching and finally dicing the structure. Figure 4 shows a summary of the process flow. These are well understood and fairly straight forward MIC fabrication industry processes. It was always the aim to use standard processes in the manufacture of these structures and not to have to customise any manufacturing protocols specific to our designs.

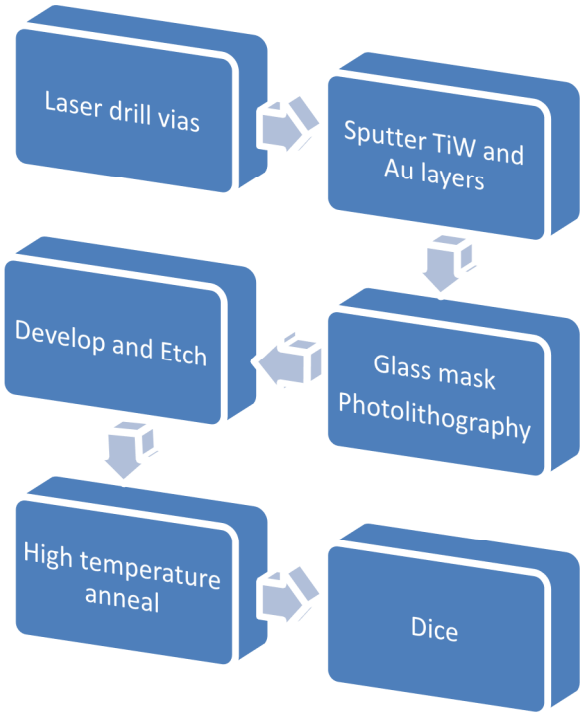

Figure 4 Sub-contractor work flow

Several designs are often placed on one wafer In this case three structures together with a 50Ω test line were manufactured. Figure 5 shows the wafer layout and drilled via holes. Figure 6 shows the delivered manufactured parts. Note the typical footprint for each device is 9 x 7 mm.

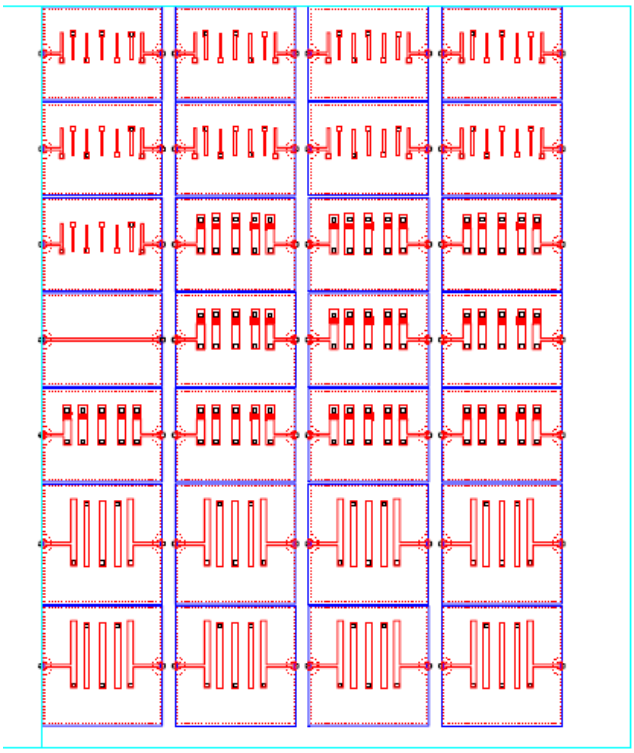

Figure 5 Wafer layout

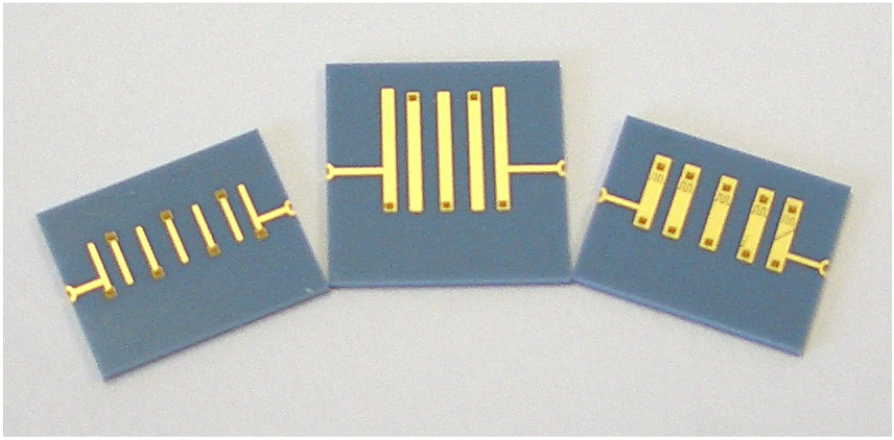

Figure 6 Realised devices

Measured Performance

In order to verify the performance of the filters two different techniques were used for testing purposes. Firstly a carrier circuit board was built and the tiles soldered down on to the surface. In order to simplify the test jig side walls and lid were omitted form the design and

the test data checked against a 3D model with side walls and lid lifted away from the device. This is only to be regarded as sample testing technique, once the device is soldered it can no longer be shipped and the test fixture is difficult to reuse. This is shown in figure 6. Note that this illustrates the small footprint of the device as these are standard SMA connectors on the test jigs.

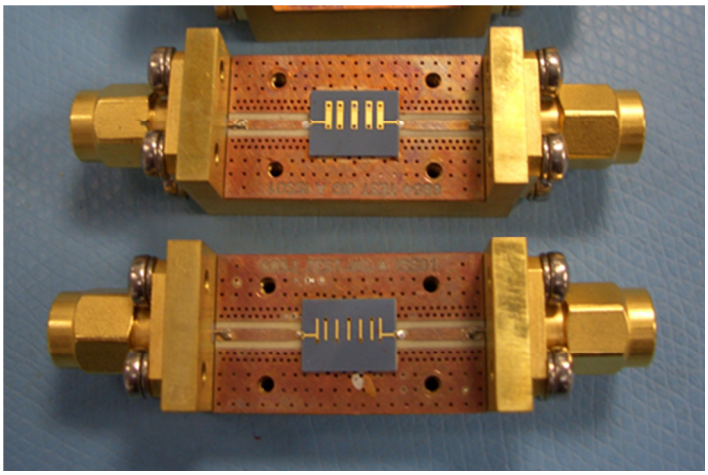

Figure 6 Temporary solder fixture

The initial test data from this approach was very promising but in parallel a universal MMIC test fixture had been purchased and modified to meet our needs. This is shown in figure.7.

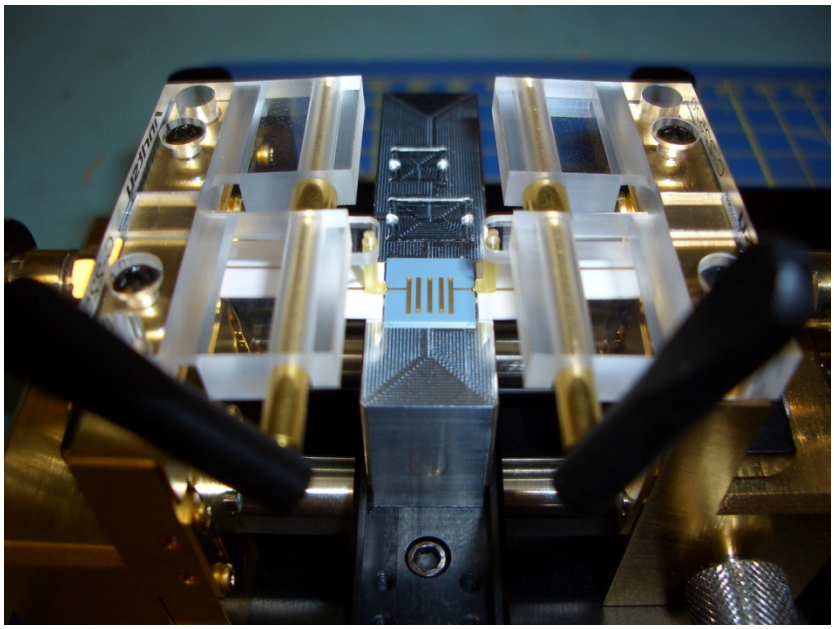

Figure 7 MMIC test fixture

The test fixture allows non-destructive testing and when fitted with a cover (omitted her for clarity) allows for full a characterisation of the device as if it were mounted on a carrier board with housing. Connection is made to the device using small sprung tracks held in place by nonconductive feet. The test fixture can be calibrated out using standard calibration techniques if required. Connecting to a standard VNA realised the test data shown here super imposed on the simulated data from the 3D model.

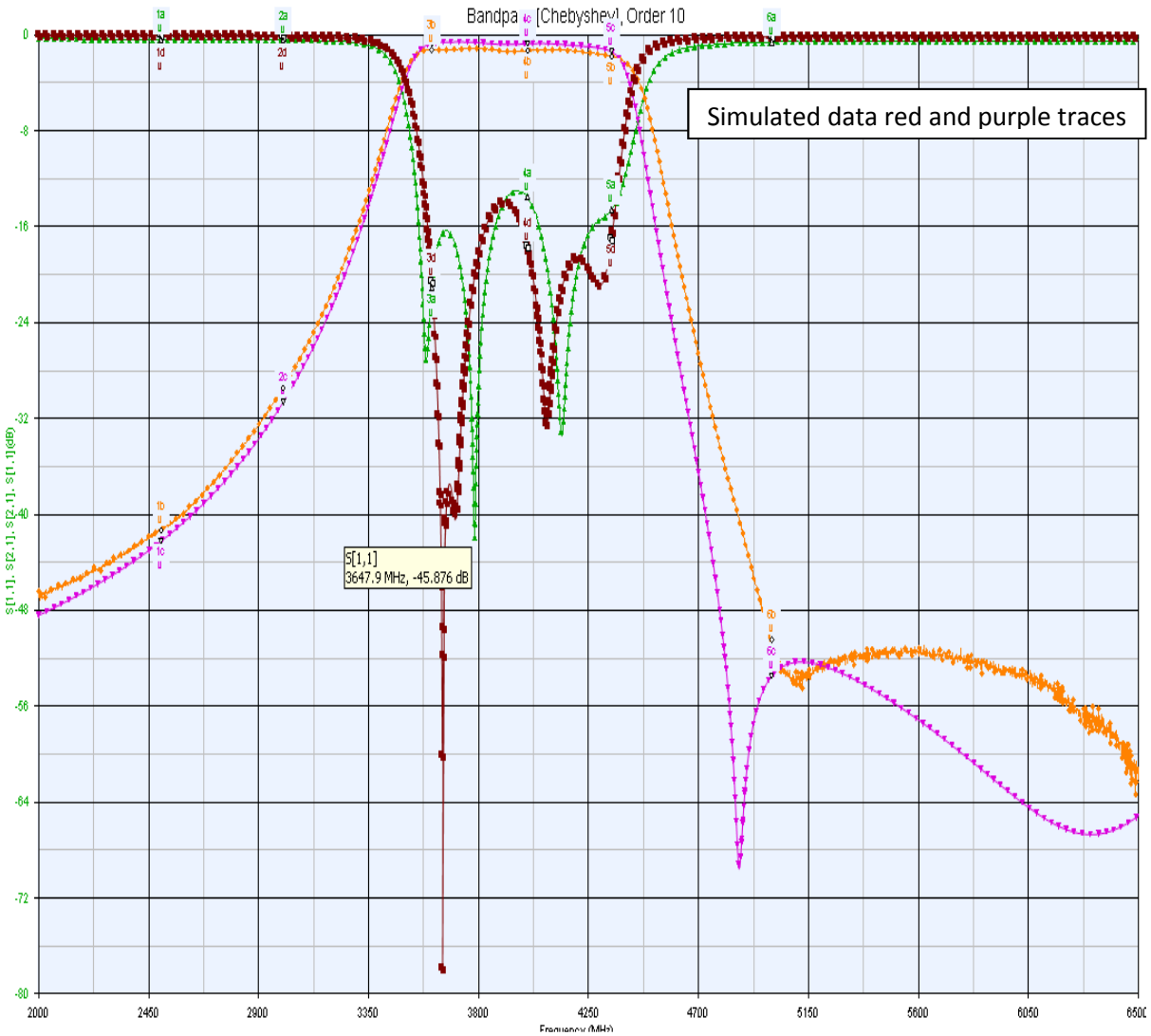

Figure 8 Simulated and actual data overlay 4 GHz Filter

Figures 8 and 9 show simulated and actual test data taken from the MMIC fixture For two designs one centred on 4 GHz the other centred on 9.5 GHz. Both illustrate good correlation between model and actual device with the small differences in insertion loss being entirely due to the additional loss of the test fixture. This verified by measuring one of the 50Ω test lines. The relatively poor return loss of the 9.5 GHz device results from the use of a standard one size edge via on all of the parts on this wafer which was optimised for frequencies below 6 GHz. Subsequent designs around this frequency have used smaller via structures to produce improved return loss performance

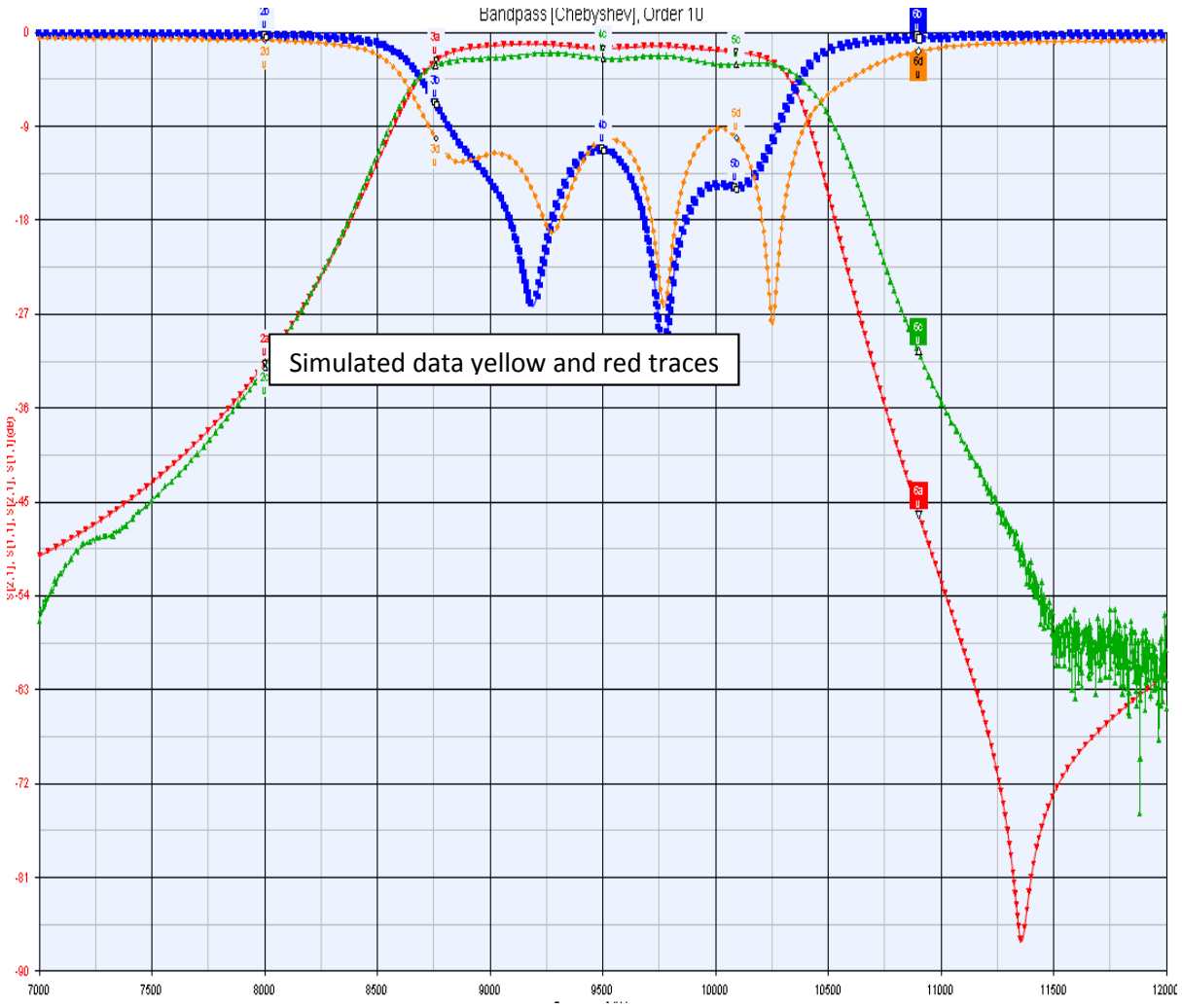

Figure 9 Simulated and actual data overlay 9.5 GHz Filter

The only real issue to address is the potential improved modelling of the high side notch in the filter skirt which appears low in frequency in the 3D simulation compared to actual test data (in the 9.5 GHz design it is just visible at the start of the measurement noise). As this is a result of cross couplings within the design additional localised meshing is likely to resolve this issue.

Conclusions

This paper has presented the design, simulation and measured performance of thin film filters using standard MIC fabrication techniques. It has proved to be an accurate and robust method for generating miniature thin film ceramic filter design over a range of frequencies.