MMICs for Broadband Receiver Applications

L.M.Devlin*, A.W.Dearn*, G.A.Pearson*, S.Williamson*, P.D.L.Beasley†

* Plextek Ltd, London Road, Great Chesterford, Essex, CB10 1NY, UK; (lmd@plextek.co.uk)

† QinetiQ, St. Andrews Road, Great Malvern, Worcestershire, WR14 3PS

Abstract - This paper details the design, realisation and measured performance of a set of MMICs for broadband receiver applications. Five different MMICs are described: A 0.5 to 20GHz dual channel limiter, a 2 to 18GHz dual channel Low Noise Amplifier (LNA), a DC to 20GHz dual channel Single Pole Double Throw (SPDT) switch, a 2 to 18GHz upconverter and a companion downconverter. The MMICs can be used to implement a compact, dual channel 2-18GHz receiver and an example of this is also described.

Dual Channel Limiter

Introduction (Limiter)

Limiters are used at the front-end of a system to protect more sensitive circuitry that follows. A limiter should attenuate any high power input signals to a level that the following receive circuitry can withstand without damage. This dual channel limiter MMIC was designed to provide receiver protection for a broadband monopulse system [1].

PIN diodes are a popular technology choice for limiter realisations because they are able to handle relatively large amounts of power using a comparatively small device. An integrated realisation allows accurate amplitude and phase matching of the two channels, which is important for a monopulse system, and results in low parasitics which facilitates the very large operating bandwidth of the design. Triquint Semiconductor Texas' Vertical PIN diode (VPIN) process was selected for the realisation of the Monolithic Microwave IC (MMIC).

A PIN diode takes its name from its structure; it comprises a region of high resistivity intrinsic material sandwiched between a region of P-type semiconductor and N-type semiconductor. When the PIN diode is forward biased, charge carriers are injected into the I region lowering its resistance. Thus at RF and microwave frequencies a PIN diode behaves as a current controlled resistor. Figure 1 shows an equivalent electrical circuit model for a PIN diode at RF/microwave frequencies. A model for a discrete, packaged diode would also need to incorporate appropriate packaging parasitics.

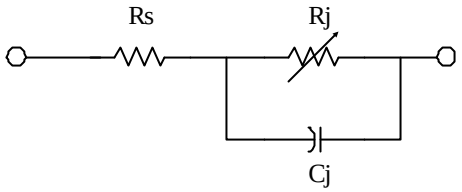


Figure 1: Electrical equivalent circuit of a PIN diode

PIN diodes shunt mounted to ground can be used to realise a limiter function. When high power RF signals are present, charge carriers are injected into the I region of the diode on one half cycle and removed on the opposite polarity half cycle. An accumulation of charge develops in the I region reducing the diode's resistance. This charge generation also results in a DC current (a rectified portion of the RF signal) which must have a DC return path in order for the limiter to function properly.

Figure 2 shows the circuit diagram of a limiter from [2], which uses an RF choke to provide the DC return.

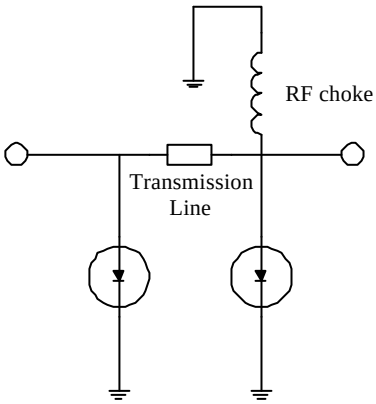


Figure 2: Limiter circuit from [2]

An alternative topology that does not require an RF choke is shown in Figure 3 (from [3]). In this case two back to back diodes are used. Charge is injected into the I region of each

diode on alternate half cycles and each diode acts as the DC return for the other's rectified current.

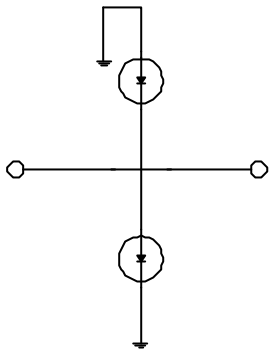


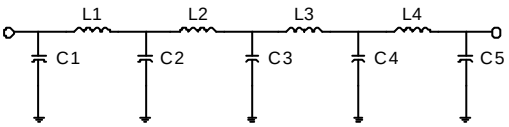
Figure 3: Limiter circuit from [3]

Circuit Design (Limiter)

The PIN diodes fabricated on the Triquint Texas' VPIN process have very low off state capacitance, which makes them suitable for use up to mm-wave frequencies.

The design methodology adopted, to cover the desired 0.5 to 20GHz frequency range, was to absorb the parasitic capacitance of the diodes within a filter structure. This conveniently allows multiple stages of shunt diodes to be incorporated into the design, which provides limiting to slightly lower power levels than with a single diode pair.

The starting point for the design was a 9th order maximally flat (Butterworth) low pass filter [4] with a cut off frequency of 21GHz. A schematic of the filter with component values is shown in Figure 4.



C1	0.053pF	L1	0.379nH
C2	0.244pF	L2	0.712nH
C3	0.303pF	L3	0.712nH
C4	0.244pF	L4	0.379nH
C5	0.053pF		

Figure 4: 9th order low pass filter

The next step was to replace the centre three shunt capacitors by antipodal diode pairs. The reason a 9th order filter was used as the basis for the design, in preference to a lower order filter, is because it results in larger values for the central three shunt capacitors. This means the size of the diodes used to replace them can be larger, which increases the maximum power handling capability of the limiter.

DC blocks were also added to the input and output of the filter and the series inductors were replaced by short lengths of high impedance transmission line. For operation to 20GHz, the required values of the series inductors are very small, which means that an MMIC realisation is very effective.

The values of the series inductive elements and end shunt capacitors were optimised to achieve low insertion loss across the operating band. Bonding interface parasitics were also included to ensure optimum performance of the assembled die. The final circuit schematic of one channel of the limiter is shown in Figure 5. Note that the outer two shunt capacitors are omitted as their value tended towards zero in the final stages of the filter optimisation.

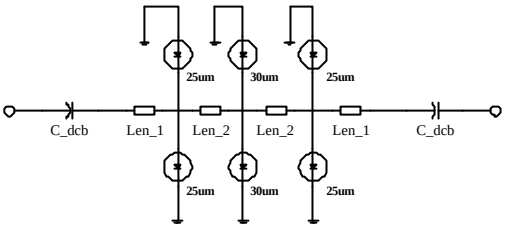


Figure 5: Schematic of the limiter circuit

A photograph of one of the dual channel limiter die is shown in Figure 6. The size of the die has been significantly increased, beyond the minimum required, to fit in with the arraying of other circuits fabricated on the same mask set. This allowed the TRL calibration structures to be included on the die.

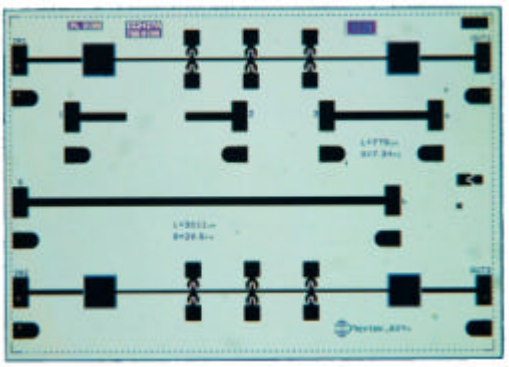


Figure 6: Photograph of one of the dual channel limiter die

Measured performance (Limiter)

The small-signal s-parameters of all limiters, from 4 wafers have been measured. Figure 7 compares the RF On Wafer (RFOW) measured performance of a typical part against the simulated. The measured insertion loss is less

than 0.8dB from 0.5 to 20GHz and is in very good agreement with the simulated. The measured return loss is lower than that simulated but is still better than 14dB across most of the band, degrading very slightly at the band edges. The average RF yield was 93%.

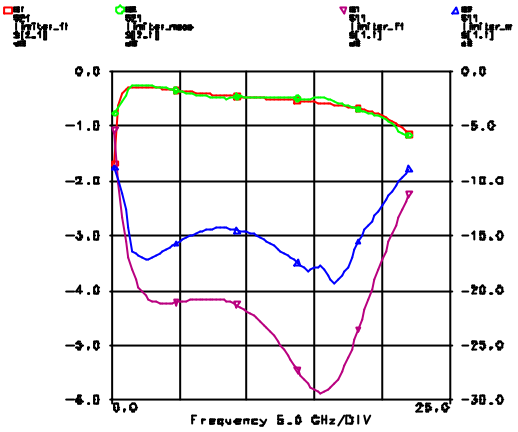


Figure 7: RFOW measured versus simulated small-signal performance

The power compression (signal limiting) performance was measured on a sample (5%) basis. Test equipment limitations meant that the highest output power, which could be generated at the probe tips, was +25dBm. However, when measured the limiters were around 10dB into saturation at this input power level. Figure 8 shows a plot of the power compression characteristics of a typical limiter measured at frequencies of 2, 5, 12 and 18GHz. The limited output power was between 15 and 16.5dBm.

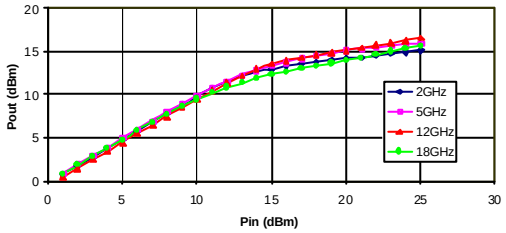


Figure 8: Power transfer of limiter

As would be expected, the amplitude and phase matching between channels is excellent, within 0.1dB and 1°.

Limiter die were subsequently assembled into modules to allow evaluation at higher power levels. Figure 9 shows a photograph of one of the modules. Figure 10 shows the measured power transfer characteristics of a limiter module at 10GHz. The peak output power level is +17.9dBm for an input power of 27.5dBm. The "kink" in the characteristics of Figure 10, at around +30dBm input, is a real and repeatable feature [5].

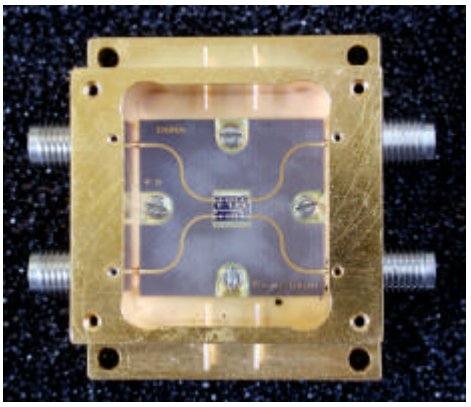


Figure 9: Dual channel limiter module

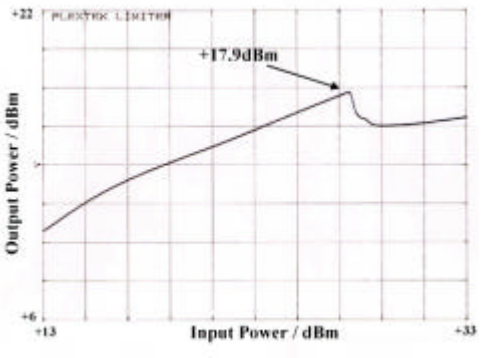


Figure 10: Power transfer characteristics of limiter module at 10GHz

A number of limiters have been tested to destruction. The input power level, which was required to cause destruction, was around +39dBm at 5GHz and around +37.5dBm at 17GHz. Following destruction, the limiter continued to provide protection but the small signal insertion loss had increased to a level, which would necessitate replacement of the module for continued operation of the system.

Conclusions (Limiter)

Details of the design, fabrication and evaluation of a dual channel limiter MMIC have been presented. It exhibits very low insertion loss (< 0.8dB) from 0.5 to 20GHz. The saturated output power (at 10dB compression) of the limiter is between 15 and 16.5dBm across the entire band and it can handle CW power levels of 4W. Amplitude and phase match between the channels is within 0.1dB and 1°. For additional information see reference [6].

Dual Channel LNA

Introduction (LNA)

The most appropriate topology for a broadband LNA is a distributed amplifier. Each amplifying stage employs multiple transistors, the capacitive input and output impedances of

which are absorbed into a low pass filter structure (sometimes also referred to as an "artificial transmission line"). The approach is well suited to a monolithic implementation as, provided that the transistors are very similar, the amplifier performance is relatively insensitive to process variation.

Circuit Design (LNA)

The simplified schematic of a distributed amplifier is depicted in Figure 11. A DC blocking capacitor at the RF input is followed by a low pass filter structure comprising a ladder network of shunt capacitors and series inductors. It can be seen that the central shunt capacitors of the filter have been replaced with transistors, in a similar manner to the design approach adopted for the limiter. The filter structure is terminated in a 50Ω load, ensuring a good broadband input match. The RF input signal travels along the filter structure exciting the input of each transistor. Another low pass filter structure is used to combine the outputs of the transistors resulting in broadband amplification.

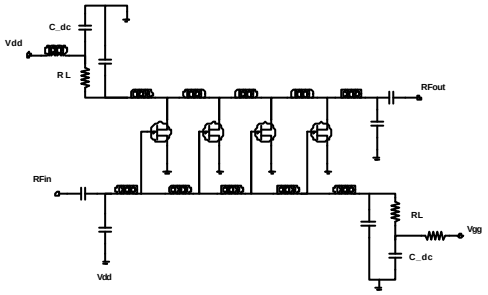


Figure 11: Distributed amplifier, simplified schematic

The 0.25µm gate length Pseudomorphic High Electron Mobility Transistor (PHEMT) process Triquint Semiconductor Texas was selected for implementation of the LNA. With a practical microwave distributed amplifier IC, the value of the series inductive elements are small enough that they can be realised using short lengths of high impedance microstrip transmission line. Four transistors are depicted in the schematic of Figure 11, however a 3 transistor design was adopted as this allowed a slightly positive gain slope to be implemented, as is evident in the simulated performance of Figure 12. This simulation includes the effects of bonding parasitics.

The simulated Noise Figure (NF) and Rollet stability factor (K) of the amplifier are plotted in Figure 13. The mid-band NF is around 3dB rising to 4dB at the top of the band and approaching 5dB at the bottom of the band.

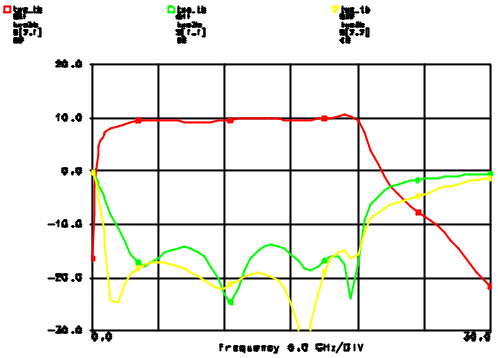


Figure 12: Simulated LNA performance, including bonding parasitics

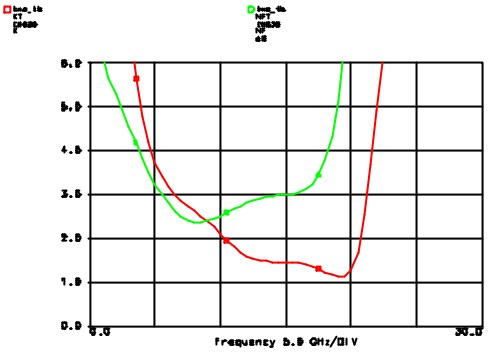


Figure 13: Simulated LNA NF and K, including bonding parasitics

A photograph of the dual channel LNA MMIC is shown in Figure 14. Spiral inductors have been used for the injection of drain bias. The shunt capacitors at the input and output are realised as open circuit stubs. A small amount of series inductance is included at the drain terminal of each transistor.

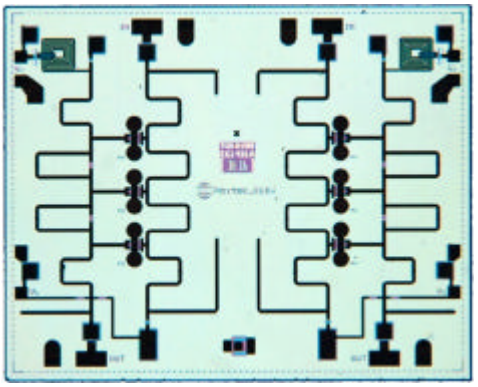


Figure 14: Photograph of the dual channel LNA MMIC

Measured Performance (LNA)

Measurements were made with the LNA mounted in to a connectorised module, shown in Figure 15. The simulated versus measured performance of the LNA is shown in Figure 16 and Figure 17. The gain response rolls off slightly earlier in frequency than the simulated

but other than this the measured and simulated results are in good agreement.

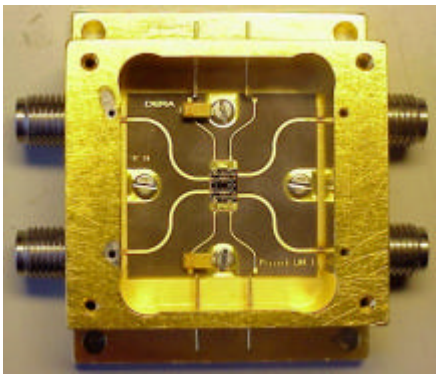


Figure 15: Photograph of a dual channel LNA module

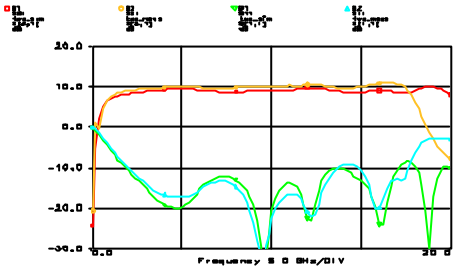


Figure 16: Measured versus simulated gain and input match of the LNA

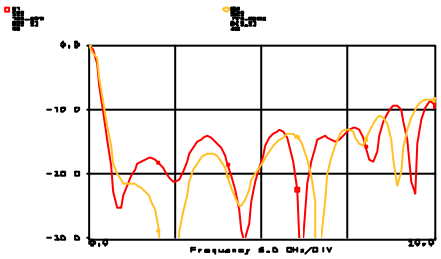


Figure 17: Measured versus simulated output match of the LNA

The power transfer characteristics of the LNA module were also measured and indicated a 1dB gain compressed output power of +15dBm. The measured mid-band NF of the LNA module is 3.5dB, which is in good agreement with the simulated performance.

Conclusions (LNA)

Details of the design, fabrication and evaluation of a dual channel LNA MMIC have been presented. The small signal gain is 10dB, output referred 1dB gain compression point +15dBm and mid-band NF 3.5dB.

Dual Channel SPDT

Introduction (SPDT)

The dual channel Single Pole Double Throw (SPDT) switch MMIC has an operating band of DC to 20GHz. Two SPDTs are realised on the same die, as depicted in Figure 18. Whilst the two SPDTs would switch together in monopulse receiver applications, the facility for independent control of each was also included.

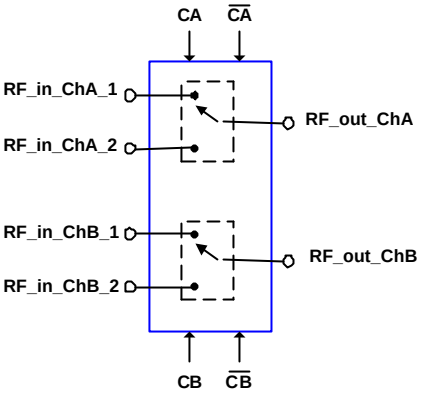


Figure 18: SPDT MMIC functionality

The same 0.25µm PHEMT process used for the LNA was selected for the realisation of the switch. PHEMTs make excellent switching devices as their drain-source resistance behaves as a voltage variable resistor, with the resistance value being set by the gate-source voltage [7]. When used as a switch, a PHEMT is operated with the drain and source at zero volts DC. The RF signal path is drain to source and the gate is the control terminal.

The on-case resistance of transistors fabricated on the Triquint 0.25µm PHEMT process is around 1.8Ωmm and the off-case resistance about 10kΩmm. There is also a parasitic drain-source capacitance of around 0.3pF/mm. It is this capacitance that limits the high frequency isolation of the off-state transistor. This means that simple series/shunt switch topologies will not provide adequate performance to 20GHz [7] and alternative topologies need to be adopted, as described below.

Design (SPDT)

A distributed topology was adopted for the switch design, as depicted in Figure 19. This technique extends the operating frequency of the switch by absorbing the off state capacitance of shunt mounted transistors into a low pass filter, in a similar manner to the LNA and limiter designs described above.

Table 1 shows the complementary switching control of each SPDT. The path from the input to one output is low loss whilst the path from the input to the other output is high isolation. The shunt mounted PHEMTs in the on-case path are pinched-off (high-resistance state) and the corresponding series device is switched on

(low-resistance state). Since the parasitic capacitance of the shunt mounted transistors has been absorbed into a filter structure, the on-case path loss is low.

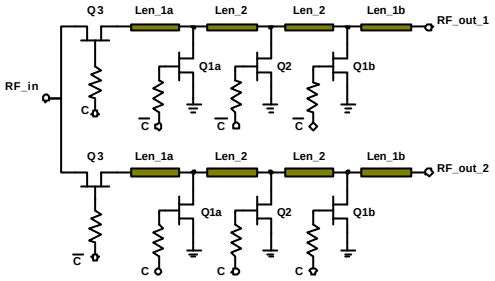


Figure 19: Schematic of the distributed SPDT

C	$\overline{C}$	Active output
0V	-5V	RF_out_1
-5V	0V	RF_out_2

Table 1: Truth table for the SPDT

With the on-case switch arm the shunt mounted PHEMTs are on (low-resistance state) and the corresponding series device is pinched-off (high-resistance state). The low resistance of the shunt transistors results in high insertion loss so providing good switch isolation. At low frequencies the series transistor is high impedance but at higher frequencies the parasitic capacitance means the transistor provides only modest isolation. This problem is addressed by ensuring that the line length 1a, together with the off-state series transistor, transforms the low impedance of the first shunt mounted transistor to a high impedance. Thus operation from DC to 20GHz is achieved.

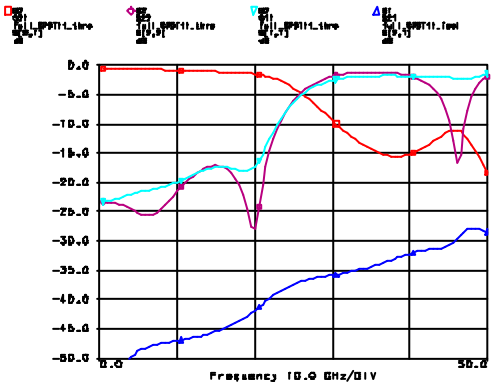


Figure 20: Final simulated performance of one SPDT

As with the limiter and LNA designs, the starting point for the switch design was to create a LPF with a cut-off frequency just above the desired upper operating frequency. The PHEMT models, and then transmission line models were then incorporated into the design and the performance re-optimised. The final simulated performance of the complete SPDT to 50GHz is shown in Figure 20. Further information about the switch design can be found [8].

Realisation and Measured Performance

A photograph of the switch IC is shown in Figure 21, the die size is 1.525mm x 2.54mm.

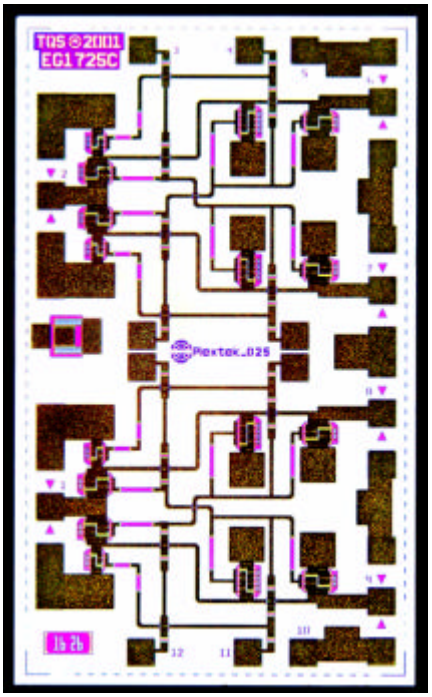


Figure 21: Photograph of the dual SPDT IC

Evaluation of the switch was carried out on ICs assembled onto an MIC carrier tile. A comparison of the measured versus modelled insertion loss and return loss from DC to 20GHz, including bonding parasitics, is shown in Figure 22. Good agreement has been obtained across the entire band. The insertion loss is less than 1dB to 10GHz and less than 1.6dB to 20GHz. The input and output return losses are greater than 14dB to 20GHz. The measured isolation is better than 22dB to 20GHz.

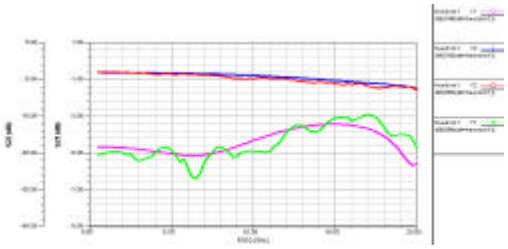


Figure 22: Measured versus modelled match and insertion loss of one SPDT

The power transfer characteristics of the switch have also been measured. Figure 23 shows the insertion loss versus input power at 4GHz. For control voltages of 0/-5V the 1dB compression point is +27dBm. With higher control voltages of 0/-8V, the P-1dB point increases by 1.5dB.

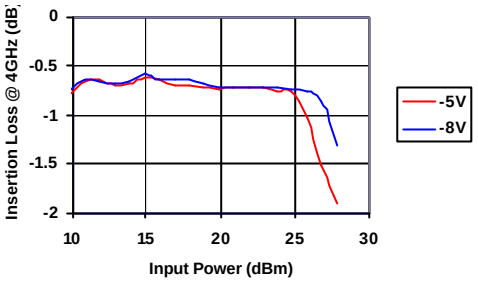


Figure 23: Measured switch insertion loss versus input power at 4GHz

Conclusions (SPDT)

A dual channel DC-20GHz SPDT has been designed, fabricated and evaluated. The measured insertion loss is < 0.7dB to 5GHz, < 1dB to 10GHz and < 1.6dB to 20GHz. The return loss is greater than 14dB to 20GHz, and isolation is greater than 22dB to 20GHz. The input referred P-1dB point is +27dBm for -5V control, and 28.5dBm for –8V control.

Upconverter

Introduction (Upconveter)

The upconverter was required to operate with an IF input range of 2-18GHz and an LO input range of 23-41GHz. These very wide operating bandwidths represented one of the key design challenges of the development.

It was decided that the IC should be based around a double-balanced mixer topology, which offers a number of important advantages compared to a single-ended design:

- All mixer ports are inherently isolated
- All even order products of the LO and/or the RF are suppressed
- Local oscillator AM noise is suppressed
- Linearity is improved

Design (upconverter)

The first consideration in the design process was the choice of mixer topology. A quad-ring resistive (switching) mixer was chosen. This topology offers small size, good linearity [9] and high LO rejection.

The quad-ring resistive mixer topology is balanced at all ports. Initial simulations assumed the availability of ideal baluns. This facilitated the selection of the optimum device size for the switching mixer. A plot of the simulated conversion loss of the quad ring mixer, versus LO drive level, is shown in Figure 24. The different traces represent RF frequencies of 2GHz, 10GHz and 18GHz. Conversion loss increases with RF frequency due to the drain-source capacitance of the PHEMT devices limiting the isolation of the switches. For an LO drive of +7dBm, conversion loss varies from 7dB at 2GHz to 11.5dB at 18GHz.

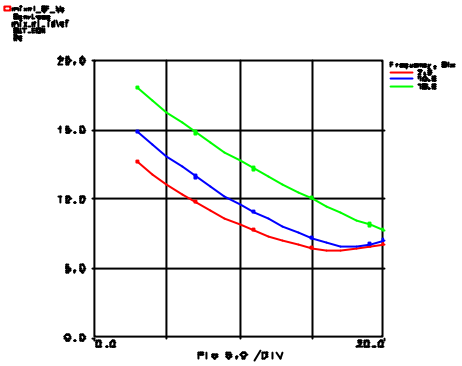


Figure 24. Simulated mixer performance

The next stage of the design was to consider the most appropriate balun topologies. The RF (21-23GHz) and LO (23- 41GHz) baluns were realised as uniplanar Marchand baluns and the IF (2-18GHz) balun as an active long-tail pair differential amplifier. Details of the balun design process are included below. The architecture of the entire upconverter IC is that shown in Figure 25.

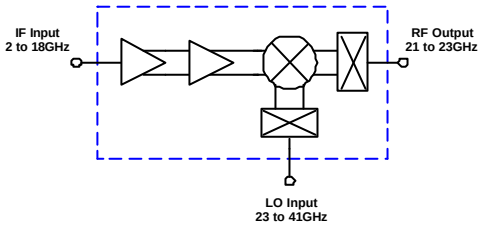


Figure 25: Upconverter MMIC architecture

Marchand baluns are capable of achieving broadband operation with low insertion loss. The implementation first described by Nathan Marchand in his 1944 publication [10], was a co-axial structure. Various printed implementations have since been described; the simplest of which is depicted in Figure 26.

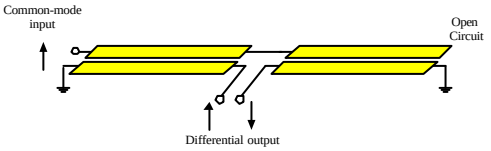


Figure 26: Printed Marchand balun

Increased coupling and therefore increased bandwidth can be obtained from a planar implementation if multiple coupled lines are used, as depicted in Figure 27. This was the balun structure adopted for the RF and LO baluns. The total length of this structure is approximately half a wavelength at the centre frequency.

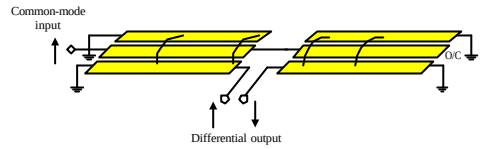


Figure 27: Multiple coupled line Marchand balun

A layout plot of the LO balun is shown in Figure 28. The layout was meandered to reduce the chip size.

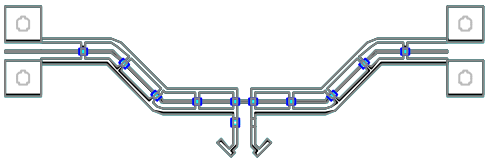


Figure 28: Layout of LO balun

Electromagnetic simulation of the Marchand baluns was carried out to properly account for the discontinuity and coupling effects of the layout. Figure 29 shows the simulated amplitude and phase difference between the two branches, which is within 0.9dB and 9° of ideal from 14 to 44GHz. The excess insertion loss of the balun is less than 0.5dB.

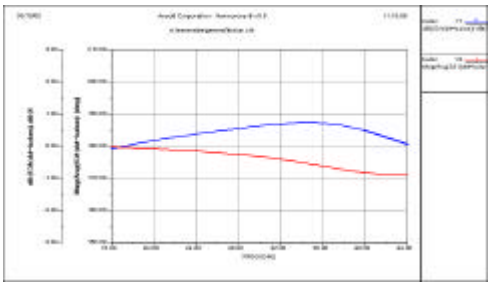


Figure 29: Electromagnetic simulation of amplitude and phase difference of the LO balun

The IF port balun needs to work from 2 to 18GHz so an integrated Marchand balun was not appropriate, both in terms of the area it would occupy and the difficulty of realising tight enough coupling to achieve the required operating bandwidth.

The solution adopted for the IF balun was to use a two stage differential amplifier. A simplified circuit diagram of the first stage is shown in Figure 30. The input is a long-tail pair biased with a current source (Q5). One transistor in the differential pair (Q4) has its gate held at ground and the gate of the other transistor (Q3) is the LO input port which is matched to 50Ω with a broadband lossy input matching network. The drain terminals are biased using active loads (Q1 and Q2) with their gate and source terminals capacitively coupled to hold them at the same RF potential. The output of this amplifier stage is a differential signal, the balance of which is improved by the use of a second differential amplifier stage.

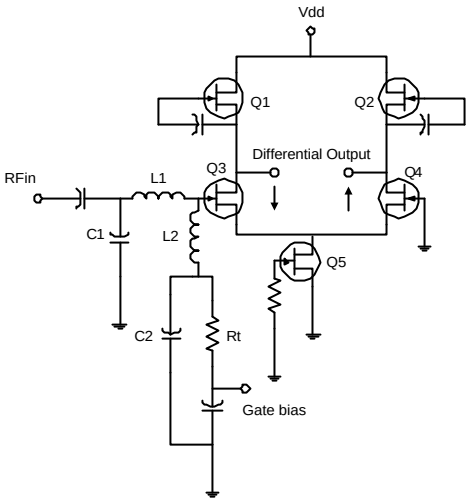


Figure 30: Input stage of IF active balun

The simulated performance of the complete active balun showed a phase difference of 180° ± 2° and an amplitude imbalance of less than 0.2dB from 1 to 20GHz.

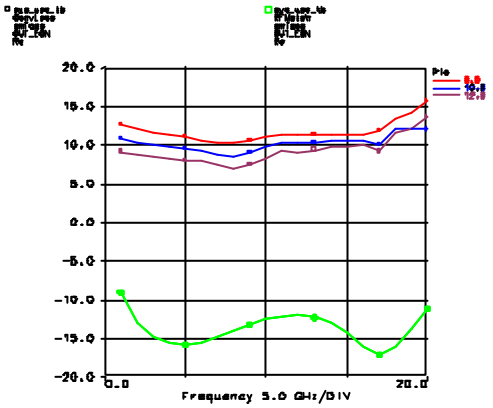


Figure 31: Final simulated performance of the upconverter

The simulated performance of the complete upconverter, including quad-ring mixer, active IF balun and passive RF and LO baluns is shown in Figure 31. Input return loss and conversion loss is shown for LO drive levels of +8, +10 and +12dBm. The input return loss is better than 12dB from 2 to 18GHz and does not change noticeably with varying LO input

power. This is a result of the isolation provided by the active balun. Across 2-18GHz the simulated conversion loss is less than 12dB for an LO drive of +10dBm.

Fabrication and Measured Performance (Upconverter)

A photograph of the upconverter IC is shown in Figure 32, the die size is 3.04mm x 3.28mm.

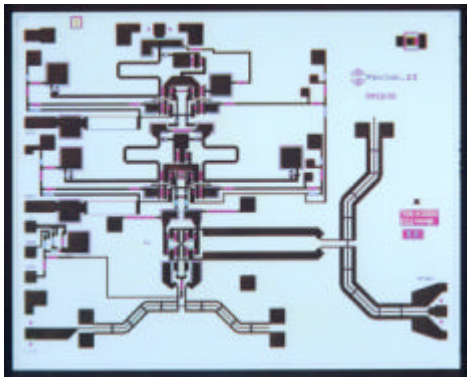


Figure 32: Photograph of the upconverter IC

Evaluation of the upconverter was carried out on ICs assembled onto an MIC carrier tile, as shown in Figure 33. This was fabricated from 0.01" thick RT/Duroid 5880 with a brass backing to give rigidity.

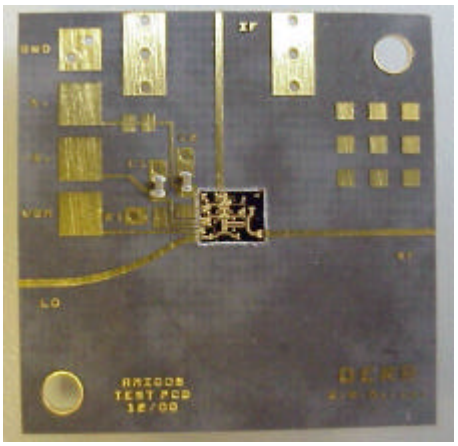


Figure 33: Photograph of the upconverter MMIC evaluation tile

The measured conversion loss of the upconverter versus IF input frequency is shown in Figure 34, for a fixed RF of 22GHz. With an LO drive of +10dBm the conversion loss is around 7dB to 14GHz, rising to 10dB by 18GHz, which is slightly better than simulated. If the LO drive is reduced to +7dBm, the conversion loss increases by around 1dB. The LO rejection is shown on the same plot and is over 30dB across the entire band. This was measured with an LO input level of +10dBm.

Measurements of conversion loss versus RF frequency were also made for a range of fixed IF frequencies and an LO drive level of +10dBm. The results are plotted in Figure 35, and show a slight increase in conversion loss with increasing RF frequency. The increased conversion loss at the top end of the IF input band (18GHz) is also evident.

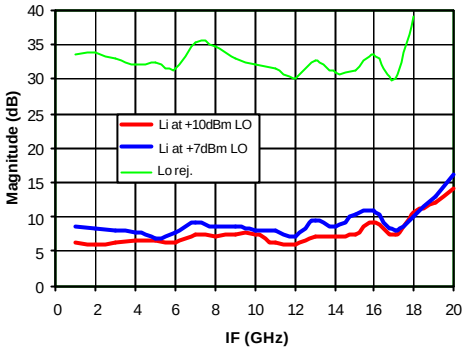


Figure 34: Measured conversion loss and LO rejection of the upconverter IC

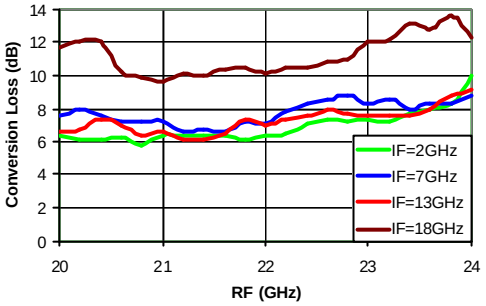


Figure 35: Measured conversion loss of upconverter across RF band

The measured IF port return loss of the upconverter is plotted against IF frequency in Figure 36. The return loss is better than 12dB from 2 to 18GHz and is in good agreement with the simulated performance.

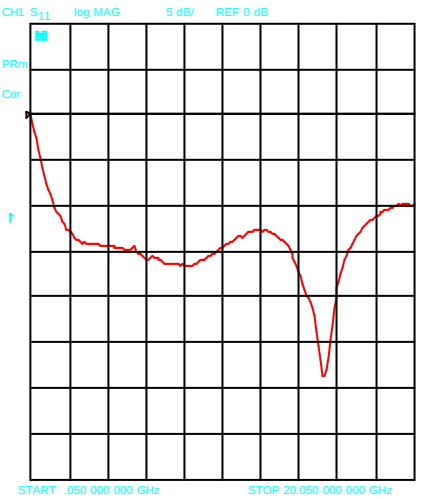


Figure 36: Measured IF port match of upconverter

Conclusions (Upconverter)

The design, fabrication and evaluation of a 2-18GHz upconverter MMIC have been described. The nominal RF output is from 21 - 23GHz and the LO input range is from 23 - 41GHz. The design includes passive baluns at the RF and LO ports and an active balun at the IF port.

Evaluation was carried out on die assembled onto an MIC carrier and, for an LO drive level of +10dBm, showed a conversion loss of around 7dB below 14GHz, rising to 10dB by 18GHz. If the LO drive is reduced to +7dBm, the conversion loss increases by around 1dB. Input return loss is better than 12dB from 2 to 18GHz and an LO rejection of greater than 30dB is achieved.

Additional detail on the upconverter MMIC can be found in [11].

Downconverter

Introduction (Downconverter)

The downconverter is designed as a companion IC to the upconverter [12]. After filtering of the wanted RF signal at the output of the upconverter (nominally a 500MHz band in the 22 to 23GHz frequency range, although wider bandwidths are viable) the downconverter performs frequency translation down to an IF suitable for digitisation.

The downconverter MMIC includes both RF and LO amplification and is therefore able to operate with a low LO drive level and provides conversion gain rather than loss.

Design (Downconverter)

The same double balanced switching mixer used in the upconverter was also used in the downconverter. The differential RF and LO drives were generated using multiple coupled line Marchand baluns, which are also similar to those used in the upconverter. The IF signal comes off-chip differentially and is combined in a surface mount wire-wound RF transformer.

The RF and LO amplifiers were both two stage reactively matched designs. Although the required RF band was 22 to 23GHz, the downconverter was designed to cover 20 to 25GHz. Similarly, although the downconverter would normally operate with a fixed LO, typically around 21.5GHz, it was designed to operate across the significantly wider LO range of 19 to 24GHz.

The simulated performance of the complete downconverter, including quad-ring mixer, RF and LO amplifiers and the printed Marchand baluns is shown in Figure 37. The plot shows the conversion gain and LO and RF port matches against RF input frequency for an LO drive level of 0dBm at 21.5GHz. Conversion gain is 4dB ±1dB across the 20-25GHz RF band. RF return loss is better than 12dB from 15 to 25GHz and the LO return loss is better than 15dB from 16 to 26GHz.

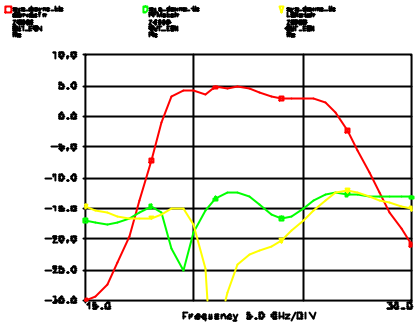


Figure 37: Simulated performance of downconverter, 0dBm LO drive

As a result of the on-chip LO buffer amplifier, the downconverter performance is quite tolerant to variation in LO drive level. A variation of ±3dB causes less than 0.5dB variation in conversion gain.

Fabrication and Measured Performance (Downconverter)

The downconverter was fabricated on the same multi-project mask set as the upconverter and is identical in die size (3.04mm x 3.28mm). A photograph of the downconverter IC is shown in Figure 38.

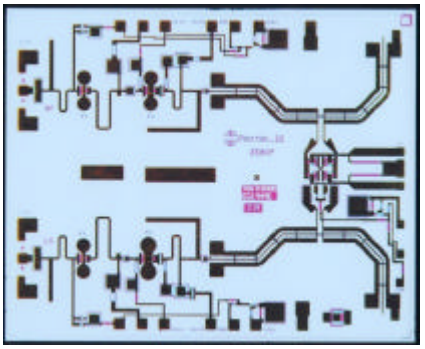


Figure 38: Photograph of the downconverter IC

Evaluation of the downconverter was undertaken with an IC assembled on to a test tile, as shown in Figure 39. The comparatively large surface mount transformer can be seen. It is used to combine the differential IF outputs into a single-ended IF that is output via an edge-mounted SMA connector.

The measured conversion gain versus RF frequency of the downconverter is plotted in

Figure 40. Three traces are shown, representing LO drive levels of –3, 0 and +3dBm with LO frequency fixed at 21.5GHz. The shaping of the gain response is caused by the IF balun, which had an upper operating frequency of 1GHz. Gain is slightly higher than simulated at 5dB, including all PCB tracking losses and the losses of the IF balun. The measured 1dB gain compressed output power was +1dBm for an LO drive of 0dBm.

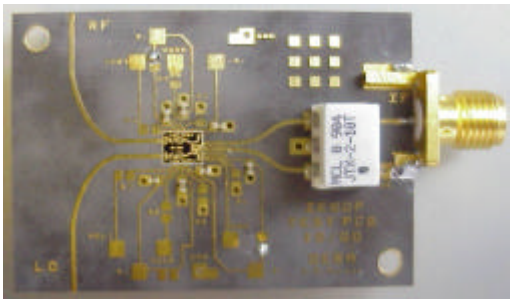


Figure 39: Photograph of downconverter evaluation tile

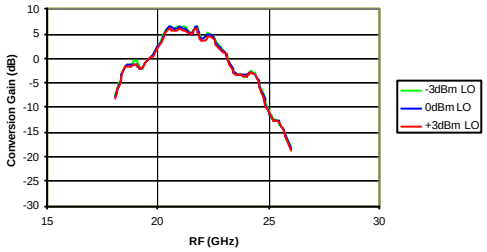


Figure 40: Measured conversion gain of downconverter

Conclusions (Downconverter)

The downconverter IC is designed to be used following the upconverter. It translates the RF output down to an IF suitable for digitisation. The design, fabrication and evaluation have been described. The MMIC operates over a wider band than required with an RF frequency range of 20 to 25GHz.

Evaluation was carried out on a die assembled onto an MIC carrier. The measured conversion gain is 5dB and varies little with LO drive levels of between –3 and +3dBm. The measured 1dB gain compressed output power is +1dBm for an LO drive of 0dBm.

Broadband Receiver MCM

A broadband receiver Multi-Chip Module (MCM) was designed, fabricated and evaluated, using the MMICs described above. The module converts signals from anywhere in the 2-18GHz frequency range to an IF suitable for digitisation, and includes low noise amplification, filtering and limiter protection. A block diagram depicting the module architecture is shown in Figure 41.

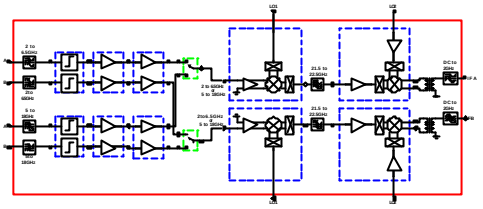


Figure 41: Block diagram of receiver MCM

The input of the receiver is split into two bands, 2-6GHz and 6-18GHz. This reflects the antenna bandwidth in the broadband ECM system for which the module was developed [12]. The bandwidth of all MMICs was adequate to cover the entire 2-18GHz band. Front-end filters remove out of band signals, then the limiter ICs are used to provide protection of the receiver. Two cascaded LNA ICs are used in each channel to improve sensitivity.

Following the LNAs, RF switches route either the pair of 2-6GHz inputs or the pair of 6-18GHz inputs to a dual channel frequency converter. (At the time the module was developed the dual channel switch ICs described above were not yet available and commercially available parts were used). Frequency conversion is realised by upconverting, using a broadband swept LO, to an intermediate frequency at around 22GHz. Coupled line bandpass filters are then used to reject out of band signals before the wanted band is downconverted to IF using a fixed frequency second LO. The differential IF output of the downconverter IC is transformed to single-ended using a surface mount balun. Low pass IF filtering is also included.

The module housed two boards; a microwave board containing the GaAs MMICs and filters and an FR4 board containing the bias conditioning and control circuitry. Great care was taken with the layout of the microwave board to preserve amplitude and phase symmetry throughout, so that good amplitude and phase balance was obtained between the two channels.

A photograph showing the two boards, with the microwave board mounted in the module housing, is shown in Figure 42. The module housing is gold plated aluminium and measures approximately 180mm x 100mm x 23mm, including a separate 3mm flat lid. The bias conditioning and control board sits above the microwave board in the housing. Interconnection between the two boards is

made using spring-loaded probes. An exploded view of the complete assembly is shown in Figure 43.

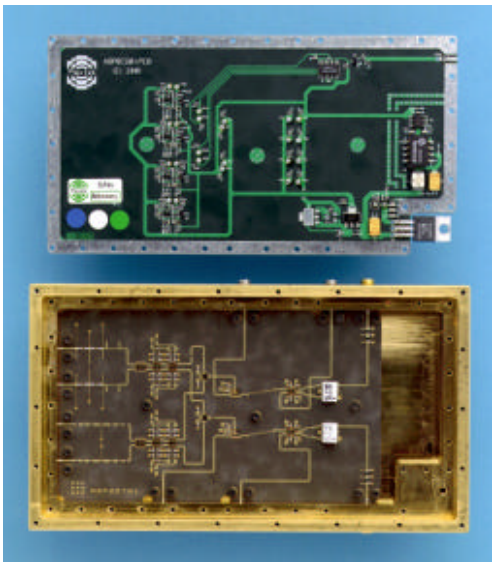


Figure 42: Photograph of the receiver module

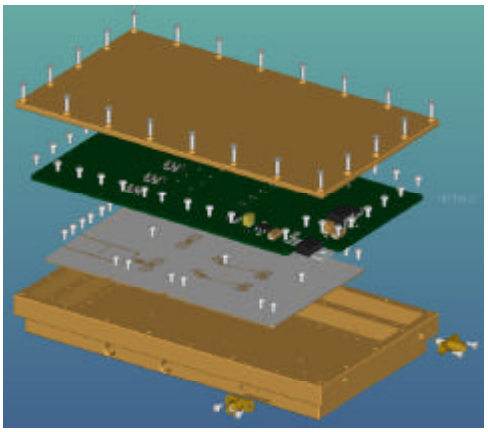


Figure 43: Exploded view of the receiver module

The measured conversion gain of the complete receiver MCM is 10dB, and the noise figure 7dB. More detail on the design and measured performance of the receiver MCM is available in [12].

Conclusions and Summary

This paper has described the design, realisation and evaluation of five different MMICs all designed for broadband receiver applications. Measured performance of all MMICs is in good agreement with the simulated performance, across the full operating bandwidth. The MMICs were designed to allow the implementation of a compact 2-18GHz dual channel receiver that makes use of an upconverting architecture. A prototype receiver module has been produced using the MMICs and a summary of this is also presented.

VII. REFERENCES

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