EMBEDDED DIE PACKAGING FOR KA BAND PHASED ARRAY MODULE

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Summary: In this project we will be balancing thermal integration of the active components, while managing the parasitic performance and loss of the system in the embedded Die PCB packaging. This project is aimed to reach to Ka for 5G application.

This project was collaboration between Microchip, SAAB and CSA Catapult. SAAB was providing the RF GaN devices, Microchip provided fabrication process and CSA catapult completed the thermal analysis and proposed packaged layout and EM model.

Introduction: Many of the megatrends in technology we are currently seeing are driven by an increase in the number, and complexity of sensors and communication systems, this is true for civilian applications such as future telecoms, satellite communications and equally for airborne platforms. Across this space there is an underlying trend to make them smaller, more energy efficient, and improve the data rate using phased array systems to focus the energy where it is needed.

High performing phased array systems are more challenging the higher up in frequency they operate due to smaller size, worse efficiency, extreme heat fluxes, and increased sensitivity to parasitics. To enable these systems, new packaging and integration solutions that enable efficient cooling while minimizing microwave parasitic and losses and maintaining reliability are needed. More efficient, highly integrated, and compact sensors and communication systems reduce weight, enable more efficient integration, and reduce energy consumption, which are all key drivers for future airplanes and airborne platforms. Furthermore, small, and light weight sensors at a lower cost would enable more widespread adoption of detect and avoid radars as well as imaging landing radars for all weather landings for commercial airplanes. This would result in safer flights, as well as reduced energy consumption.

In this paper, present developing a new compact, lightweight, energy efficient, reliable, and cost-efficient solution for microwave front-end modules up to at least 18 GHz. We will integrate multiple transceivers in a single module (e.g. a 4 by 4 active antenna solution) and embed common building blocks of a communication/sensor system such as amplifiers and filters. The proposed solution enables heterogeneous integration of different semiconductor technologies to maximize performance and allow for more cost-efficient solutions. Focus will be on embedding GaN MMICs due to the high power and high temperature capability of this relatively new semiconductor technology. Although the focus is on the microwave front-end, there is a clear path towards integration of CMOS logic for fully digital and compact transceiver solutions. The antennas equally lend themselves to being integrated in the module or surface mounted, and this project will provide an interface to enable this.

The improvements in the developed packaging technology would directly address commercial microwave sensor and communications systems. It is thought that by starting with the perhaps most complex use-case of high frequency phased arrays, the developed approaches could in the future be adapted to low frequency as well as high-efficient power electronic solutions. The power electronics have the same drivers for solutions optimized for compactness, reliability, and thermal performance, which has been highlighted as a clear requirement for both hybrid and electrical propulsion, clearly a key future direction for aviation.

This project was collaboration project between CSA Catapult, Microchip and Saab. The main responsibility from Catapult was doing thermal management and EM modelling for package and interconnects.

The integration plan

In this section, the floor planning for MMIC GaN devices are optimized based on a 2x2 phased array antenna module and the thermal management requirements. The module contains four antenna element RF feeds, four transceiver front-ends formed by LNA, PA and SPDT switch and Single layer capacitors (SLCs).

The size of MMIC GaN devices were defined by the supplier which is SAAB in this project. The size of each tile has been calculated based on number of devices and floor plan. The location of devices are optimised for best thermal management of power amplifiers, the location of each antenna element and the RF input and output pins.

The floor plan ensures the shortest bond wire length between MMICs, MMICs and SLCs, and MMICs and TLs. To compensate for the bond wire parasitic, the impedance matching should be considered on chip. Alternatively, the MMICs with balanced configuration can be considered due to their insensitivity to the termination impedance.

Since large SMDs occupy a considerable area due to their size, 100pF single layer capacitor has been proposed for high frequency decoupling while large SMD capacitors contributing in low frequency decoupling can be placed off the chip (on the board).

Figure 1 shows one example of integration plan in this project.

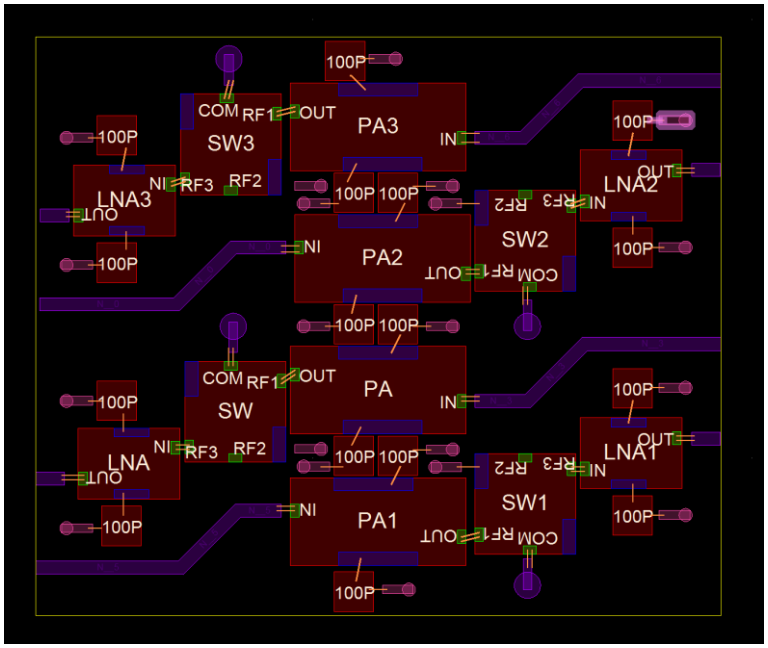


Figure 1 : integration plan for phased array

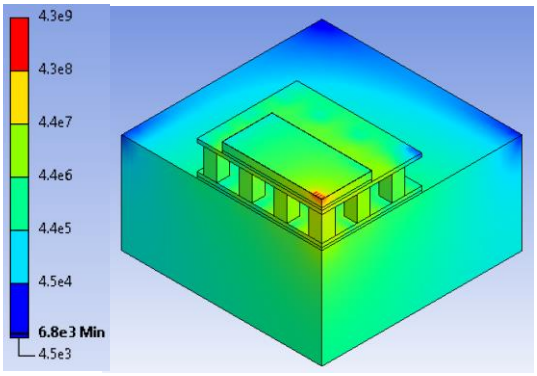
Based on manufacturing technology the number of layers and material has been defined. In this project the manufacture of embedded PCB was Microchip which provided the details of materials for each layers.

Thermal management :

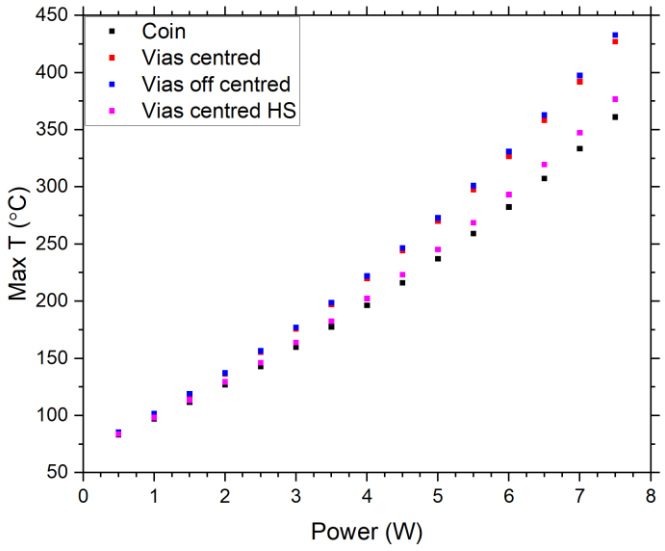
The thermal aspect of the project began by investigating the proposed package design and the potential materials used. The initial simulations explored the performance difference between a silver epoxy and silver sintering die attachment, with the impact on maximum temperature shown in Figure 2. The key take away was that silver epoxy was not suitable for die attach as the temperature rise would be significant enough to limit the performance of the system, meaning that soldering, or sintering were necessary. Figure 3 (a) shows a false colour plot of the heat flux within a package containing copper vias through the host PCB. The temperature results for the simulation of copper coin and copper vias – both centred and off centred on the device – and the copper vias with a heat spreader are shown in Figure 3 (b). It was found that although a copper coin gave the best results for the mounting substrate, copper vias were acceptable particularly when paired with a heat spreader.

The second phase of the project focussed on the characterisation of the thermal test chips developed by SAAB. The purpose of these test chips, which have multiple temperature sensors integrated onto them, is to provide an assessment of the thermal performance of the final package solution. To enable this, simulations were created to two different configurations of sample - one where the chip is bonded to a copper substrate with a thermally conductive adhesive, and one where the chip is sintered to a copper plated ceramic substrate. These simulations allow for a full characterisation of the test chips prior to their implementation in the final package, giving confidence in their application. Figure 4 (a) shows the thermal simulation result for a test chip bonded using adhesive, whilst Figure 4 (b) shows the time dependent increase in the temperature for two scenarios, one where the power load is implemented immediately (red) and the other where the load is gradually increased (blue).It was found that the gradual implementation of the power load provided a closest match to experimental data.

The simulations showed that there were two unknown material properties in the systems which were the thermal boundary resistance within the chip itself, and the die attach material. Figure 5 shows the steady state temperature measured through experiment, with the optimised simulation results and a +/- 10% error margin also shown.. In both systems, it was possible to compare the simulations to the experimental data and determine the die attach properties, but unfortunately the measurements were not sensitive to the internal thermal boundary resistance. Therefore, the next steps of the project are to develop a new test chip design which allows this measurement to be made.



(a)



(b)

Figure 3: (a) False colour plot of heat flux (W/m^2) in a package with copper vias , (b) Temperature comparison of copper vias vs copper coin

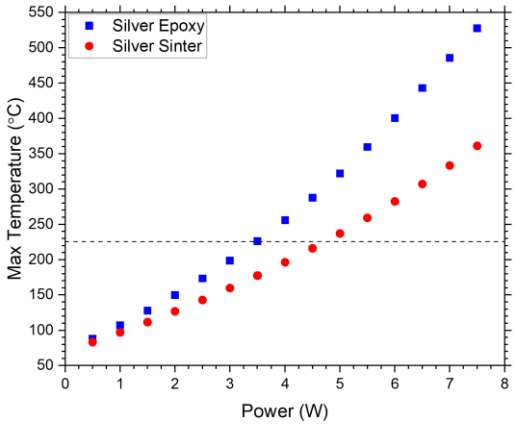
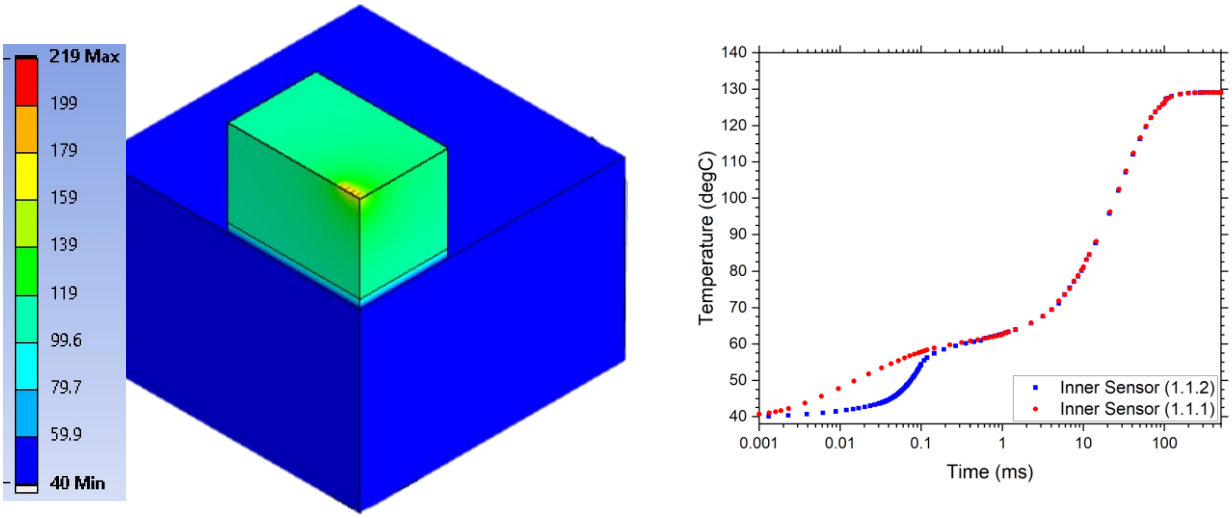


Figure 2: thermal simulation for silver epoxy and silver sintering.



(a) (b)

Figure 4: Transient temperature data from simulation

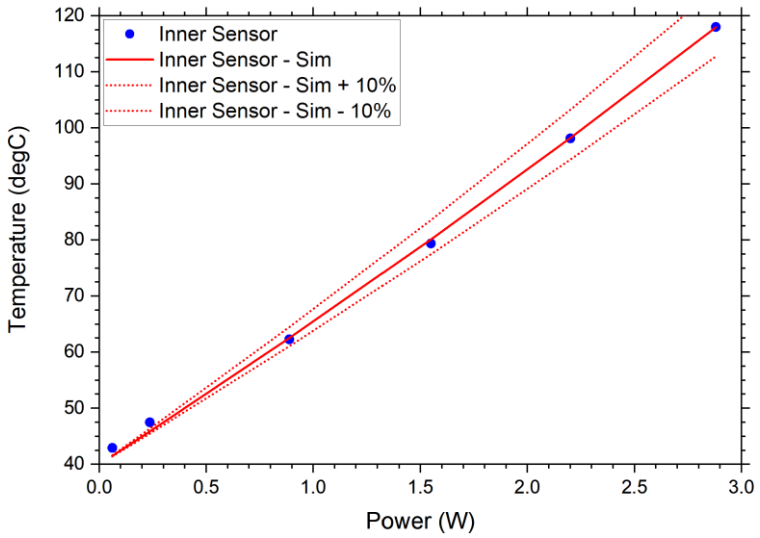


Figure 5 : Comparison of simulated data and experimental data.

EM Analysis

EM modelling and simulation

The 3D package has been designed and analysed in HFSS. The package was optimized by comparing different materials and thicknesses. The transmission line inside the package and the transition for connecting to the board has been designed and simulated. The grounded coplanar waveguide transmission line (GCPW TL) on board has been proposed to connect to the coplanar waveguide transmission line (CPW TL) on the package through the half via transition on the package. The half via acts as the soldering pad besides the transition. The final design was achieved based on Microchip proposed stack layer. The stack is formed by MT40 substrates and 4 metal layers. The mother board transmission line designed on Rogers 4003 .

In figure 6 shows the stack up of the layers of embedded PCB and how the die will implement.

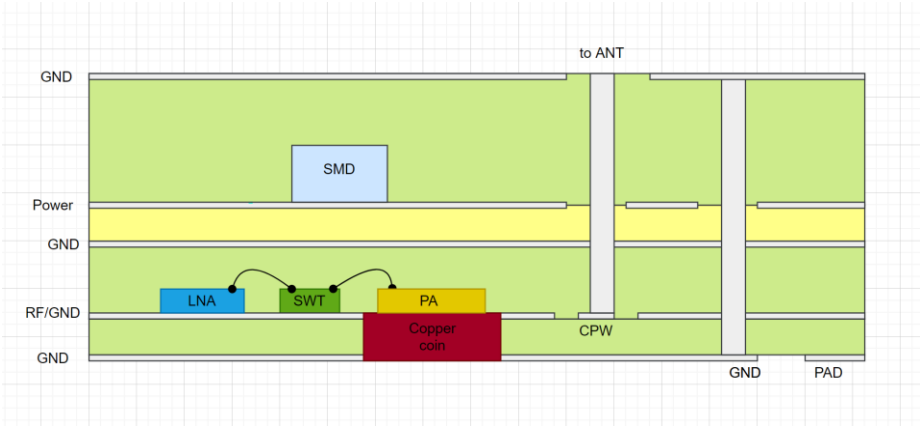


Figure 6 : Stack up for embedded die in PCB

The EM simulated S-parameters for the proposed package on the board are given below.

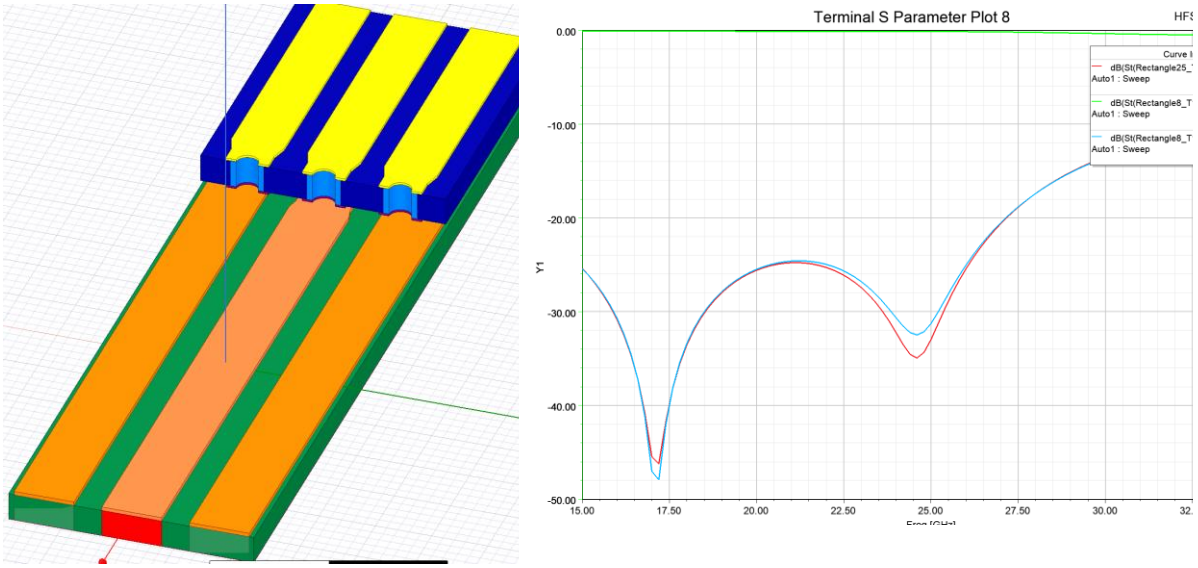


Figure 7 (a) part of package when connect to the main board (b) S parameter for mother board and package.

The final 3D package is based on implementing 4 front-end tiles integrated in one package. Half via pad method has been chosen for this package.

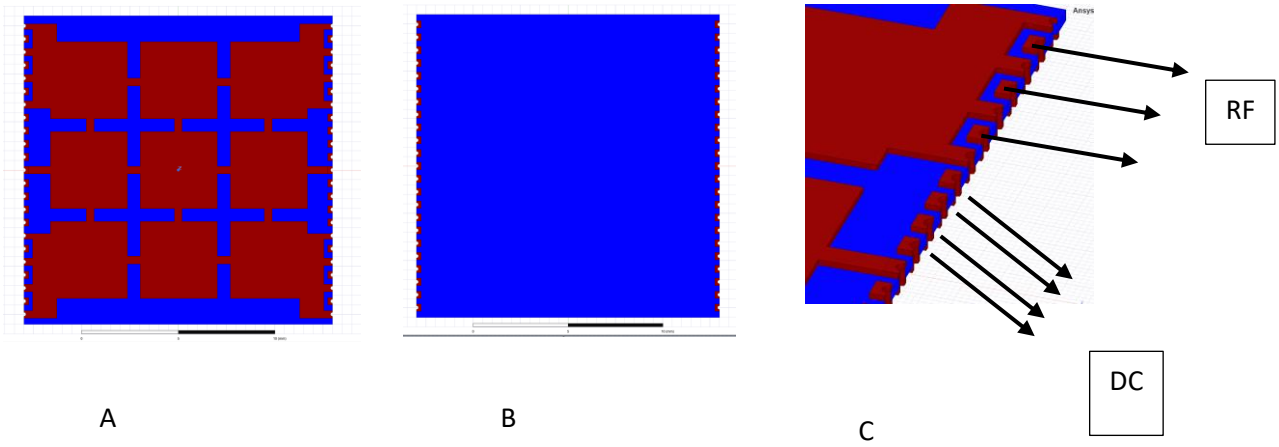


Figure 8 (A) Bottom view , (B)Top View , (c) Side view

Figure 8 shows the final package design. A is bottom view of package which grounds are defined for soldering purpose and thermal management as well.

B is the top view of the package which in this step still we didn't consider the RF out pads and array of antenna yet.

The C shows the side view of the package and the definition of each pads. Each tiles have 3 RF in pad and 5 ground pads with 4 DC pads.

Conclusion :

An embedded package for a phased array module with four transceiver front-ends has been developed and integrated. The thermal management was analysed with copper coin, copper via, silver epoxy and silver sinter. The most optimum thermal result was achieved with copper coin and silver sintering specially in higher power dissipations; however, the copper vias showed acceptable thermal performance. The on-package transmission line and the transition pad were also designed and modelled in HFSS to obtain a 50-ohm impedance matching up to Ka-band frequencies. The RF structure avoided the complexity while maintaining an excellent matching and loss performance.