How to Package mmWave MMICs

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Abstract

The mmWave frequency bands are increasingly used for high-volume commercial applications, including automotive radar, 5G, Fixed Wireless Access (FWA) and LEO satellites. This demand has driven the need to package mmWave ICs in low-cost surface-mount packages that are suitable for high-volume assembly, with low manufacturing costs and high yields.

Although mmWave SMT (Surface Mount Technology) packaged components resemble those used at lower frequencies, the packaging parasitics become much more significant at higher frequencies and their potential to cause serious performance degradation is greatly increased.

This paper provides an overview of mmWave SMT packaging technologies and aims to help engineers understand the issues and avoid the problems. It also provides an overview of how to optimise the performance of mmWave packaged ICs using a range of SMT packaging technologies, based on the author's practical experience. It will explore the problems that can be caused by packaging parasitics and will describe proven techniques for implementing high performance packaged mmWave ICs.

Introduction

There has been significant growth in the availability of SMT packaged mmWave components over recent years. This growth has obviously been driven by demand, in particular the demand for broadband wireless data, which has led directly to increased exploitation of the mmWave frequency bands.

Whilst the physical appearance of packaged mmWave ICs is often much the same as packaged RF ICs, the potential for the packaging parasitics to cause serious performance degradation is greatly increased. Appropriate packaging technologies and design and mitigation strategies must be adopted to achieve optimum performance for an SMT packaged IC operating at mmWave frequenices.

MmWave Packaging Options and Trends

The main SMT packaging approaches/technologies used at mmWave frequencies are summarised in Table 1. The frequency range column does not represent a hard limit, it is the range over which the technology approach is currently commonly used. Pushing the frequency of use beyond this is certainly possible, if challenging.

Style/Technology	Approximate Frequency Range	Comments
Over-moulded plastic	To ~ 40GHz	Custom leadframes often used for higher frequencies
Air-cavity plastic	To ~ 45GHz	Often uses custom leadframes
Laminate	To ~ 45GHz	Often custom designed for higher frequency use
Flip-chip wafer level chip scale packaging (WLCSP)	To ~ 100GHz	Package processing often added as final steps of IC processing
Multi-Chip Modules (MCMs)	> 100GHz	Bare die assembled with custom substrate
Antenna in Package (AiP)	> 100GHz	Very compact but very application specific

Table 1: Overview of mmWave packaging approaches

Over-moulded Packaging

The QFN (Quad Flat No-leads) style of package is the most commonly used for SMT packaged ICs operating at mmWave frequenices. It is popular in plastic-overmould, air cavity and laminate packaging technologies.

Figure 1 depicts a single-chip Front-End Module housed in an over-moulded 5mm x 5mm QFN package together with its evaluation PCB. This is a 28GHz component designed for 5G applications comprising a 3-stage PA with temperature compensated RF power detector, a 2-stage low current LNA and a transmit/receive switch with associated control logic [1].

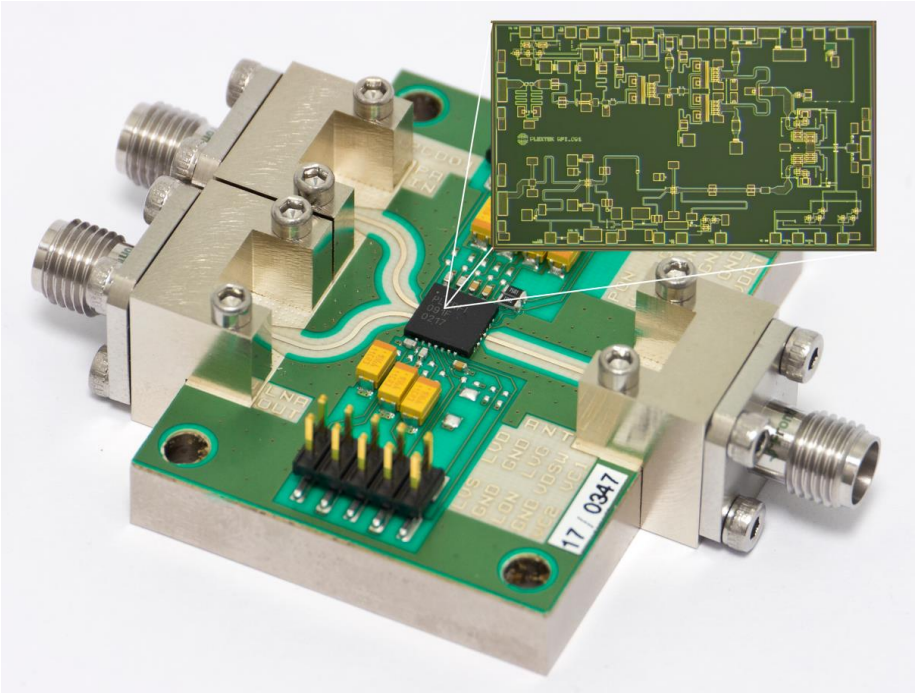

Figure 1: 28GHz single chip FEM in over-moulded SMT package on eval PCB

The packaged FEM in Figure 1 is able to provide very good performance at 28GHz whilst using a standard, low-cost, high volume overmoulded plastic assembly process. There are, however, careful design steps that need to be taken to achieve this.

Figure 2 shows a close in photograph of a 20 pin 5mm x 5mm over-moulded plastic QFN package plus an example die that has been packaged in this package style. The right image is the underside showing the package pads and the large, exposed paddle. The exposed paddle is normally attached to a PCB ground pad to provide low inductance ground connection and a good thermal contact.

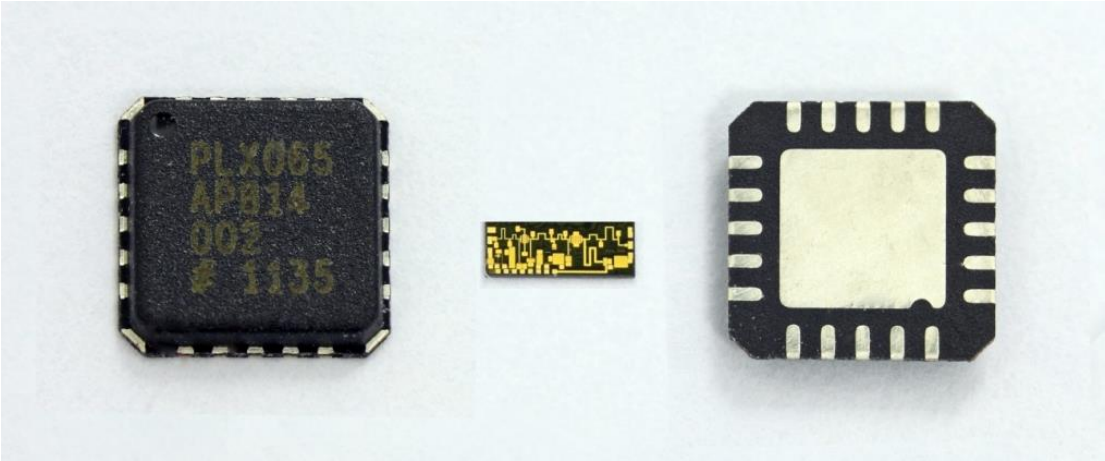

Figure 2: Plastic over-moulded 5mm x 5mm QFN-20 package

Figure 3 shows a standard “open-tooled” leadframe for a QFN-32 package. The square metal pad in the centre is the Die Attach Paddle (DAP). There are four corner ties that connect the DAP to the leadframe. The red outline in the centre image shows the approximate location of the edges of the package body. The blue outline on the right image depicts the approximate die edge. With a mmWave IC it is important that the RF ports are as close to the DAP edge as assembly rules allow to keep the bondwire lengths as short as possible. This obviously means that the packaging design and the IC design must be done together as a common engineering task.

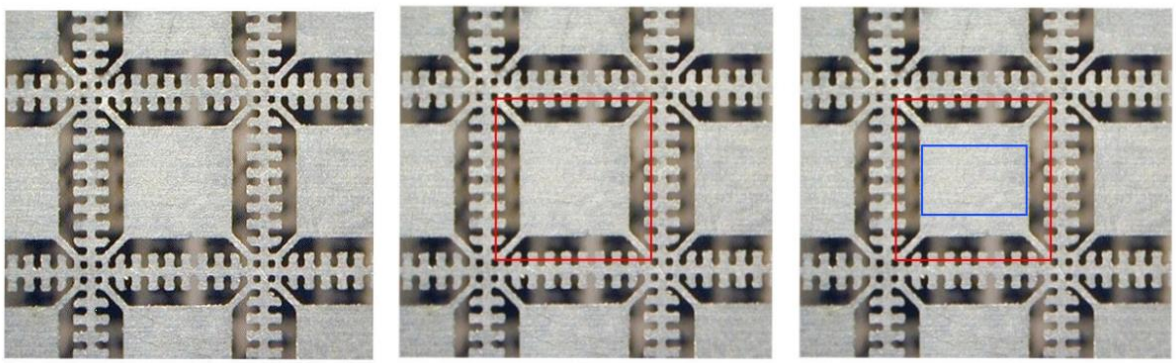

Figure 3: Standard leadframe for 20 pin 5mm x 5mm QFN, with annotation

Parasitic Effects of SMT Packaging

Packaging mmWave ICs will introduce parasitics that can degrade the performance. The key is to manage and mitigate these parasitics to optimise the performance of the packaged components. The main effects that will be encountered are:

- Dielectric loading (loss and permittivity)
- Grounding inductance of package and PCB and leadframe parasitics
- Series inductance of RF bonds
- Increased thermal resistance (and so junction temperature)

Dielectric Loading

Dielectric loading is not an issue in air cavity packages but in over-moulded packages the moulding compound is in contact with the IC and the impact of its permittivity and loss can affect RF performance. This can be mitigated by the use of a surface passivation on the IC as part of the IC processing. Passivation coatings such as PBO and BCB are available on many GaAs and GaN processes. The coatings are normally thick enough to cause the addition of moulding compound to have only modest impact. The passivation itself does degrade transistor performance slightly but the effect is normally included in the PDK (Process Design Kit). EM simulation of the IC including both passivation and moulding compound can be undertaken to simulate the performance of the packaged IC.

Grounding inductance

Grounding inductance can cause serious problems for microwave and mmWave ICs. The grounding inductance is made up of the IC ground contacts to the DAP, the die attach material, the DAP itself, the solder contacting the exposed paddle to the PCB and the PCB grounding inductance.

GaAs and GaN ICs normally include through substrate vias that provide low inductance contacts from the surface of the die to the backside. Si ICs may need to make use of down-bonds to provide ground contacts between the IC and the DAP. Flip-chip packaging (discussed later) can address this and provide an alternative means of making a low inductance ground contact.

The DAP itself is normally some form of copper alloy and as a solid metal connection it has low inductance. Similarly the die attach material and solder to attach the package to the PCB have a modest effect on grounding inductance.

It is actually the PCB inductance between the PCB pad for the exposed paddle and the PCB ground plane that can dominate the grounding inductance of an SMT packaged mmWave IC. Great care must be taken when mounting the packaged die on a PCB to keep this grounding inductance sufficiently low as excess grounding inductance can cause serious RF performance degradation and even instability. The impact of the grounding inductance increases with increasing gain and increasing frequency. Compensation of grounding inductance is not practical – it must be minimised and confirmed as low enough.

In order to determine if the grounding inductance is low enough an estimate must be made of how much grounding inductance can actually be tolerated. A simple approach to this has been used to come up with a working estimate:

- An ideal amplifier component is considered with 100dB return losses & 200dB isolation
- A variable grounding inductance is added to this amplifier and adjusted until the return losses are degraded from the near perfect starting point to the still very respectable 20dB.
- Examples cases for amplifiers gains of 10dB, 20dB and 30dB are evaluated

Figure 4 plots the results of this exercise. The maximum level of tolerable inductance plotted is a guideline rather than an absolute limit, but it clearly demonstrates that the grounding inductance needs to be smaller as frequency and gain increase. It also shows that mmWave amplifiers must have very low grounding inductance.

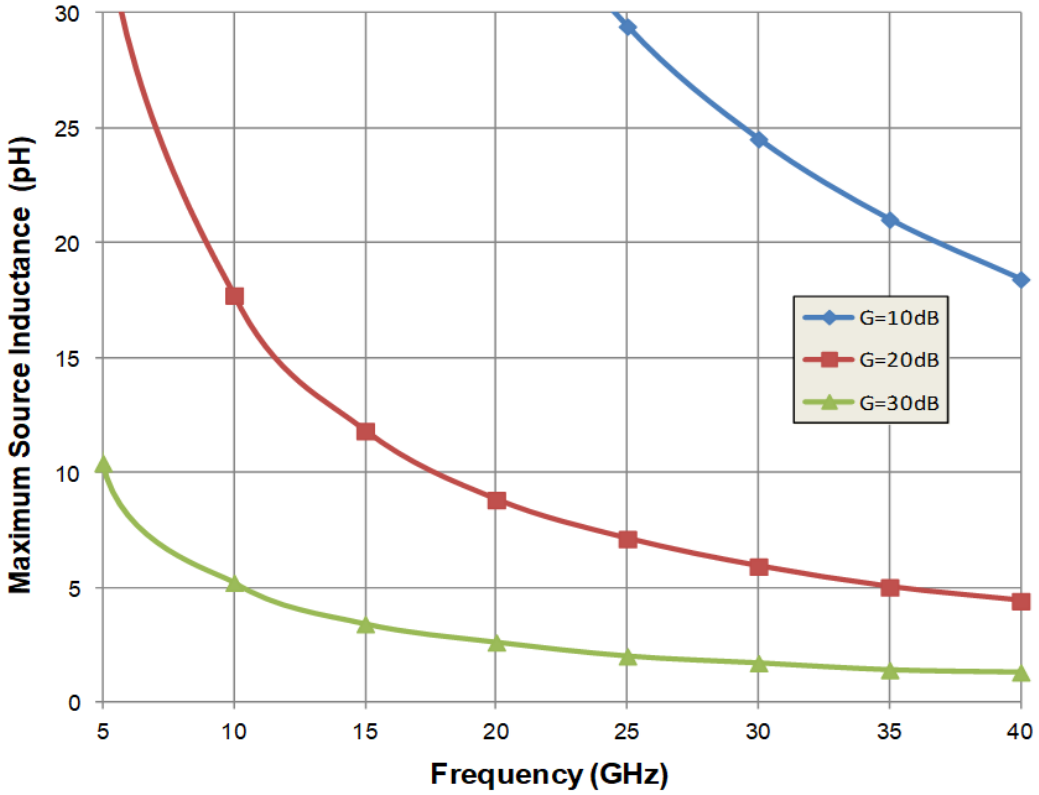

Figure 4: Approximate levels of tolerable ground inductance versus frequency

As mentioned above, the PCB onto which the SMT component is mounted will have a significant effect on the grounding inductance. The exposed paddle of the SMT package normally sits on an array of vias in the PCB. Using a thin PCB material reduces the inductance of these vias. Fortunately, a thin PCB material is preferred at mmWave frequencies to minimise dispersion[2] with an 0.008" thick substrate being a popular choice.

The number of vias used to ground the exposed paddle should be as large as practical with the PCB grounding pad extending beyond the package body. Figure 5 shows an example layout for a well-designed PCB for a mmWave SMT packaged IC. This is for a 26.5 to 29.5GHz amplifier with 21dB gain and a 1dB compressed output power of 25dBm (the CMX90A702 from CML). The package is a 4mm x 4mm QFN-20. The tightly packed array of vias under the exposed paddle area is clearly visible.

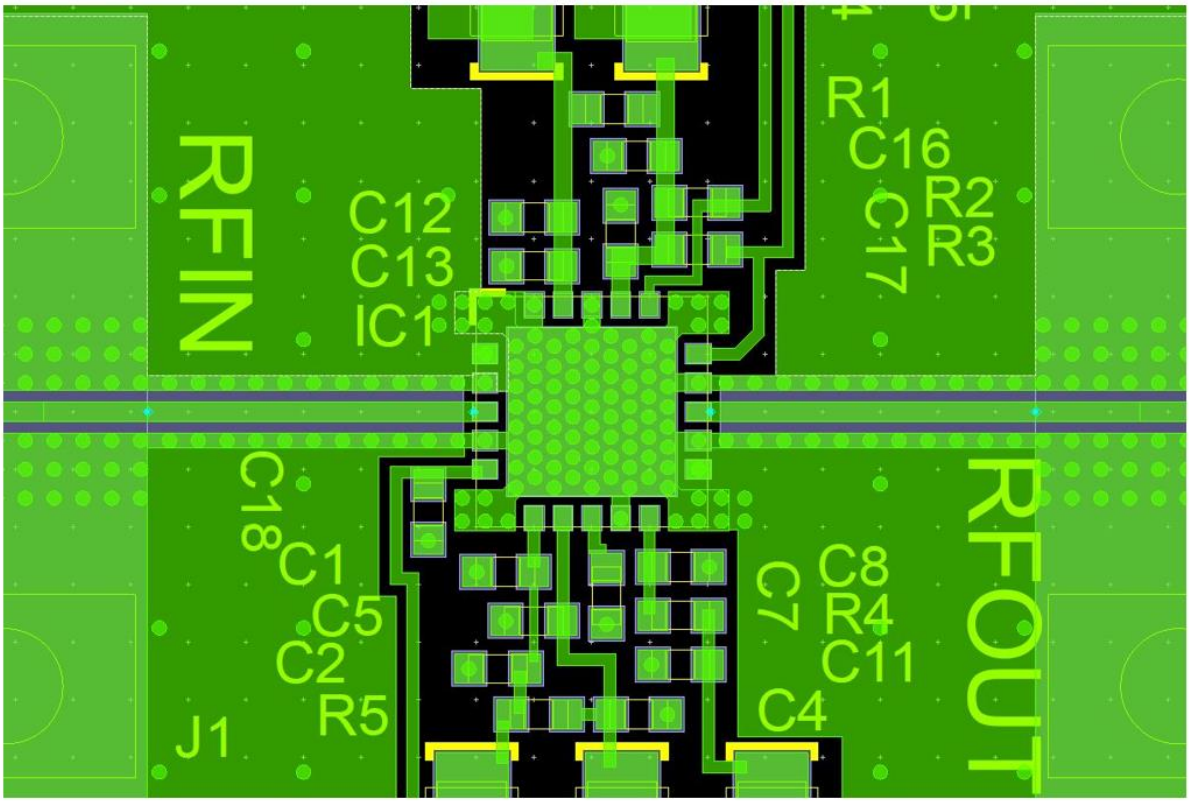

Figure 5: Example PCB layout with good RF grounding (courtesy of CML)

Series Bondwire Inductance

The impact of bondwire inductance increases with increasing frequency. Even an inductance of just 0.5nH has a reactance of 88Ω at 28GHz. It is possible to compensate for the inductive effect of a bondwire interconnect so long as the inductance doesn't become too large. The first step is to minimise inductance of the RF bond transition:

- Use multiple (2 or 3) parallel bondwires at each RF port
- Layout die to fit selected package lead-frame with minimum bond length at RF ports
- Work with assembly house on limits that set the minimum bond length; use reverse bonding; custom lead-frame

Figure 6 depicts 3 parallel bonds modelled in Keysight's ADS simulation tool. The total bond length is ~ 0.75mm. The bonds have been arranged in "V" configuration to minimise the inductance due to mutual coupling. The Smith Chart plot on the right-hand side shows the simulated input impedance of the bondwire link connected to ground. It can be seen that the inductance at 28GHz is ~ 0.21nH. Whilst this is certainly a low inductance, it still has a reactive impedance of ~ 37Ω at 28GHz.

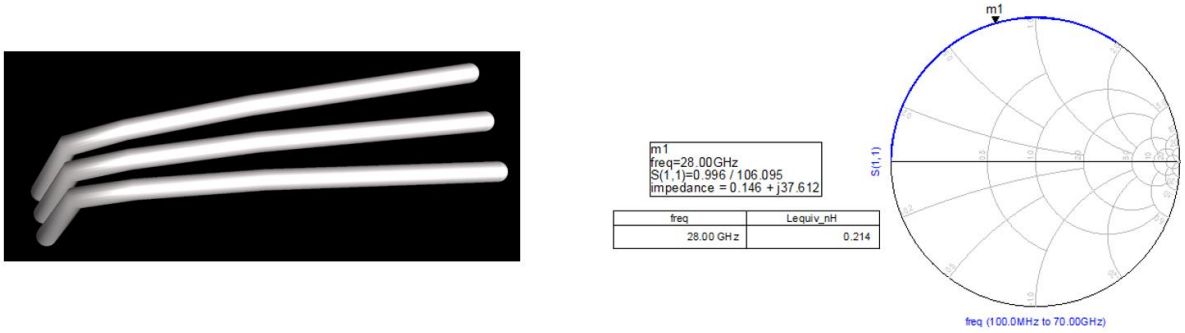

Figure 6: Simulated inductance of 3 short bonds

The s-parameters of the triple bond connection, as a two-port network, are plotted in Figure 7. It can be seen that the S11 rises above -15dB at just 12GHz and the insertion loss reaches 0.5dB at around 25GHz. It is difficult to see how the bond transition can be configured for lower inductance and based on this initial simulation the idea of implementing a wire bond transition that operates well to 40GHz can seem daunting.

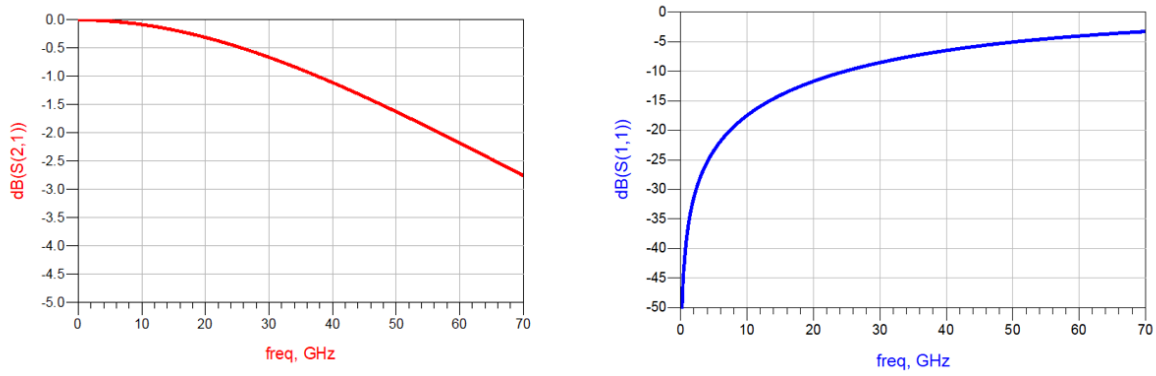

Figure 7: Simulated s-parameters of 3 short bonds as a series element

Fortunately it is possible to improve the RF performance of this bondwire transition without further reducing its inductance. The key is to add capacitive compensation at each end of the bondwire to form a C-L-C low pass filter. Figure 8 shows how the RF performance of the transition improves if the optimum value of shunt capacitance is added at each end. It can be seen that an excellent 50Ω transition in now obtained to 40GHz.

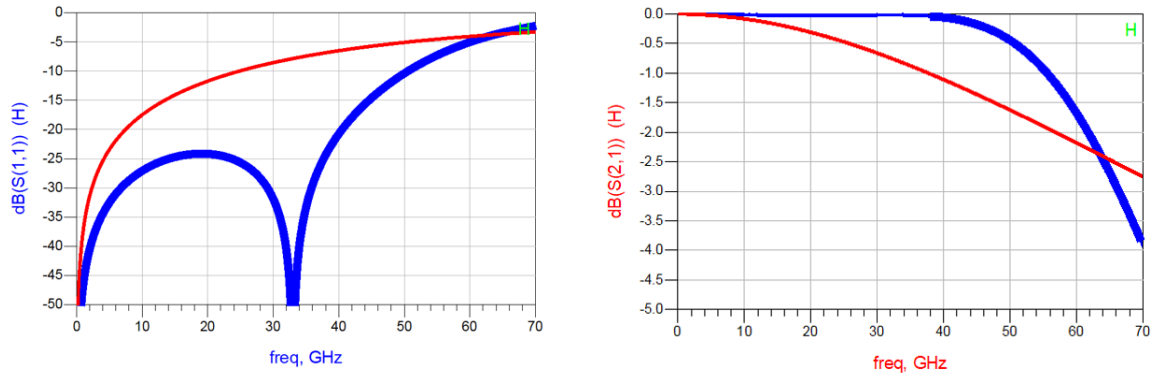

Figure 8: Effect of adding capacitive compensation to the 3 bondwire connection

The remaining question is how to implement this capacitance in practise. Fortunately the bondpad on the IC and the SMT package pad on the PCB both add capacitance to ground. The transition from IC to PCB should be simulated in full and practical adjustments made to obtain a transition offering good performance to the desired operating frequency.

For a given bondwire inductance there is an upper frequency to which this compensation approach can be used. This is the cut-off frequency of a third order low pass filter incorporating the inductance. The upper frequency to which an inductance can be ideally compensated is plotted against inductor value in Figure 9. For a given inductance, package transitions can be implemented that work well to a slightly higher frequency than that shown but perfect compensation is not possible beyond the frequencies indicated in Figure 9.

The key to implementing a good RF transition in a mmWave package is to minimise the series inductance first, then to accurately model the transition and then to compensate for the inductance and optimise the performance.

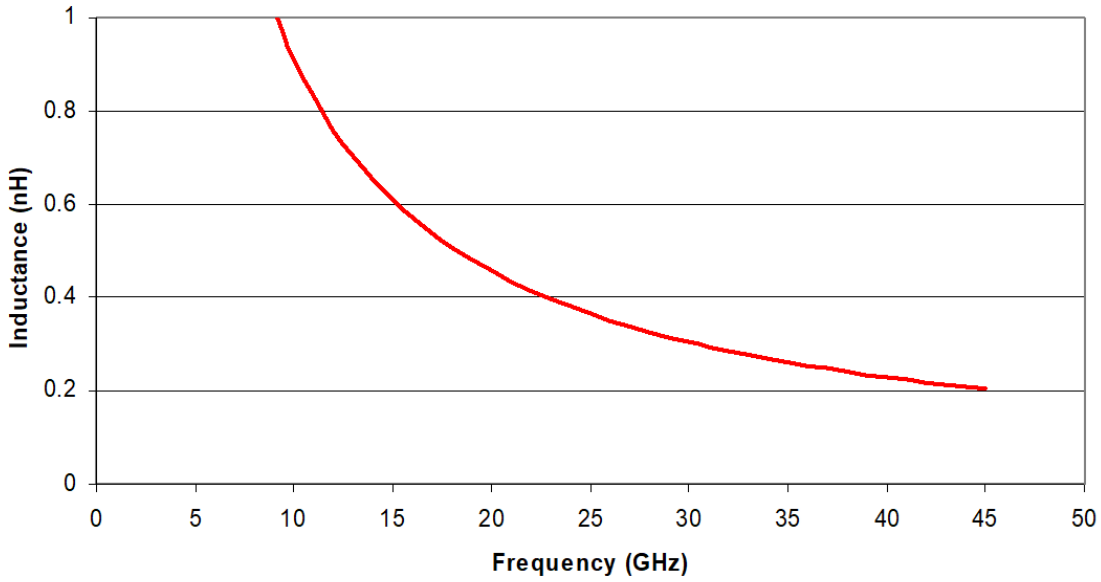

Figure 9: Maximum inductance that can be perfectly compensated versus frequency

Two examples of custom leadframes designed to optimise the performance of a mmWave package are shown in Figure 10. The left-hand image is an X-ray of a 28GHz amplifier designed by PRFI [3] assembled on to its evaluation PCB. Fused pins connecting some of the SMT pads to the DAP can be seen. This is done either side of the RF pads at input and output to provide a ground-signal-ground transition. The right-hand image is from a publication by Endwave [4]. This is an image of the leadframe and pins fused to the DAP are again clearly visible. An enlarged section at the RF input and output pins has been introduced. This will allow multiple bonds to be spread a little more widely and will also add some shunt capacitance. It can also be seen that the use of multiple pins fused to the DAP has allowed the corner ties to be avoided, which will reduce any risk of physical resonances due to these structures.

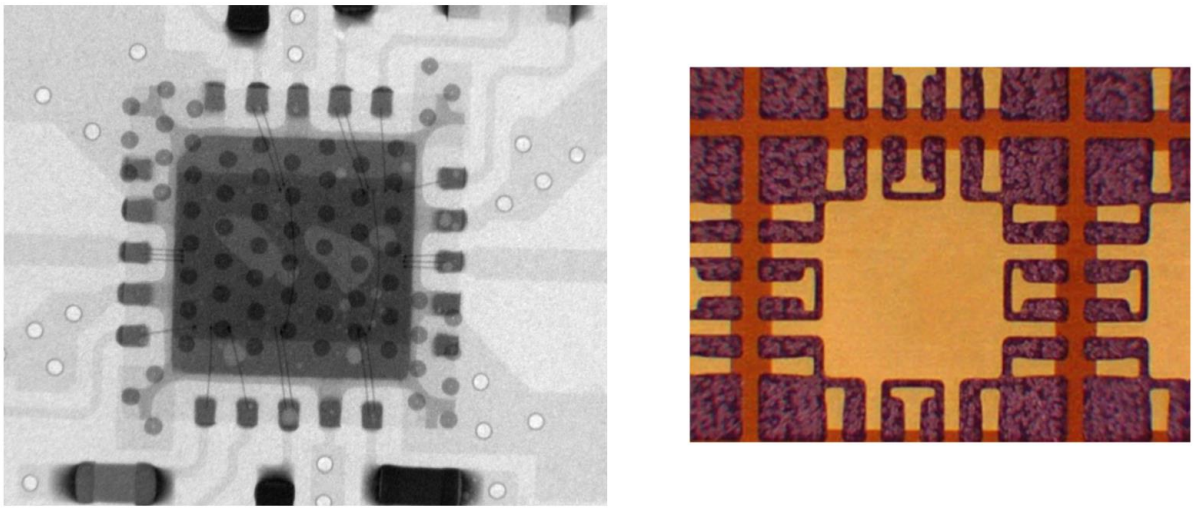

Figure 10: Examples of custom leadframes for improved mmWave performance

Thermal Effects of SMT Packaging

The higher the junction temperature of a transistor the lower its median lifetime. RF performance of transistors also tends to degrade with increasing junction temperature. IC designers need to consider the expected junction temperature for the range of ambient temperatures over which the IC needs to operate. It is important to ensure that the junction temperature (T_j) is low enough to ensure an acceptable lifetime and good RF performance.

The T_j that a transistor will reach is dependent on the IC process, the dissipated power and the junction to ambient thermal resistance ($R_{\Theta JA}$). The higher the thermal resistance the hotter the transistor. For most commercially available ICs the datasheet specifies the junction to case thermal resistance ($R_{\Theta JC}$). For a QFN package this is the thermal resistance between the junction and the exposed paddle on the underside of the package.

$R_{\Theta JC}$ is the sum of all thermal resistances from the junction to the package case. The packaging adds to this because of the thermal resistance of the die attach material and the package itself. The thermal resistance of QFN packages is relatively low because of the solid copper (alloy) lead-frame to which the die is attached. Custom lead-frames with pads fused to the die attached lead-frame can help reduce thermal impedance of the package.

Most SMT packaging uses some form of conductive epoxy or sintering paste to attach the die to the DAP. There are a wide range of products available with thermal conductance varying from very low to very high. It is important to work with the assembly house to select an epoxy that not only provides a low enough thermal resistance but is also suitable for attachment of the die to the DAP in terms of its coefficient of thermal expansion and its flexibility (a material with lower Young's modulus will provide some compliance to better cope with differing thermal expansion rates between the DAP and the die).

IC vendors typically provide information on the junction to case thermal resistance and leave the impact of the PCB and mechanics for the user to determine. With SMT components the impact of the PCB on the overall thermal resistance can be very significant. Having an array of vias beneath the DAP helps with this and the use of copper filled vias can further reduce the impact of the PCB on the total $R_{\Theta JA.}$

Air Cavity Packages

As the name implies, air cavity packages do not have an overmould compound in direct contact with the die, they are designed to include a cavity above the die that avoids the loading impact of the overmould compound. Air cavity packages are available as standard “open-tooled” designs but can also be custom designed for the specific needs of the user, in this case tooling charges would be incurred. Air cavity packages tend to have a slightly smaller DAP area than an over-moulded package of the same body dimensions as the package wall must be self-supporting prior to lidding. A photograph of a 39GHz PA in a 5mm x 5mm air cavity plastic QFN package is shown in Figure 11 along with the associated evaluation PCB.

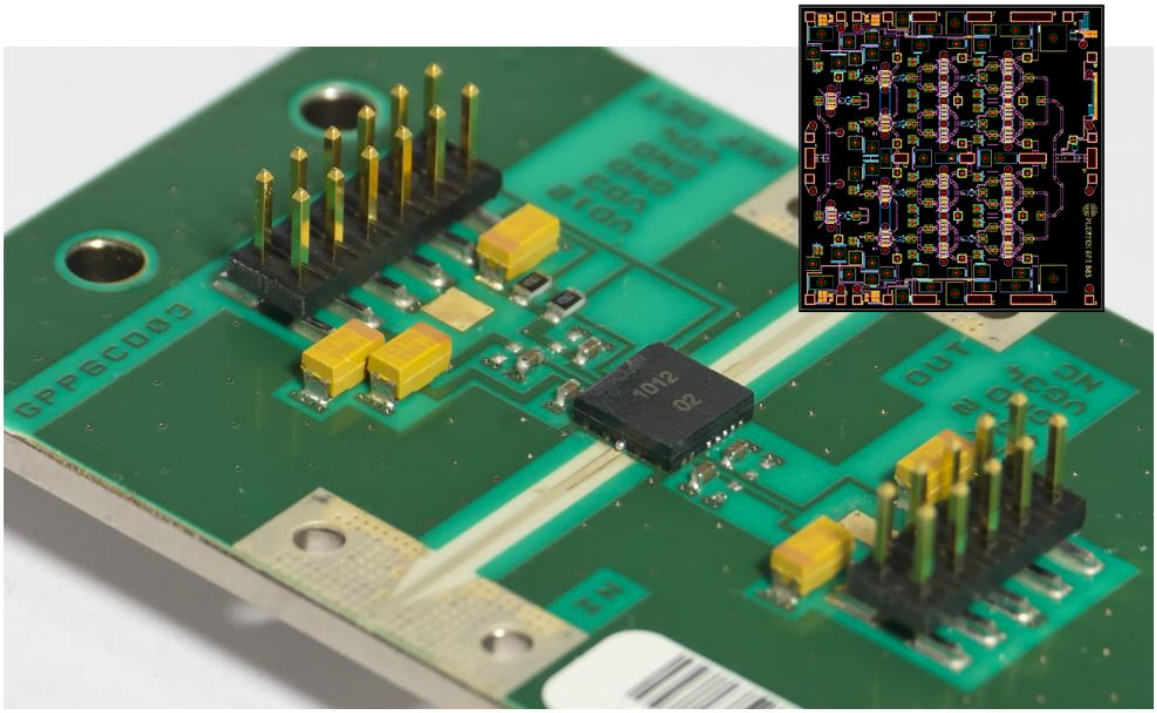

Figure 11: Photograph of a 39GHz PA in a 5mm x 5mm air cavity QFN with eval PCB

Laminate SMT Packages

Laminate packages are typically manufactured from the same PCB materials as many mmWave PCBs, including the evaluation PCBs shown above. One of their key advantages is flexibility of package design at a relatively modest cost. Figure 12 shows a photograph of a 26GHz FEM in a 10mm x 10mm custom laminate SMT package [5] on the left hand side with the evaluation PCB on to which it was mounted on the right hand side. The FEM includes 3 commercially available die: A Power Amplifier (PA) at the top left, a PIN diode switch MMIC at the centre right and a Low Noise Amplifier (LNA) MMIC below the switch.

The die in the FEM of Figure 12 are mounted on to a metal base through apertures in the laminate. This provides low electrical inductance and a good thermal path. The package also includes integral filter structures printed during package manufacture. At the output of the PA is a high-pass harmonic rejection filter and at the output of the LNA there is a coupled line band-pass filter which has been meandered to make it more compact. Copper filled through laminate via holes are used to connect frontside circuitry to the SMT pads on the underside of the package.

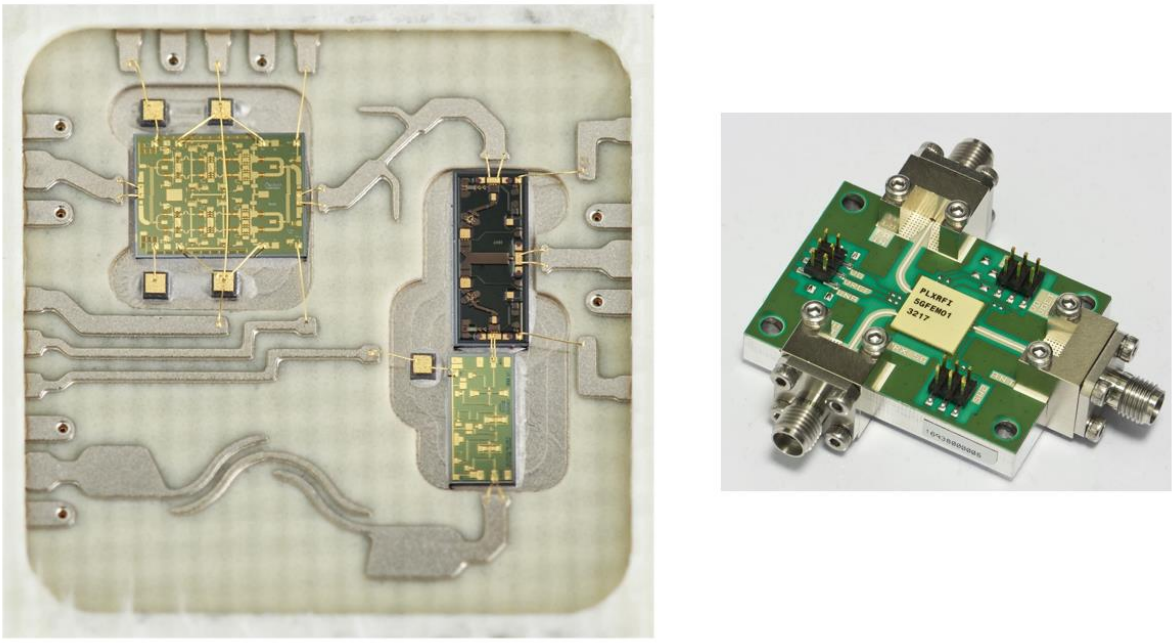

Figure 12: Photograph of 26GHz FEM in 10mm x 10mm custom laminate SMT package

Another example of a custom laminate mmWave SMT package is shown in Figure 13. This is a dual channel 26GHz amplifier designed for 5G applications In the 26GHz European "Pioneer Band [6]. Ground-signal-ground routing can be seen at the RF ports.

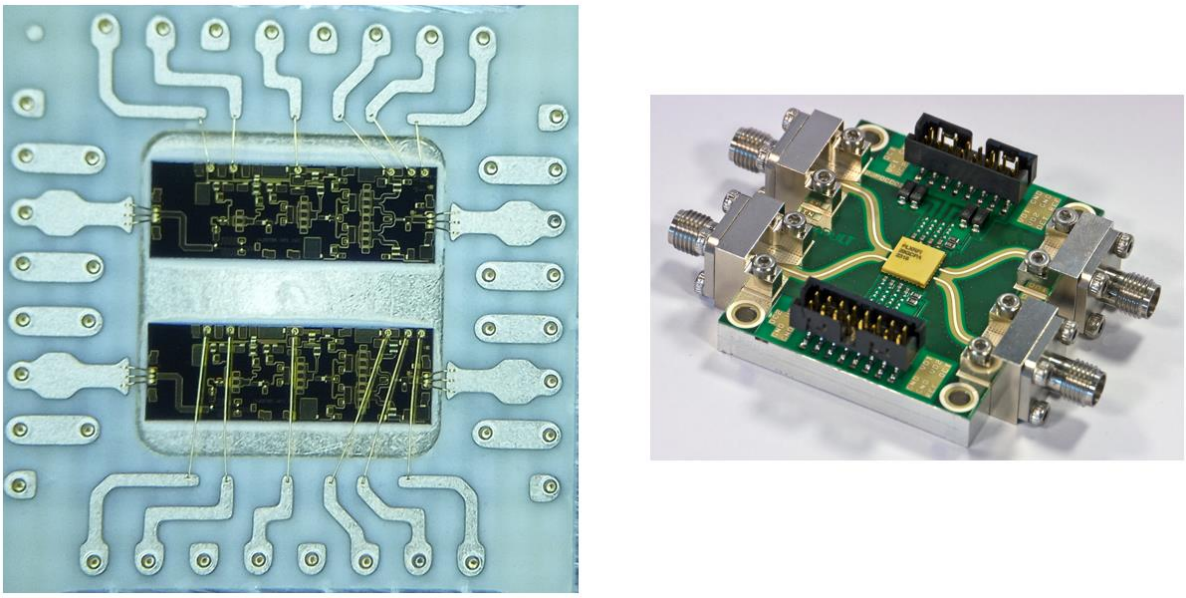

Figure 13: Photograph of a laminate packaged dual channel 26GHz PA

MMWave Multi-Chip Modules (MCMs)

An MCM includes multiple die, often single function components such as amplifiers, mixers or switches, interconnected to form a multi-function module. Figure 14 shows a photograph of a

mmWave MCM with die mounted on the surface of the PCB. This provides a low-cost approach to implementing mmWave MCMs. RF routing can be implemented on the surface of the PCB or on separate interconnect pieces designed to bring the surface of the RF routing pieces to the same level as the die surface and so reduce bonding inductance. Direct die to die bonding can also be used.

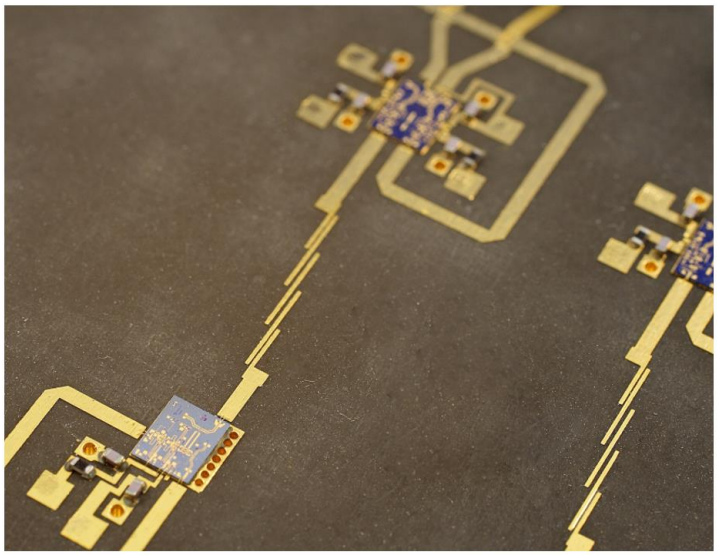

Figure 14: MMWave MCM with die mounted on the surface of a PCB

Antenna In Package ICs

At high mmWave frequencies the physical size of a wavelength becomes short enough to allow the possibility of including antenna structures as an integral part of the package. This removes the need to provide RF transitions to a PCB. Figure 15 shows an impressive demonstration of this approach. It is a W-band phased array transceiver from IBM [7]. Four 16-element transceiver ICs are integrated into a single package containing a total of 64 radiating elements. The spacing between the elements is $\lambda/2$ at 94GHz (around 1.6mm). The spacing from antenna elements to the side of the package is $\lambda/4$, which facilitates the tiling of multiple components to realize a larger array. The design targets radar and active imaging applications where small size and low weight are required.

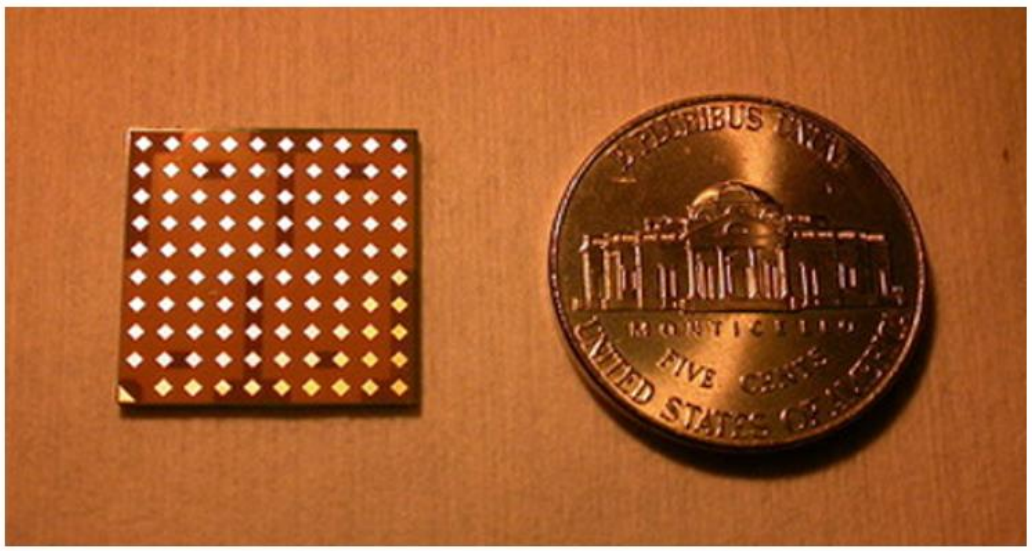

Figure 15: AiP package containing 4 transceiver die (64 radiating elements)

Figure 16 also shows a photograph of one of the 16-element die. It contains 32 receive channels (to facilitate simultaneous reception in two polarizations) and 16 transmit channels (which can be switched to either polarization).

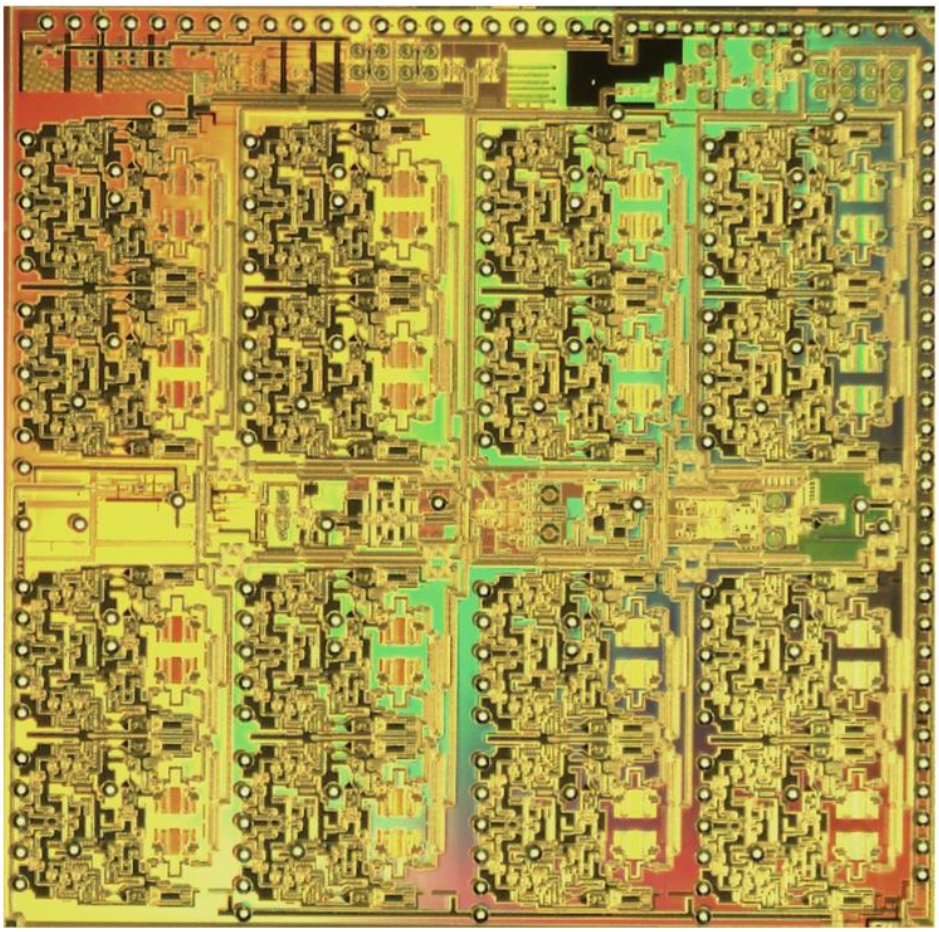

Figure 16: W-band phased array transceiver – courtesy of IBM

Flip Chip Wafer Level Chip Scale Packaging (WLCSP)

Wafer Level Chip Scale Packaging (WLSP) normally uses a ball grid array on the underside of the package for attachment to the PCB. The die is assembled within the package with its surface facing downwards towards the package contacts and ultimately the PCB on to which it will be mounted. This approach results in a package that is truly chip scale, being not much larger than the die itself. It also means that the interconnect parasitics can be very low. WLCSP is often undertaken as an augmentation to the wafer fabrication process.

A number of manufacturers have WLCSP processes such as Infineon's embedded Wafer Level Ball Grid Array (eWLB) technology [12]. Sumitomo has demonstrated a set of E-band ICs in WLCSP [14]. These include a frequency tripler, an LNA, a balanced mixer and a Power Amplifier (PA). The packaging technology is depicted in Figure 17, which shows a WLCSP evaluation PCB (LHS) and a process cross-section (RHS).

The process technology for the ICs of Figure 17 is GaAs PHEMT with additional processing steps added to form the WLCSP. This WLCSP processing includes the ability to add routing to connect to a uniform

array of solder balls for SMT attach. The surface of the IC package is covered with a common ground metal, which has multiple links to the die ground. Openings are made in the package ground plane for signal, control and bias connections to the die.

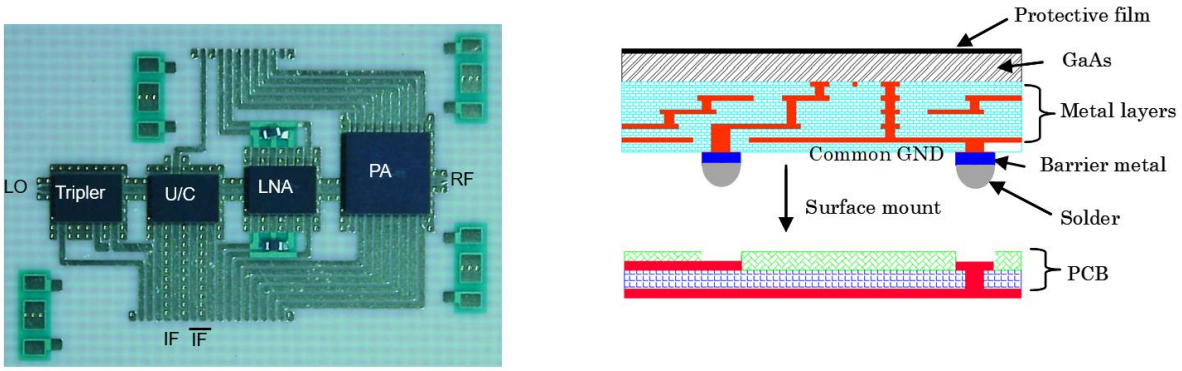

Figure 17: WLCSP evaluation PCB (LHS) and process cross-section (RHS) – courtesy Sumitomo

Conclusions and Summary

This paper has provided an overview of packaging options for mmWave ICs together with some guidelines for optimising performance and avoiding problems.

The most commonly used microwave and mmWave SMT packaging technology is over-moulded plastic, in particular QFN style packages. With careful co-design of package and IC this approach can be used to frequencies of around 40GHz. Air cavity packages avoid the effects of plastic loading and help push the upper operating frequency higher

It is important to provide good low inductance grounding for mmWave ICs and the importance of this increases with increasing gain and frequency. The design of the PCB on to which the package is mounted will heavily impact the grounding inductance and must be considered carefully by both the end user and the IC designer.

The inductance of the RF bonds is possibly the most obvious packaging parasitic. For mmWave use this inductance should be minimised; the approach to do this has been discussed. It is also possible to compensate for the inductance so long as it is sufficiently low for the maximum intended operating frequency. Techniques to implement this compensation have been presented and the importance of modelling the RF transitions to allow optimisation have been discussed.

WLCSP facilitates miniaturisation and helps reduce package parasitics and can extend the upper operating frequencies of SMT packaged ICs.

Antenna in Package technology can offer very compact solutions at high mmWave frequencies but it is very application specific

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