Optimum N-way Power Divider Using Klopfenstein's Taper

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***Abstract* — A proposed eight-way corporate power divider uses Klopfenstein's taper to provide optimum equal-ripple input match from a specified lower frequency, with the shortest possible length. The divider is realized in PolyStrata® micro-coax, operates from 2 GHz to 42 GHz, with 1.5 dB maximum loss in a 1-inch diameter radial divider SMT footprint and is capable of ten-watt CW input with some measure of graceful degradation. The described technique can be used in all N-way wired divider or combiner designs.**

***Keywords* — Passive circuits, combiner, divider, Wilkinson, Klopfenstein, taper, solid-state power amplifier.**

I. INTRODUCTION

The terms *power dividers* and *power combiners* may be used interchangeably, in this paper we will refer to the proposed network and others as *dividers*. Dividers are a key component of solid-state power amplifiers and are also used in other applications such as antenna feeds. Key requirements often include minimizing insertion loss and size. Isolation is also important in SSPA applications, typically provided by isolation resistors first described by Wilkinson[1].

Divider configurations can be radial, in-line[1], or H-tree. Radial dividers have low routing losses, where N ports combine into a single node. Wired radial dividers have inherently low loss because path lengths are short, but the designer must deal with matching to impedances of $\frac{Z_0}{N}$ [2]. A new class of radial divider has been introduced that combines amplifier assemblies using input and output antennas to form antipodal antenna arrays inside a coaxial waveguide; the "Spatium® combiner" features very low loss and wide bandwidth[3] but is relatively large in size. Planar, in-line dividers often use corporate Wilkinson two-way dividers matched to Z0 at input/output nodes. Planar H-tree dividers used in antenna arrays are usually cascaded two-way dividers which may be Wilkinson or reactive. Direct, N-way Wilkinson dividers above N=2 ideally require star resistors and non-planar connections.

This effort presents a modified corporate Wilkinson divider, configured into a compact radial format (see Figure 1). The combiner fits within ~1 inch circle (25.6mm) and measures just 21.6mm x21.6mm when fabricated on a multi-up panel (see Figure 2). The proposed design technique could also be applied to arbitrary N-way configurations including in-line or H-tree.

Our divider is similar to a planar, corporate two-way Wilkinson cascade but no position inside the divider is matched to 50 ohms; the *entire network* is a gradual impedance transformer. Due to layout constraints the design does not allow resistors at every possible node that could be isolated, so isolation and split-port return loss require some minor compromises.

Klopfenstein published a paper[4] in 1956 on a network that he called the Dolph-Tchebycheff taper, which is the shortest-length equal-ripple transformer to match to a given lower frequency, with no bound on upper frequency beyond media limitations. An N-way corporate divider, in the common mode, can be considered as an impedance transformer. The proposed divider is based on performing the impedance transformation with Klopfenstein's taper but could employ other impedance transformation solutions as well.

Ours is not the first effort to use a taper in a power divider. Yau showed a five-way straight-line direct network[5]. A more recent effort by Miralles[6] showed a tapered two-way Wilkinson design technique. However, we have added degrees of freedom to the design so that none of the section impedances are unusually high or low, and we have provided the ability to route the divider arbitrarily while maintaining minimum length for a given lower frequency cut-off.

Figure 1. Full 3D layout of proposed eight-way divider

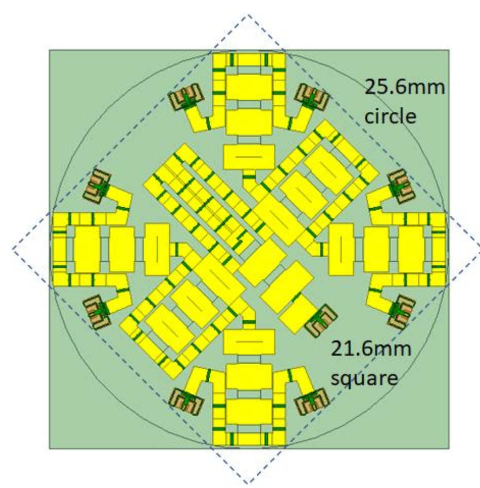

Figure 2. Eight-way combiner footprint dimensions

[1] Common port on one side, divided ports all on opposite side

A. *PolyStrata technology*

PolyStrata® technology is 3D microfabricated media employing pure copper conductors and predominantly air dielectric that can form the lowest-loss transmission line at millimeter-wave frequencies. Typically configured as rectangular coax, the technology was first published in 2008[7], as part of the DARPA 3D-MERFS program. In one extreme example, PolyStrata media was used to fabricate a 1:4096 power divider to drive a D-band antenna array[8].

In all additive technologies, cost is inverse to signal attenuation. Taller coax results in lower loss but takes more time to fabricate. We used a cross-section of 800 x 600µm air box, where 50 ohms is sized at 200x279µm center-conductor. Coax height including top and bottom wall thickness is 800µm. Transmission line attenuation in this configuration is 6.3dB/m at 10 GHz; divider loss could be reduced with a larger coax cross-section. PolyStrata coax typically has effective dielectric constant of 1.05, due to dielectric support material.

II. DESIGN

B. *Linear model development*

The proposed eight-way divider starts as a taper design, from 50 ohms (Z_0) to 400 ohms ($8xZ_0$). Total length is 63.5mm, which was chosen for lower frequency of 2 GHz, maximum VSWR of 1.3:1 and DK of 1.05. The taper was segmented into 37 sections, all are 1716µm long, or 45 degrees at center frequency (21.5 GHz). Section impedances vary as shown in Figure 3 and were computed with a free Excel spreadsheet download available on Microwaves101.com[9].

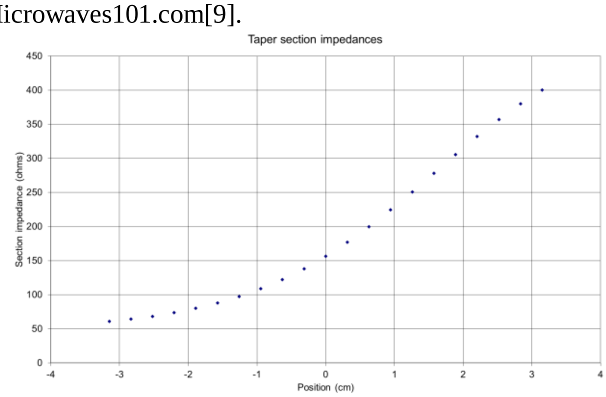

Figure 3. Segment impedances in 50-ohm to 400-ohm taper

Return loss of the linear model taper is shown in Figure 4. This illustrates the beauty of the Klopfenstein taper, it behaves as a high-pass structure with equal-ripple in reflection coefficient. The loss of the taper is also shown at 0.91 dB at 42 GHz, using a global value of 6.3dB/m at 10 GHz for all sections regardless of impedance, scaled at SQRT(frequency).

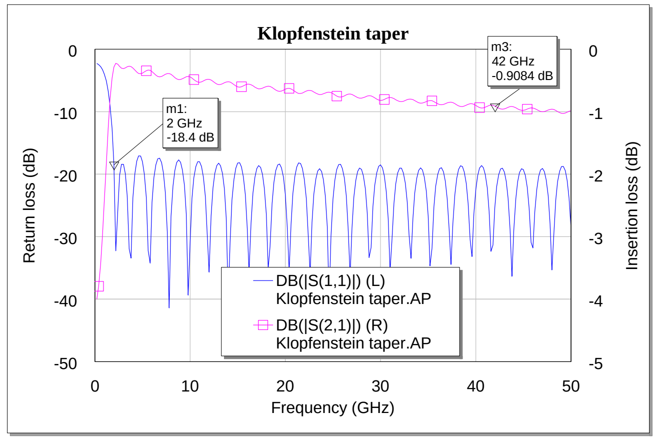

Figure 4. Return loss and insertion loss of 50-ohm to 400-ohm taper

Next, a linear model of the eight-way, nine-port network is built up from eight of the tapers, as show in Figure 5. Note the highest impedance of 345 ohms at the combined port P1.

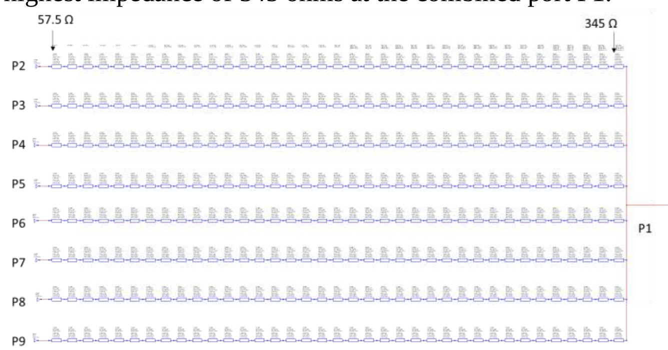

Figure 5. Eight-way schematic, prior to parallel combining

The schematic is reduced by parallel-combining any transmission lines that have greater than 80 ohms impedance and inserting isolation resistors at quarter-wave spacing where the layout affords opportunities. This is shown in in Figure 6.

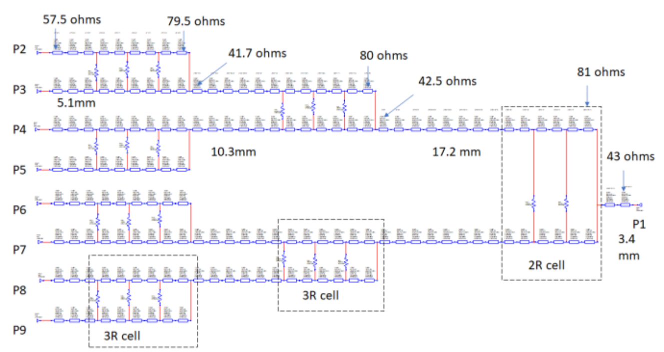

Figure 6. Eight-way divider network after parallel combining and addition of isolation resistors

Schematic reduction is done in conjunction with a sketch of the desired configuration, as shown in Figure 7. We targeted a radial design that would fit well within a 1.5-inch diameter circuit card assembly. The 2R and 3R cells signify where the layout affords opportunities for isolation resistors, while the interconnect lines between them are singular transmission lines of less than 80 ohms impedance.

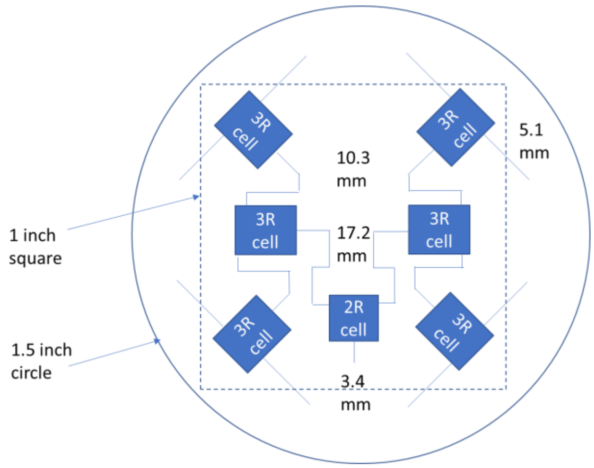

Figure 7. Sketch of the divider prior to detailed design

Next, isolation resistors are optimized within the linear model, to obtain good split-port match in odd-mode, and good isolations. We found a global value of 133 ohms worked well. Of interest is the effect on split port (odd mode) match, prior to parallel combining, after combining, and finally after incorporation of resistors, as shown in Figure 8. Without combining any lines or adding resistors, return loss would be 2.2 dB (the match looking into 50/8=6.25 ohms). That loss is slightly improved by attenuation of the network (brown trace). When lines are combined, variations in return loss crop up (blue trace). Finally, when 133-ohm isolation resistors are added, return loss is better than 10 dB everywhere but the top end of the band (purple trace). In the even mode, if the network is used as a combiner fed from eight MMIC amplifiers, each amplifier would see good impedance match even without isolation resistors. However, such a reactive network would be incapable of any measure of graceful degradation.

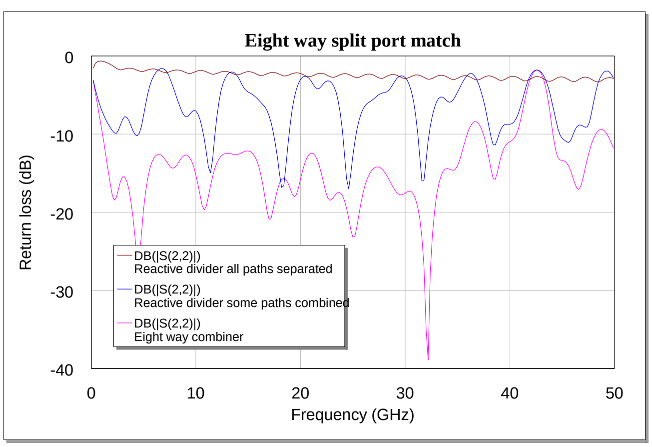

Figure 8. Split port match, three cases

C. *Graceful degradation*

We analysed the divider for 10W CW power input with a simulated amplifier failure causing high VSWR and unknown phase. Figure 9 shows dissipations for three resistors closest to the failed amplifier, with reflection phase swept 0 to 315 degrees in 45-degree steps. Worst case dissipation is 0.5 watts, which could be handled with aluminum nitride, beryllium oxide or diamond resistors. In this study we used alumina resistors rated at 100 mW which would not survive an amplifier failure at 10W input, due to supply chain issues for higher power handling components. Ignoring graceful degradation and used as a power combiner, the design is capable of handling 10s of watts but would be limited only by the designer's choice output connector.

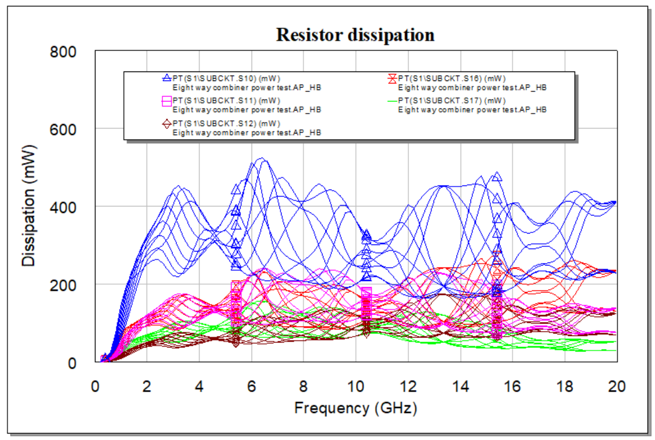

Figure 9. Resistor dissipations with one failed amplifier, 10W input

D. *Detailed Full-Wave Design*

Detailed design was done using Ansoft's HFSS environment. Initial work was done on the 2R and 3R sections. Objectives of this work were to compact the designs as much as possible, and to absorb all parasitics associated with the design so that they would behave as close as possible to the original linear model. A view of a 3R section is shown in Figure 10. Resistors are 0201 size (0.6 x 0.3mm), mounted as flip-chips to minimize inductance. The center-conductors they attach to are supported underneath by semi-insulating silicon carbide chocks. These chocks normally remove center-conductor heat due to surface resistivity of the transmission lines. In the case of an amplifier failure or other out-of-balance situation, the chocks also serve to guide isolation resistor heat to the divider's overall copper structure. Widths of the lines that span dielectric supports must be reduced to compensate for added capacitance of the supports, to maintain desired impedances.

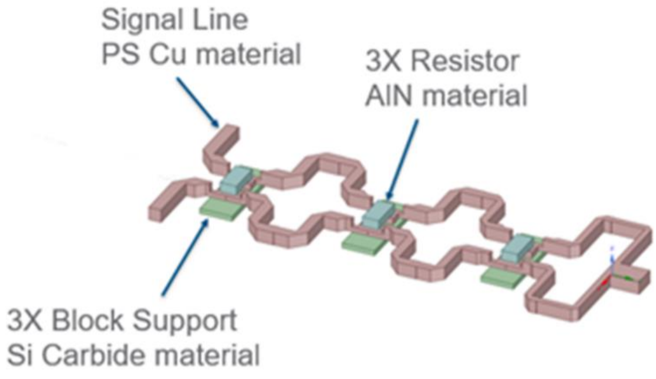

Figure 10. 3R section model in HFSS showing X-ray view

Next, the full-wave wight-way divider model was built up. Again, bends and parasitics were absorbed as well as possible into the design. A physical view of the finished divider is shown in Figure 1.

The final predicted insertion loss is shown in Figure 11. Subtracting 9.03 ideal loss, the result is 1.35 dB loss at 40 GHz. This is greater than the linear prediction, in part due to metal removal to compensate for silicon-carbide chocks. It also takes into account gold/silver plating to passivate the bare copper (4E7 S/m used for bulk conductivity).

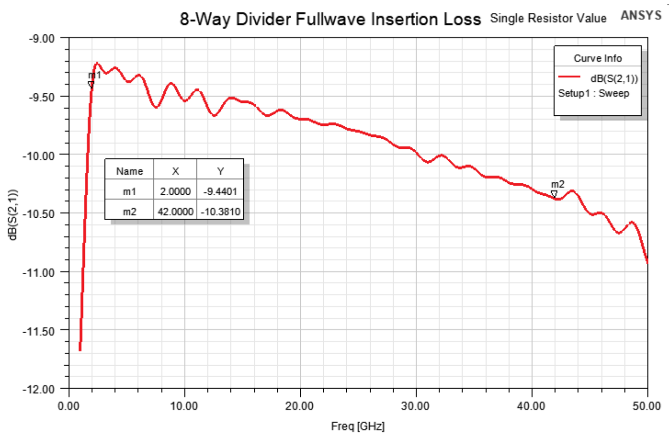

Figure 11. Full-wave prediction of divider loss

Final predictions of the return losses are shown in Figure 12. S11 is the common port (red trace). Due to layout effects, it no longer presents an equal-ripple response, but it shows -15 dB match across most of 2 to 50 GHz. The split port match (S22, blue trace), is similar to the linear model response and is better than 10 dB from 2 to 40 GHz

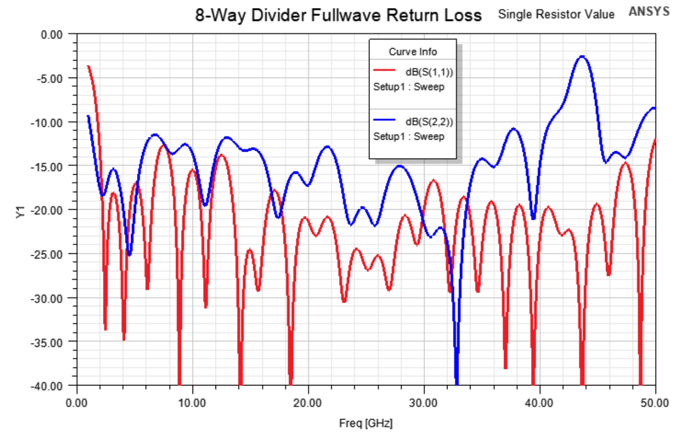

Figure 12. Full-wave HFSS return loss result.

Final isolations are shown in Figure 13. The red line is for adjacent ports, where isolation is at a minimum. The design provides 10 dB isolation or better except at band edges.

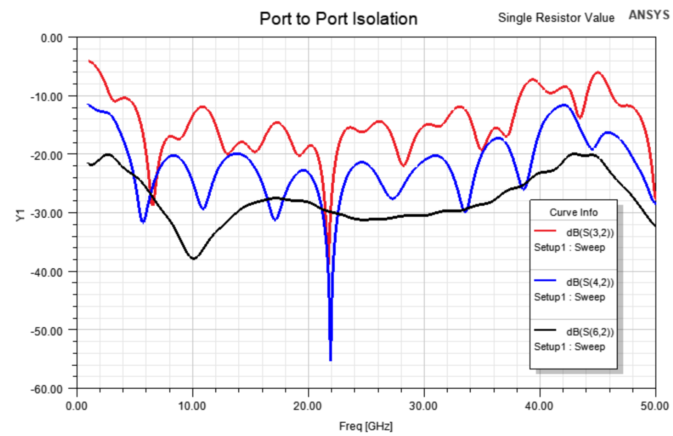

Figure 13. Full-wave prediction of divider isolations

E. RF transition

The divider design requires ground-signal-ground (GSG) interconnects be surface mountable. The transition was separately designed and developed using HFSS. and is shown in Figure 14. A pair of transitions adds 0.3 dB loss at 42 GHz to the overall design, as shown in Figure 15.

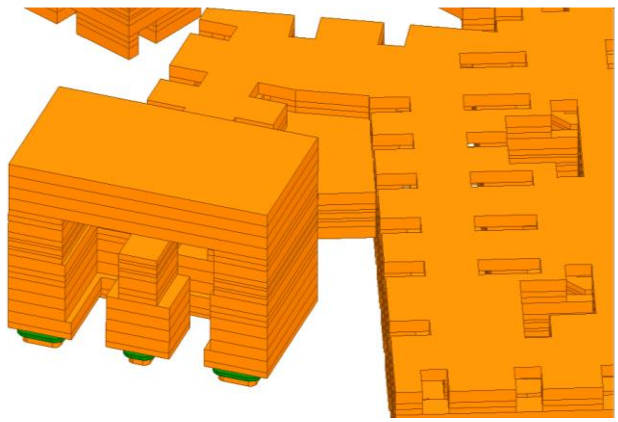

Figure 14. Details of SMT RF transition

Figure 15. Full-wave simulated performance of single RF transition

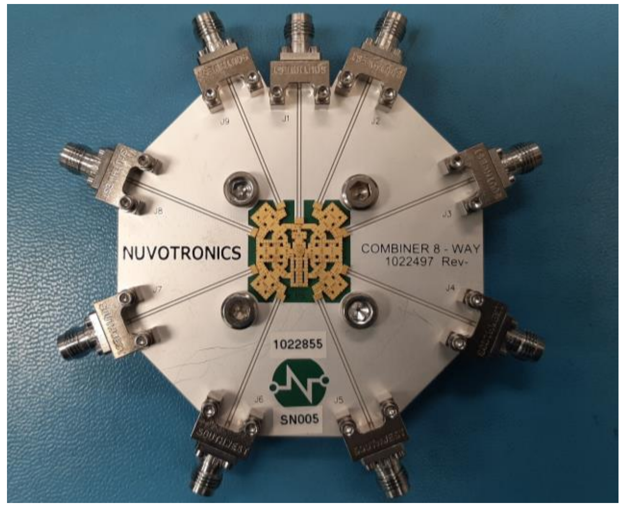

Figure 17. Assembled unit ready for test

F. Modal analysis

Dynamic properties of the 3R section were investigated to determine natural mode shapes and frequencies of the copper PolyStrata® structure using a finite element analysis software package (ANSYS).

The first six modes showed high frequency values over 6000 Hz (first mode, see Figure 16). Mass participation was calculated for all axis and rotational directions and is not significant (less than 1.9%). Based on historical data, the natural mode shapes are outside of the system excitation frequency range. The amplitude response of the copper structure will not be impacted at this frequency range.

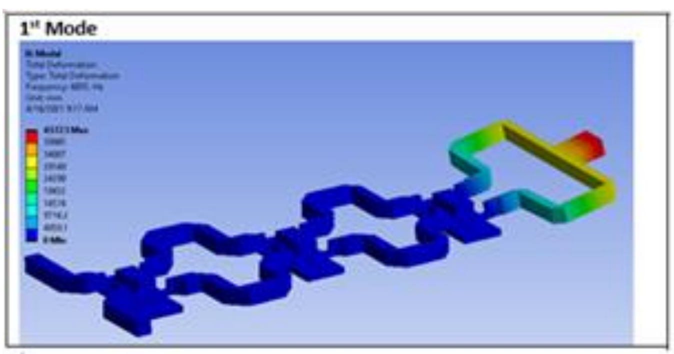

Figure 16. 1st mode (6035 Hz). Radiator body hidden for clarity.

III. Results

Sample parts were evaluated on a circuit card assembly with 2.4 mm precision coaxial connectors, shown in Figure 17. The loss and VSWR of the test fixture dominate the characteristics of the divider under test.

We used a 12-port VNA with 2.4mm interface but made no attempt to calibrate out connectors and traces of the evaluation board. Raw return loss of the common port is shown in Figure 18, here the equal-ripple response is masked by the VSWR of the connectors. Raw isolation is plotted in Figure 19 and is close to predictions.

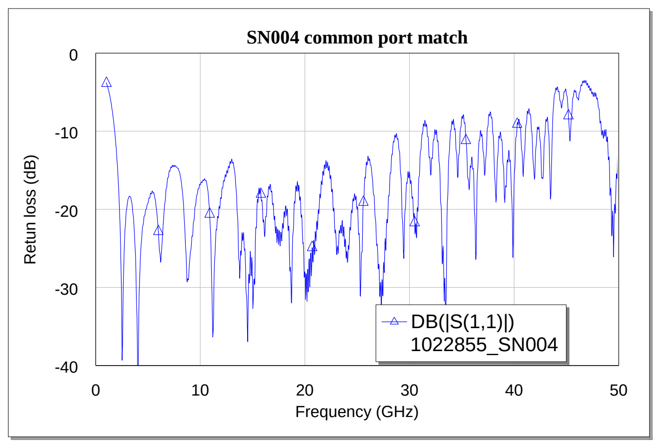

Figure 18. Measured common port return loss

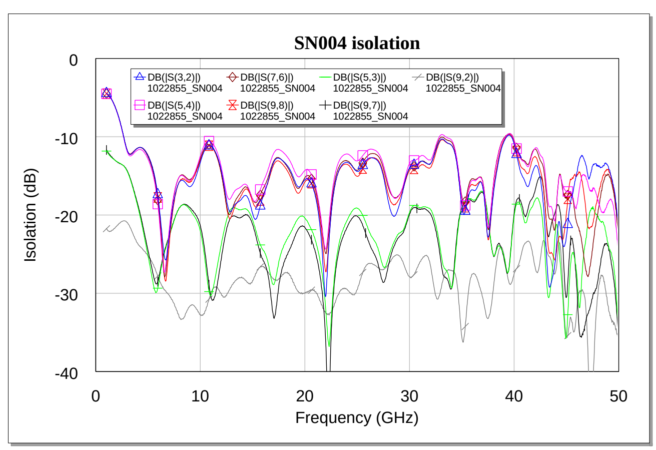

Figure 19. Measured isolations

We subtracted the modelled loss of the circuit card paths from the loss data and removed mismatch loss to evaluate the transmission loss of the divider (including the transitions). The loss trends to 1.5 dB at 40 GHz as shown in Figure 20, however there is a fair amount of noise in the resulting data which could not be removed.

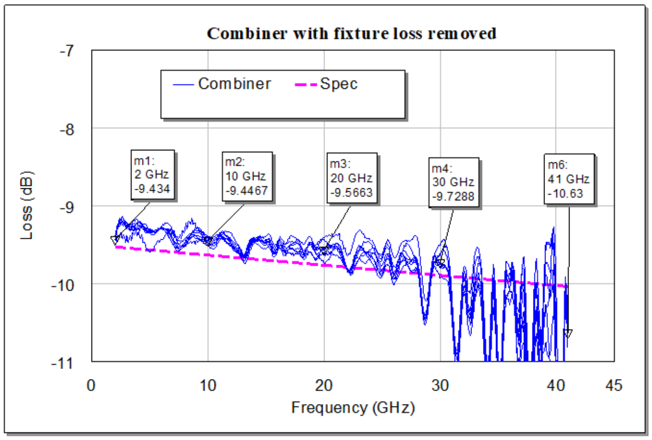

Figure 20. Measured, corrected insertion loss

IV. Conclusions

This paper presents a design procedure for creating optimum N-way corporate power dividers with broadband response, resulting in a 2-42 GHz (11:1 bandwidth) eight-way design. Insertion loss was evaluated at less than 1.5 dB. With size fitting a circle of 25.7 mm diameter and 1.5mm height, this divider shows unprecedented bandwidth, size and efficiency. With proper isolation resistors the divider can handle 10W or input power with graceful degradation.

Acknowledgements

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