Investigation of GaN on Si FET optimal efficiency harmonic terminations using a compact large signal model

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Abstract
There is much debate in the high frequency Power Amp design community as to which class of operation is most suitable for optimizing the efficiency of the GaN FET PA. While active loadpull measurements can be useful in observing actual termination sensitivities they do not necessarily explain the class of operation at the intrinsic current generator plane, without significant de-embedding, or reveal more subtle effects of device non linearity. A simplified compact large signal model was developed with emphasis on low number of parameters and robust, fast convergence under high harmonic reflection coefficient. The model has been constructed in a piecewise fashion to enable the effect of each of the intrinsic nonlinearities for example gate-source charge, to be easily disabled or examined. The model has been used to examine harmonic terminations and waveforms at the intrinsic current generator and to show the origin of the optimum second harmonic terminations on a GaN on Si device.

I. Introduction

Much focus has been given to the subject of increasing the dc to rf conversion efficiency of single ended and combined power amplifiers used in both commercial and defense applications. In terms of achieving GaN FET Power Amplifiers with high efficiency there are several models of operation or classes, as characterized by the device drain current and voltage waveforms and/or harmonic terminations. At the fundamental level the product of the overlapping (in time) drain current and voltage waveform dictates the dynamic power lost to internal dissipation, while the shape of the waveforms is enhanced by the harmonic impedances. The following table summarizes the main efficiency classes used by microwave frequency PA designers targeting high efficiency, and highlights their theoretical potential max drain efficiency and mode of operation.

Class	A	B	C	F	F^{-1}	J
Max Efficiency	50	78.5	100	100	100	78.5
Current Waveform	Sine	½ Wave Rectified Sine	Reduced Conduction Angle Rectified	½ Wave Rectified	Square	
Voltage Waveform	Sine	Sine	Sine	Square	½ Wave Rectified	
2fo Load Impedance	-	Short	Short	Short	Open	High Reflect Capacitive
3fo Load Impedance	-	-	-	Open	Short	-
Bias Point	Mid current	At Pinch Off	Below Pinch Off	Near pinch off	Near pinch off	Near pinch off

In this work an active harmonic loadpull system (Mesuro) was employed to carry out a search to iterate to the point of maximum efficiency for all harmonics under control rather than specifically set out to set up a particular class of operation. Fundamental load impedance and both 2f0 at input and output (source and load) are varied to reach the point of maximum drain efficiency achievable. We then present an investigation of the optimal terminations and waveforms with the help of a nonlinear model, to understand which class the device is operating in. Previous literature suggests that an inverse class F mode is the most efficient mode for GaN FETs since it has the benefit of a large voltage range open to the drain waveform (since GAN Fets are typically operated with supply voltage lower than 1/3 of breakdown voltage).

II. SECOND HARMONIC SOURCE AND LOAD PULL RESULTS

For the measurement study a 2mm x 0.4um GaN on Si pcm device with coplanar feed was used at 28V and an Iq of 20mA (near to pinch off). The initial set of results describe the input side second harmonic source pull in fig. 1. After iterating to the point of peak efficiency (gate current maintained <1mA/mm) by tuning/loadpulling f0 and 2f0 load, the 2f0 source pull was measured at points spread across the Smith chart and at fixed input power. The key features are that the peak efficiency point of 74.5% is located at close to a short circuit – at an angle of ~170degrees. Rotating clockwise the efficiency falls relatively quickly down to the low of 65%, which is maintained over a wide range of angles ie ~a 90 degree range. On the counter clockwise side of the peak the drop off is somewhat more gradual. In magnitude terms a full reflect condition is that which leads to the maximum efficiency.

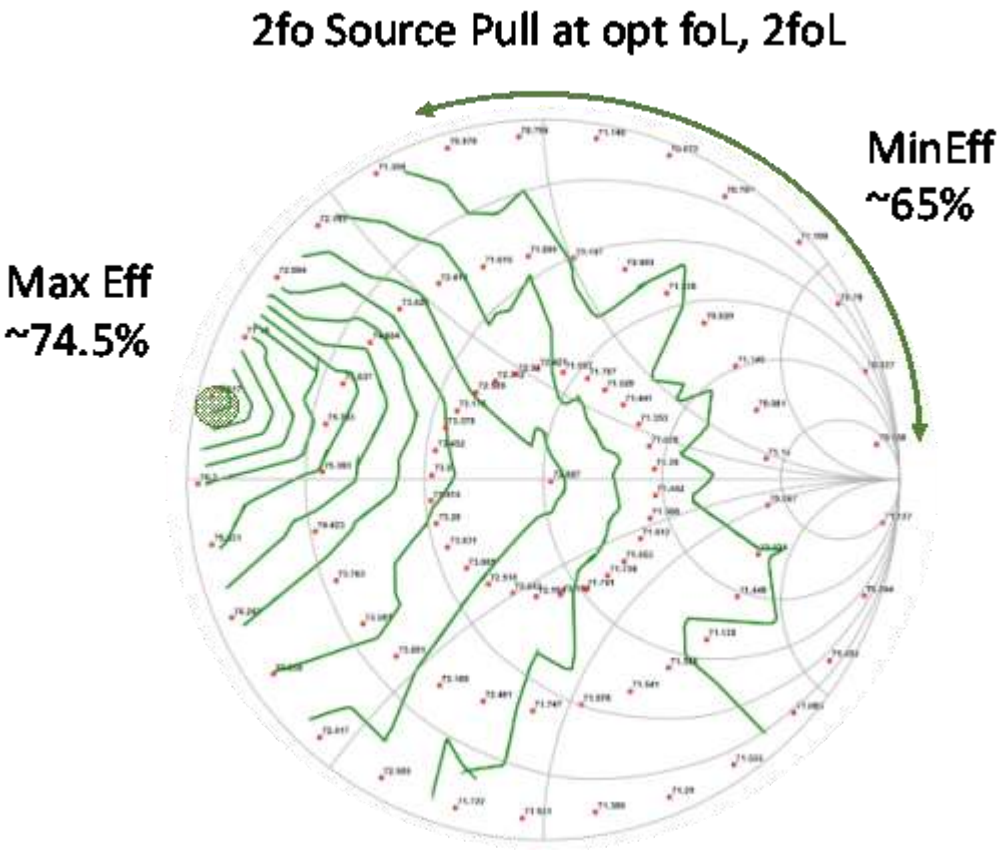


Fig. 1. 2f0 Source pull contours measured after iterating to peak efficiency point (with f0 and 2f0 load) on a 2mm GaN/Si device, f0=2.7GHz.

Second harmonic load pull was also carried out with two conditions of source 2f0 impedance are shown in Fig.2 and fig.3. Fig.2 shows the 2d harmonic load pull measurement with the 2f0 source set to 50ohm, while fig.3 shows the same load pull at 2fo but with an optimum 2f0 source (reflection coefficient 0.95, angle 170 degrees).

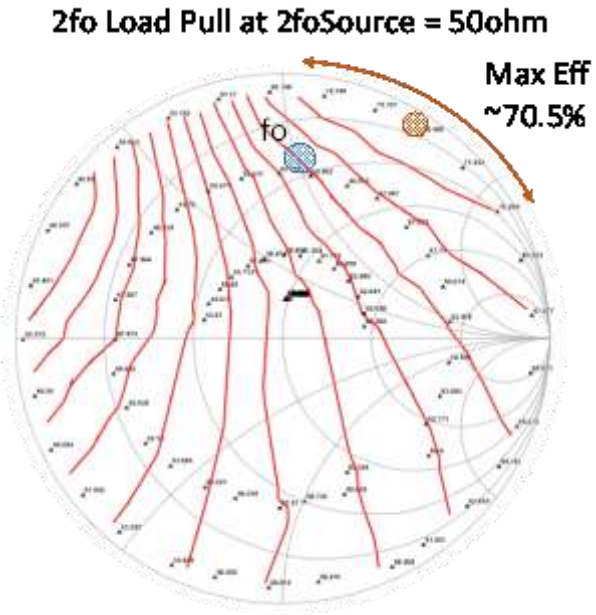


Fig. 2.2.7GHz 2f0 Load pull contours measured after iterating to peak efficiency point (with f0 load) and with 2f0 source at 50ohm, on a 2mm GaN/Si device, biased at 28V Iq 10mA/mm f0=2.7GHz

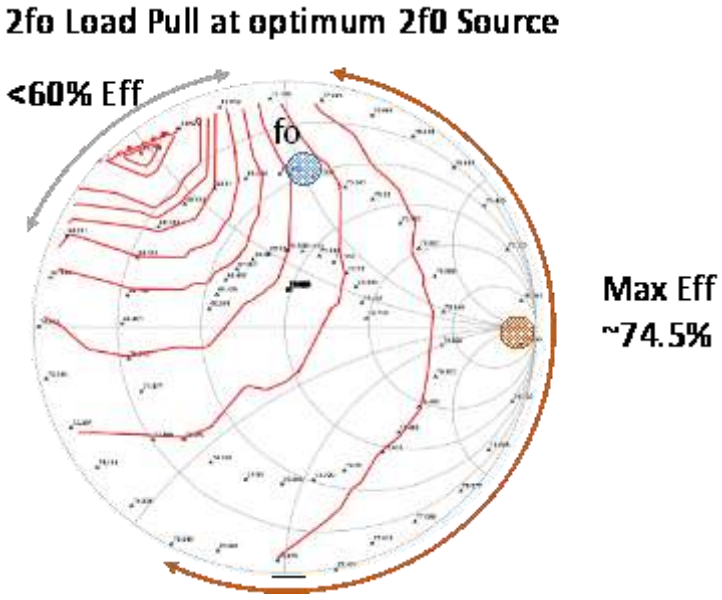
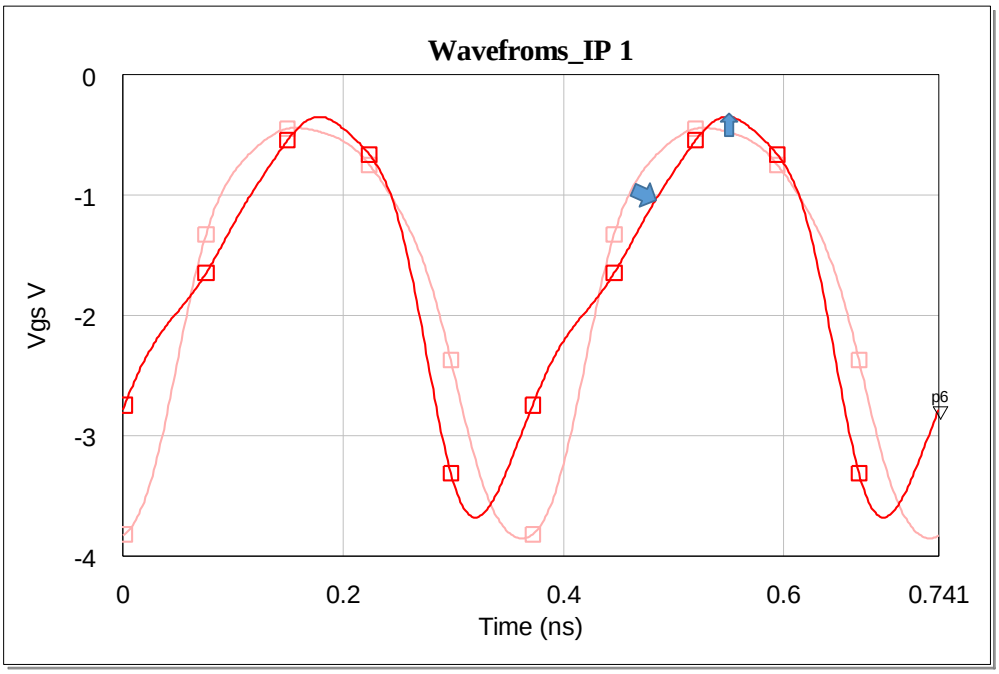


Fig. 3. 2.7GHz 2f0 Load pull contours measured after iterating to peak efficiency point (with f0 load) and with 2f0 source at optimum reflection coefficient = 0.95, angle 170 degrees, on a 2mm GaN/Si device, biased at 28V Iq 10mA/mm f0=2.7GHz.

The key features of the 2fo load pull results are as follows; that by setting the optimum 2fo source (rather than 50ohm or non-optimum phase) around 4% higher efficiency is obtained ie in this case 74.5% over 70.5%. For both graphs the red arcs give the range of angles that obtain efficiencies within 5% of the respective peak efficiency.

Fig. 4. Input voltage Vgs (internal) waveform simulated at peak efficiency point conditions (with f0, 2f0 load) and with 2f0 source at optimum reflection coefficient = 0.95, angle 170 degrees (bold trace) and with 2f0 source = 50ohm (feint trace), on a 2mm GaN/Si large signal model, biased at 28V Iq 10mA/mm f0=2.7GHz. Blue arrows indicate the sharpening up of the Vgs waveform obtained by



the optimal input 2f0 termination.

III. INVESTIGATION OF WAVEFORMS BY MODEL SIMULATION

An in house compact large signal model of the 2mm GaN on Si device was used to investigate the waveforms at the intrinsic device plane. Model agreement with waveform measurements at the extrinsic level was reasonably good, so this method was chosen essentially in place of de-embedding. Figure 4 shows the intrinsic input voltage waveform Vgs simulated for both the 50ohm 2fo source case (lighter red trace) and the optimum 2fo source impedance case (red trace in bold). What is apparent is that the top half of the Vgs waveform is less compressed ie more sinusoidal in the optimum impedance case. The compression of the original waveform is due to the nonlinear input 'capacitance' or alternatively the effect of the input displacement current. This topic has been outlined in [1] where voltage across an idealized nonlinear capacitor (with increasing capacitance versus voltage) is analyzed, showing the characteristic compressed effect. It is also noted that the optimum 2f0 tuned Vgs waveform is more consistent with a 'peakier' lower conduction angle shape (ie higher fundamental to dc average component) which will be translated to the output current waveform – since the current waveform is directly derived from the input Vgs by the device transconductance.

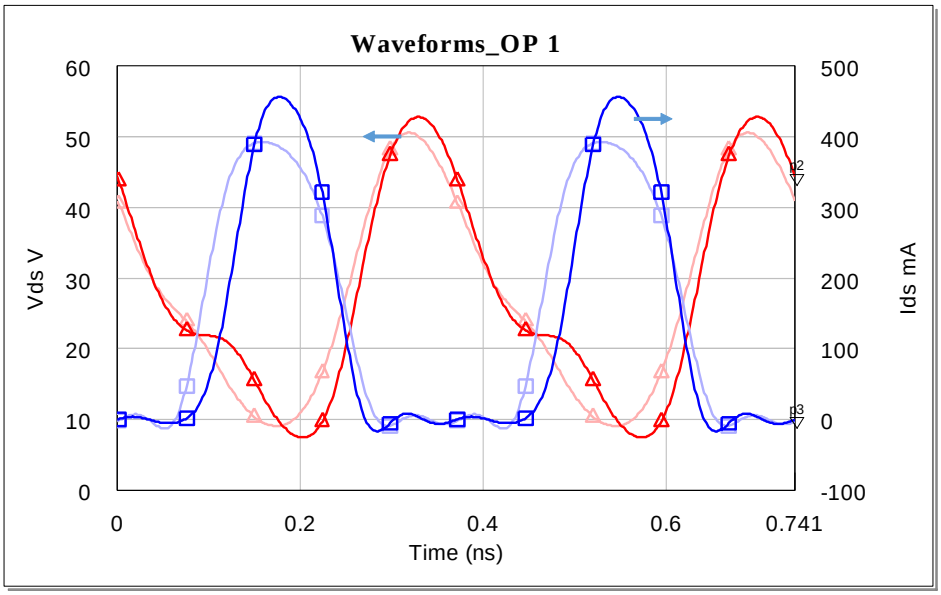


Fig. 5. Intrinsic (current generator plane) output voltage Vds and Ids waveform simulated at peak efficiency 2f0 source and load point conditions (bold traces) and with 50ohm 2f0S impedance (feint traces), on a 2mm GaN/Si large signal model, biased at 28V Iq 10mA/mm f0=2.7GHz.

This is shown to be the case with the output waveforms (taken before the onset of saturation) at the current generator plane given in Fig.5, where the current waveform of the optimum 2f0 source impedance case is also shown to have a 'peakier' lower conduction angle shape than the 50ohm case which is consistent with the higher efficiency obtained. Intrinsic 2f0 load impedance at this point is capacitive and is 'pulled' by the output nonlinear capacitance with drive.

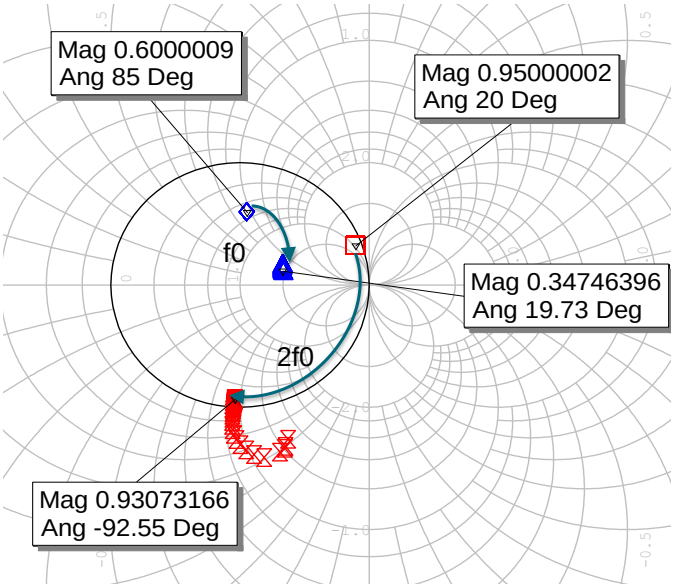


Fig. 6. Extrinsic and de-embedded f0 and 2f0 loads (to the current generator plane).

V. CONCLUSION

By employing a large signal model to investigate intrinsic voltage and current waveforms on a GaN on SI FET it has been shown that the optimum termination on the 2f0 source impedance reshapes the positive going input voltage waveform towards a more sinusoidal, and lower conduction angle shape. This is turn shapes the output current waveform into a lower conduction angle 'peakier' rectified wave and is the main reason for improved maximum drain efficiency. Output terminations and waveforms suggest the mode of operation at peak efficiency is saturated class J (capacitive intrinsic 2f0).

ACKNOWLEDGEMENT

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REFERENCES

[1] S. C. Cripps, "RF Power Amplifiers for Wireless Communications", Second Edition, Artech House Microwave Library, Artech House, 2006