E-BAND TRANSCEIVER DESIGN AT FILTRONIC

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ABSTRACT

The massive growth in mobile data is making increasing demands on backhaul capacity. Existing point to point links make use of ~15GHz of total bandwidth distributed in narrow licenced bands between 6 to 42GHz. These are already running close to capacity and more bandwidth is urgently needed to keep pace with the forecast growth in mobile data. An additional 21GHz of bandwidth has been allocated in V, E and W bands (57 to 95GHz), and is now coming into use. These frequencies offer opportunities to use much wider channels, up to ~2GHz, and the potential for data rates up to ~10Gbps. This paper will deal with some of the design methodologies in making low cost, high performance transceivers at these frequencies, particularly in the areas of MMIC technology and diplexer design. Considerations will be made of manufacturing tolerances and process variation, operation over a specified temperature range, reliability and stability, integration into transceivers and testability. The relevant microwave parameters simulated will be presented and will show good agreement with actual measurements.

INTRODUCTION

This paper will deal with transceivers where the Transmit and Receive signals are separated by Frequency Division Duplex (FDD). Other methods are Time Division Duplex (TDD) and polarisation diversity. With FDD, transceiver#1 in the link transmits in the frequency range 71-76GHz and transceiver#2 at 81-86GHz. Within these 5GHz bands, channels are allocated in 62.5MHz multiples, so for channels with 250MHz bandwidth, for example, 19 different channels can be established (125MHz guardbands must be placed at the ends of each 5GHz band).

Typically, a transceiver would transmit powers between ~12 and ~24 dBm depending on the modulation type and its partner receive with noise figures ~7dB. Antenna gain is limited by regulation[1] to be >38dBi (otherwise the beam angle would be too large and interference may occur with other links). A one foot Cassegrain antenna has 43dBi gain and the transceivers are typically separated by a few kilometres. The link budget can therefore be calculated but must take into account rain fade which is significant at these high frequencies and is of the order 10dB/km for heavy rain (25mm/hour). Under the conditions described, a 1.5km link (path loss 135dB) will, in practice, support a 3.2GB/s data rate in a 500 MHz channel with 256QAM modulation and >10GB/s in a 2GHz channel with 128QAM.

The effect of rain fade and its variability must be taken into account in the design of the transceivers which must maintain traffic under variable precipitation and temperature conditions and deliver Quality of Service >99.999% (equivalent to <5minutes outage / year). This can be achieved to a certain extent by using adaptive modulation and hence variable datarate. Transceivers however must also contribute to accommodating these variations by providing

transmit and receive gain control with Voltage Variable Attenuators or with amplifiers whose gain can be altered with gate voltage control. In addition the design must tolerate temperature and process variations of the components used. For example GaAs transistor gain typicaly varies by 0.0125dB/°C/gainstage and to avoid the need for complex tuning, the design must accommodate the statistical performance spread of the components which is typically of the order ±0.5dB/transistor gainstage.

The complete RF front end of the transceiver therefore comprises variable gain stages with an upconverting mixer in the transmitter and a downconverting mixer in the receiver. A common port is used for attachment to the antenna but Transmit and Receive signals are separated with a passive diplexer.

Specifications for the individual components was calculated, taking into account, on one level, receiver noisefloor and transmitter linearity and power. Compliance with spectral mask was also calculated with a systems simulator

MMIC design

E-band MMIC Chipset

The architecture of the RF front-end of a transceiver to be discussed is shown in figure 1 and, with the waveguide diplexer, comprises an LNA, mixer, frequency multipliers, medium power amplifiers, modulator, power amplifers, and voltage variable attenuators

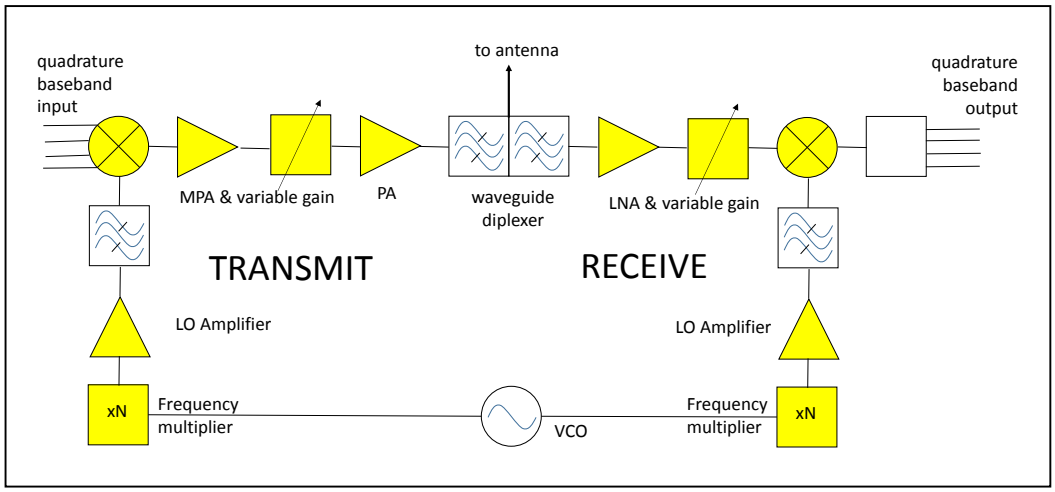

Figure 1: transceiver architecture: yellow shaded elements are included in the MMIC chipset

Using a common VCO means that additional downconversion is needed in the receive path since the output of the RF mixer is the separation between TX and RX frequencies (10GHz). A direct downconversion architecture requires two VCOs

Choice of foundry

The UMS PH10 commercial foundry process was chosen for the lower power / low noise and WIN Semiconductors PP10 commercial foundry process for the PAs and HPAs

Small signal gain

Good agreement was obtained between simulation and measurement of most MMICs. Examples for the lowband LNA and lowband PA are shown in figures 2 and 3

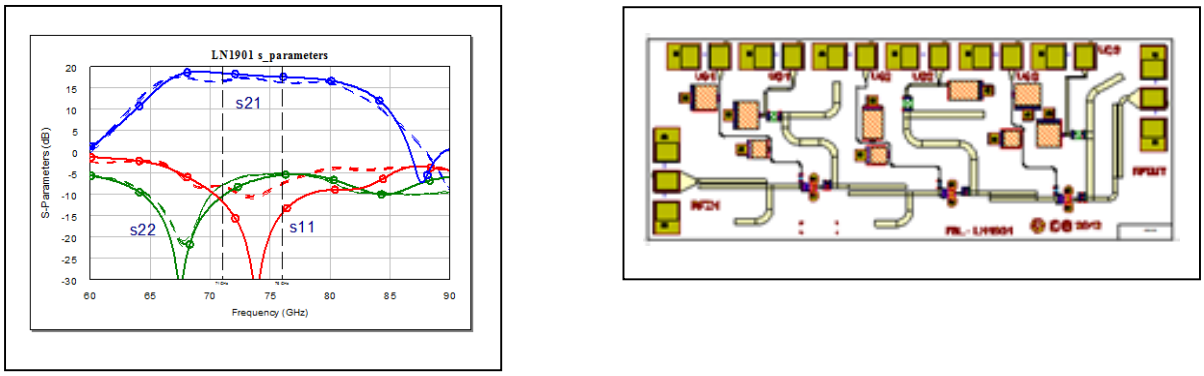

Figure 2: lowband (71-76GHz) LNA s-parameter simulation (solid traces) versus measurement (dashed traces) and layout

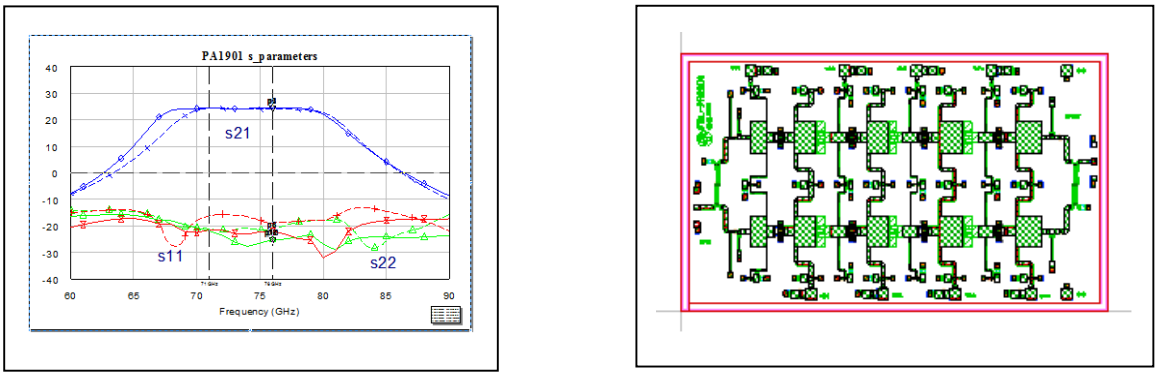

Figure 3: lowband (71-76GHz) PA s-parameter measurement (solid traces) versus simulation (dashed traces) and layout

Linearity

The faithfulness of the device output to follow input is crucial in the application and characterised by the third order intercept point (IMD3) where the effects of the interaction between two tones closely spaced in frequency are monitored. Figure 4 shows good agreement between the simulation of IMD3 for the same power amplifier described above and the measurement of a typical device. At a total output power of 18dBm (the greatest at which the device is expected to operate), simulation predicts the measured -27dBc to -31dBc range (over 71-76GHz) within 1dBc

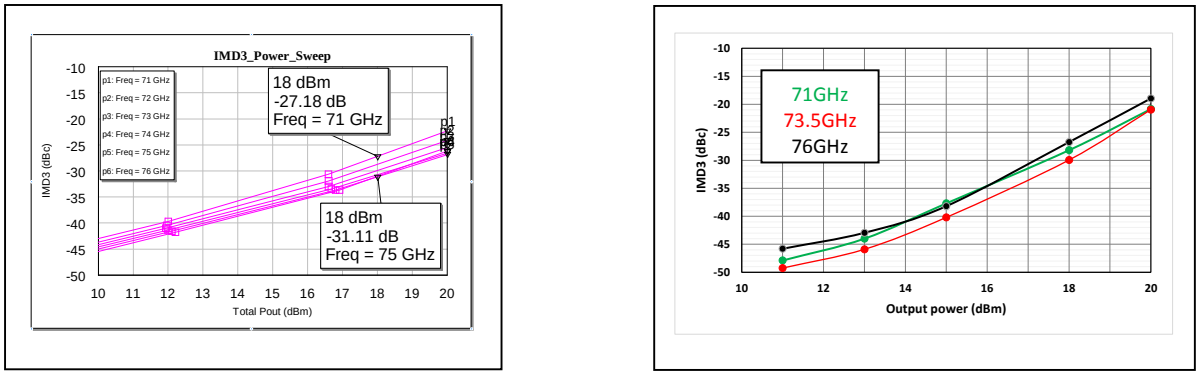

Figure4: simulated (left hand graph) and measured (right hand graph) of Output IMD3 of the lowband (71-76GHz) PA

Process and temperature sensitivity analysis

MonteCarlo analysis simulations were carried out with the process variations given in the design manuals. For amplifiers, this gave rise to the ±0.5dB/gainstage variation, which was demonstrated in practice with a large number (4812) of devices made from three production runs (8 wafers). For the 3-stage LNA, described above, 90% of the population had s21 within 3dB, as shown on the left in figure5. Gain variation with temperature followed the generally accepted value of -0.0125dB/°C/stage, as demonstrated by a five-stage medium power amplifier and shown on the right in figure 5

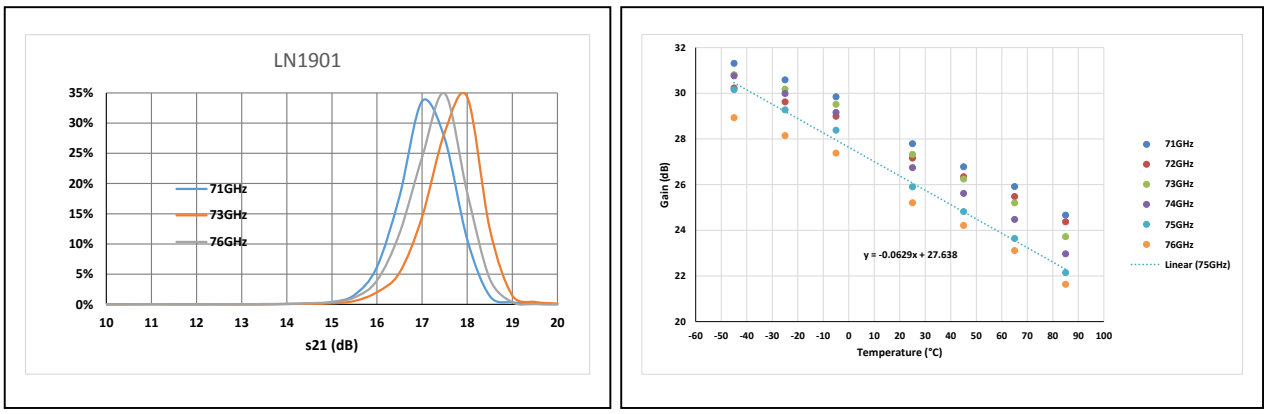

Figure 5: demonstration of gain variation over many devices and over temperature. The lefthand graph shows s21 distribution over 4812 LNAs. The righthand graph shows results from a medium power amplifier

Electromagnetic simulation

Since a standard circuit simulator will only take into account connections between adjacent elements, the interaction between features which are laid out physically close but nodally separated will not be calculated. It was therefore essential to carry out electromagnetic (em) analysis. However, this was only possible on the passive devices, so these had to be extracted from the circuit, simulated as an n-port, then re-inserted into the main circuit with the transistors. The difference between a simulation where the passive parts of the circuit have been em simulated and a simulation of the same device where this has not occurred is shown in figure 6, along with the measurement of the real device. The simulation without em simulation has a response shifted away from the measurements whereas that with em analysis represents the measured data well

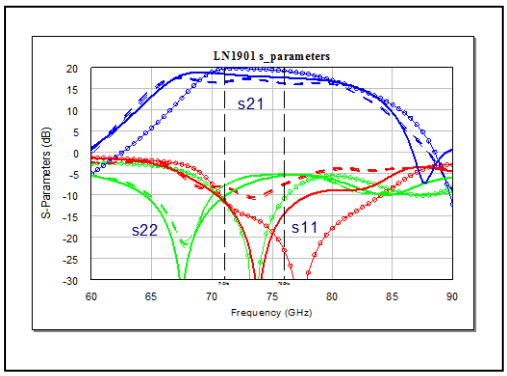

Figure 6: Comparison between simulations using

- *Simulation with schematic elements only (lines with circles)*
- *Simulation with full em analysis (solid lines)*
- *measurements of several devices (dashed lines)*

Em analysis was also essential for creating new passive structures that are not available in the foundry design manual. An example is shown in figure 7 where well modelled 2x50 transistors are combined with a 7-port manifold, which clearly could not be regarded as a standard element such as a transmission line

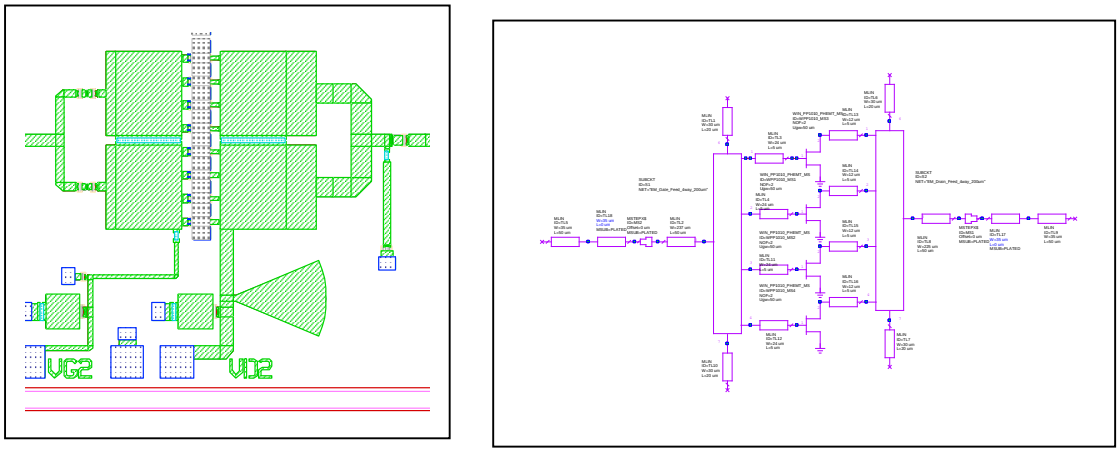

Figure 7: em analysis used to create a new element

Stability

The Rollets stability criterion (k) is necessary but insufficient for determining the stability of a MMIC. This parameter measures whether a circuit is unconditionally stable from the outside ports but does not indicate if there are any internal instabilities. Instead, it is necessary to take advantage of an element provided in most circuit simulators which determine the complex reflection coefficient looking out from and in towards an active device. The gain of the loop formed between the forward and reverse signals around the join is calculated and the Nyquist stability criterion states that if this gain, when plotted on the complex plane, encircles the -1 point in the clockwise direction, then the closed loop system will be unstable. Figure 8 shows the analysis of a transistor in the lowband Power Amplifier

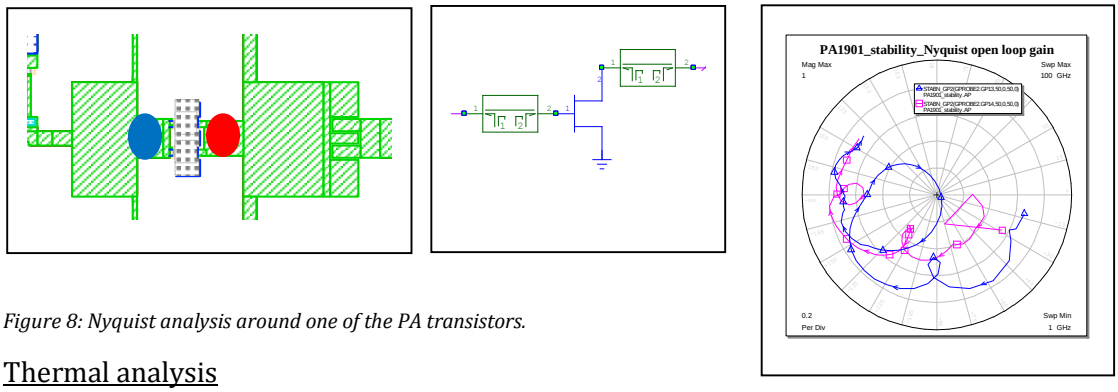

Figure 8: Nyquist analysis around one of the PA transistors.

Thermal analysis

It was essential to calculate the thermal properties of the devices, since temperature significantly affects reliability as well as performance. In Comsol Multiphysics, the heat developed in the drain source region of each transistor was simulated with a heat source calculated from the dc current and voltage. For the PAs, peak junction temperatures were predicted to be 159°C with the device biased at 4V, 250mA/mm in a module operating at 80°C, as shown in figure 9.

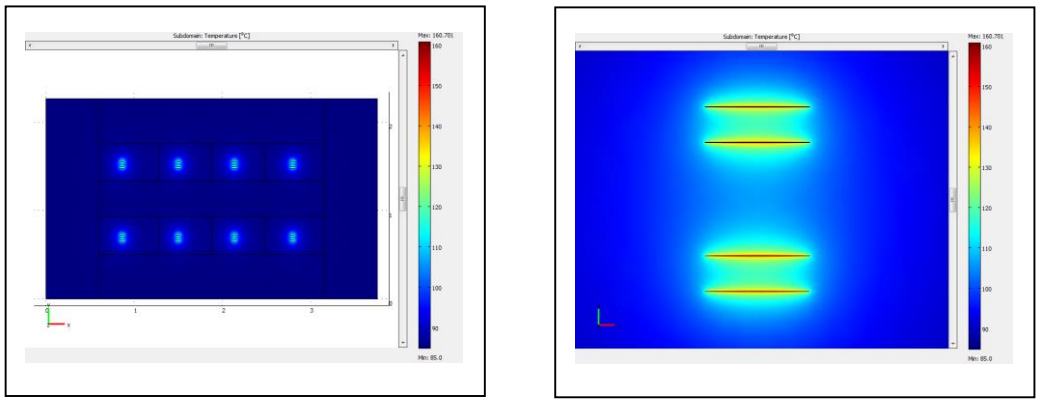

Figure 9: thermal simualtions of the PA MMIC. The lefthand image is of the complete MMIC, the righthand image is of one of the 4-gate transistors

Mean-Time-To-Failure (MTTF) was then calculated from the Arrhenius equation

$$MTTF \; \alpha \; exp \; (Ea/kT)$$

where k is Boltzmann's constant, T (Kelvin) is the operating temperature and Ea is the activation energy of the degradation process, considered to be "gate sinking" which is the interaction between the gate metal and underlying semiconductor. Ea is determined in the foundry by measuring the time to failure (t) of 50% of several sets of devices heated to different elevated temperatures, then calculating the gradient of the ln(t) vs 1/T graph formed.

For the Power Amplifiers in question running at 250mA/mm with a junction temperature of 159°C, MTTF was calculated to be 1.49 $x10^7$ hours

Voltage Variable Attenuator

A VVA was designed in the pHEMT process with transitors shunting the RF in a continuously controlled way using adjustable gate bias. Using four transistors, 23dB range was achieved with 2dB standing loss. Linearity was predicted well with a worst case occurring close to maximum attenuation (IIP3=5dBm)

Frequency Multipliers

By appropriately biasing the transistor gates to allow drain current to flow during 25% of the cycle, the second harmonic of the input signal can be efficiently extracted. With a single stage pre-amp, frequency doublers were designed and made which had 0dB gain and delivered the required 0dBm in E-band, with >17dB rejection of the fundamental.

Mixer

A fundamental mixer was designed which provided 8dB conversion loss, as simulated

Modulator

The LO signal was modulated with the baseband signal with a vector modulator comprising Lange couplers arranged to alter the phase and magnitude of the LO according to the differential baseband I, Q signal

Design checking

It was crucial that designs were made "right first time" as it is almost impossible to correct afterwards (and impractical in production) and it is very expensive to repeat a foundry run. Before submission to the foundry, the designs were checked as follows:

- using Rollet and Nyquist analysis to ensure devices are stable
- with thermal analysis to ensure reliability is adequate
- by MonteCarlo analysis to ensure performance is met under all conditions of temperature, and process variation
- with Design Rule Checks, which are mandatory to ensure that the foundry can reliably manufacture to the design submitted
- that tracks and resistors (and gates) can support the currents
- that voltages across components are not exceeded
- that components were not placed within 50μm of bond pad and that bondpads are kept at least 150μm apart. (A wirebonding tool has a typical outside diameter of 100μm, so would crush any feature within this range)
- that there are no RF ports on the same MMIC edge as DC. The devices in question are RF-On-Wafer tested and as RF probes are extremely expensive, these probes must be used for different device types. This would not be possible if they were associated with IC-specific dc pads.
- that the external circuit into which the MMICs will be placed is considered. For example, bonds could not cross each other

DIPLEXER DESIGN

The waveguide diplexer comprises a lowband and highband bandpass filter. The methodology for designing a practical diplexer was as follows :

1. Given the passband and ripple, the number of poles needed for an ideal Tchebychev filter were determined by the isolation required.
2. Using in-house design software, a waveguide filter prototype was designed which outputs idealised physical dimensions for the discontinuities.

3. These physical values were imported into 3D software (EMPro), the machining restrictions (such as radii) were included and the s-parameters of each real discontinuity were simulated (see figure 10).
4. The s2p files produced were combined with well established models of straight waveguide sections whose lengths were varied in a circuit simulator until the required filter performance was achieved. The number of discontinuities combined was the filter order
5. Simulations of the highband and lowband filters were combined in a waveguide tee to form the diplexer, as shown in figure 10.

Agreement between simulation and measurement is excellent, as shown in figure 11

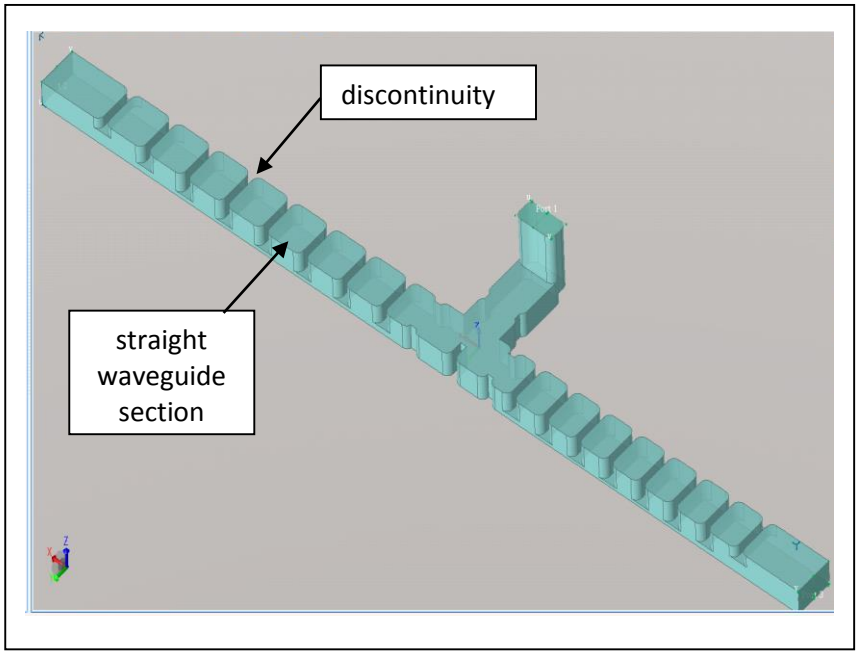

Figure 10: Physical shape of the diplexer simulated, showing the discontinuities, straight waveguide sections and tee: the blue shade regions are air

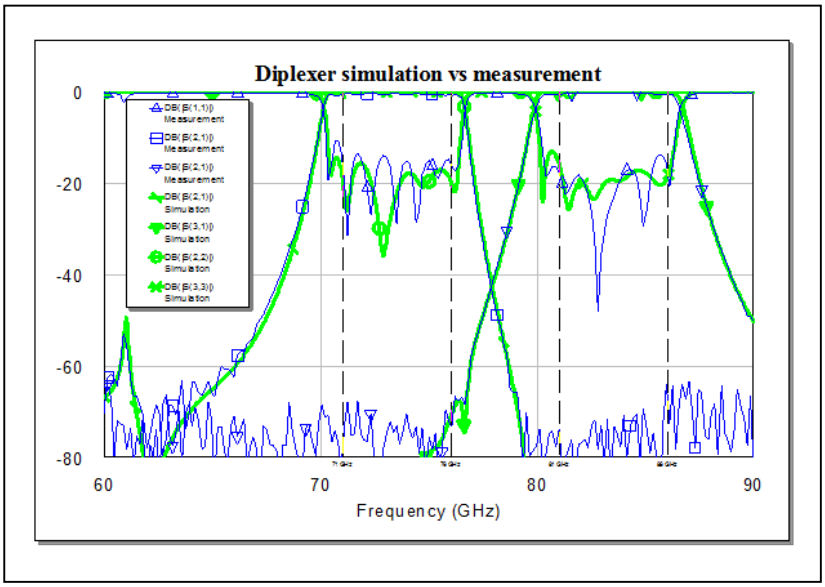

Figure 11: simulated (blue) and measured (green) performance of the diplexer

TRANSCEIVER EXAMPLE

An example of a transceiver product with MMIC and diplexer designed as described is shown in figure 12

Figure 12: Transceiver

Figure 13 shows the mm Wave section with integrated surface mount diplexer:

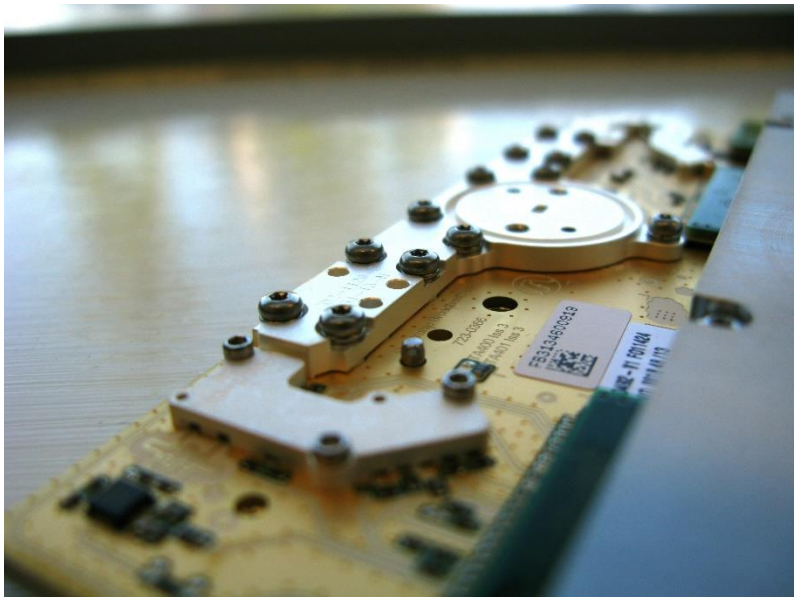

Figure 13: mm Wave section with integrated surface mount diplexer

This transceiver is fully integrated requiring just a single connection to the modem for Tx and Rx baseband signals, power supplies and SPI control. It contains VCOs, PLL and a microcontroller to set operating frequency and transmit power. Automatic Rx gain control is incorporated to adjust the Rx gain to accommodate receive signals over >65dB dynamic range. The transceiver is capable of operating at modulations levels up to 256QAM which, in a 500 MHz channel, will deliver error free data rates of 3.2Gbps with transmit powers up to 13dBm. Figure 14 shows the 256QAM constellation and signal to noise ratio.

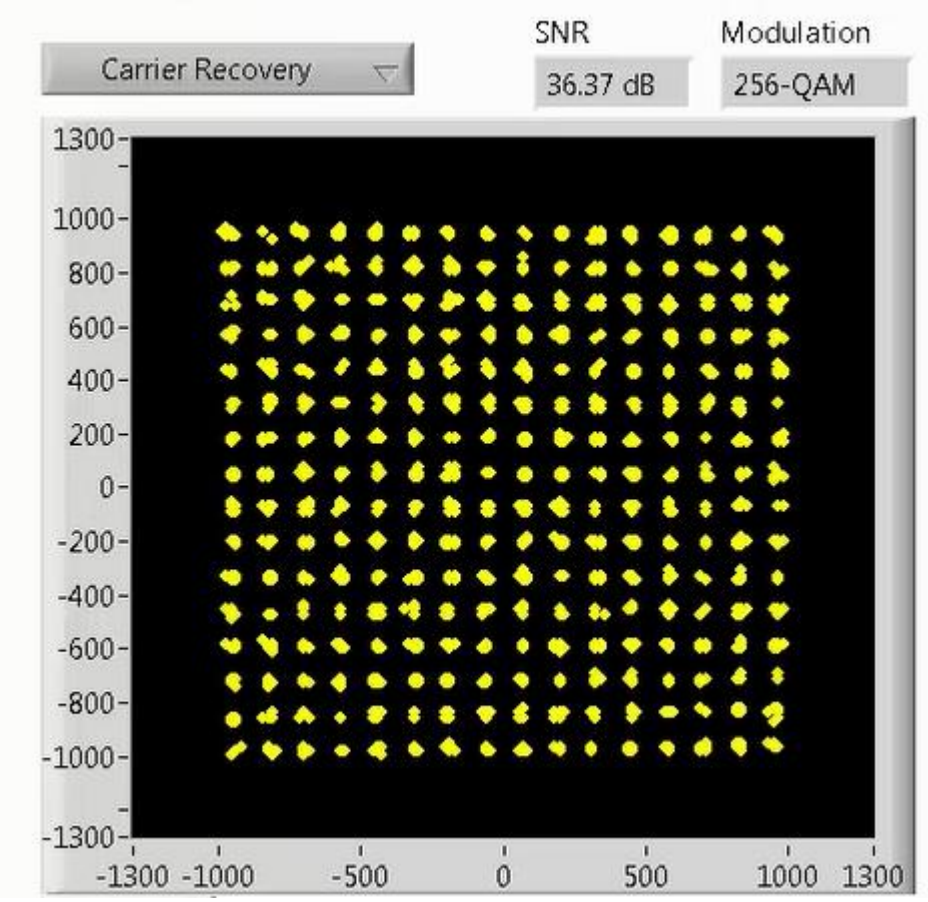

Figure 14: 256QAM constellation and signal to noise ratio of the Transceiver

CONCLUSION

The methodology for designing the key elements of the RF frontend of an E-band transceiver has been described. By following the principles outlined, good agreement was obtained between what was required for the diplexer and what was achieved. In the case of the MMICs, all circuits performed right-first-time on a pizza maskset. The designs were then transferred to production masksets and the devices are now used in E-band transceivers capable of delivering 3.2GB/s data rates in 500MHz channels in E-band.

REFERENCES

1. ETSI document EN 302 217-4-2 clause 4.4. Fixed Radio Systems; Characteristics and requirements for point-to-point equipment and antennas; Part 4-2: Antennas