A Fully Integrated 3.5GHz Single Chip GaN Doherty PA for sub-6GHz 5G

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Abstract

This paper describes the development of a fully-integrated packaged Doherty amplifier monolithic microwave integrated circuit (MMIC), fabricated on a 0.4 µm 28 V GaN-on-SiC process. It provides 18 dB of small-signal gain between 3.4 GHz and 3.8 GHz and delivers 45dBm of output power at saturation with a power-added efficiency (PAE) of 50 %, while maintaining a PAE of 31.5 % at 8 dB back-off. The PA is suited to many high-power applications for transmission of modulated signals including in a 5G base station transmitter. The PA may be used in conjunction with digital predistortion (DPD) for improved linearity.

Introduction

5G will be implemented in two distinct frequency ranges, the sub-6GHz region (FR1) and the mm-wave frequencies (FR2). 5G networks at mm-wave frequencies promise very high data-rates across very small network cells (picocells), typically in densely-populated cities. However, the first 5G networks will utilise sub-6GHz frequencies and transmit across large cells in cities, towns and rural areas. Not only will this make the transition from 4G/LTE to 5G easier for service-providers (whose existing LTE/4G networks already use channels within bands between 600 MHz and 3.5 GHz), but good overall coverage is achievable due to the long-distance propagation characteristics of lower frequencies. Like the current 4G/LTE networks, base stations will transmit high-power RF signals over large areas or "macrocells", each requiring a high-efficiency power amplifier (PA) to avoid unnecessary power consumption during transmission. One of the expected sub-6GHz 5G bands will be between 3.4 GHz and 3.8 GHz.

A popular method for obtaining high power-added efficiency (PAE) at back-off from compression is the Doherty Amplifier. A good summary of the various implementations of the Doherty amplifier can be found in [1]. Plextek RFI has developed an S band, packaged MMIC PA for use in 5G base station transmitter applications. The design was realised on GCS' 0.4 µm Gallium Nitride (GaN) process and assembled by Filtronic into an 8 mm x 8 mm custom laminate QFN-36 package.

The PA delivers 45 dBm of saturated power from a 28 V supply rail, with a peak PAE of 50 % and a PAE of 31.5 % at 8 dB back-off. Operational bandwidth is between 3.4 GHz and 3.8 GHz, which covers the allocated international 5G channels in this band. This paper covers the design, simulation, assembly, and subsequent measurement of the power amplifier IC.

Doherty Amplifier Basics

5G networks will use modulation schemes with high peak-to-average power ratios (PAPR). Since the transmitter PA is required to amplify large yet infrequent signal peaks, it spends most of its

conduction time amplifying comparatively small signals, drawing excess current from the power supply between peaks.

When choosing a suitable PA for this application, Class A amplifiers are too inefficient, Class D/E/F amplifiers are too nonlinear and feedforward or outphasing techniques are difficult to implement. Class AB or Class B power amplifiers are often used as a compromise between efficiency and linearity, but these may only provide a typical backed-off PAE of 15 %.

A basic Doherty circuit, as seen in Figure 1, employs two amplifiers; the 'Main' and 'Auxiliary' amplifiers (sometimes referred to as 'Carrier' and 'Peaking' amplifiers, respectively). The main amplifier is biased in Class AB while the auxiliary amplifier uses a Class C bias, ensuring that both amplifiers are conducting under large signal-drive but only the main amplifier is in use at back-off. The output matching network consists of two impedance transformers which ensure that optimal impedances are presented to the amplifier in both compressed and backed-off operation. By operating at two input power-dependent bias points, this topology allows the amplification of both small- and large-signal inputs without compromising efficiency.

The impedance inverter at the output of the main amplifier results in a 90° phase shift between the main and auxiliary amplifiers. In order to ensure that the main and auxiliary output powers are combined in large-signal operation, a corresponding 90° phase shift has to be added to the input of the auxiliary amplifier branch.

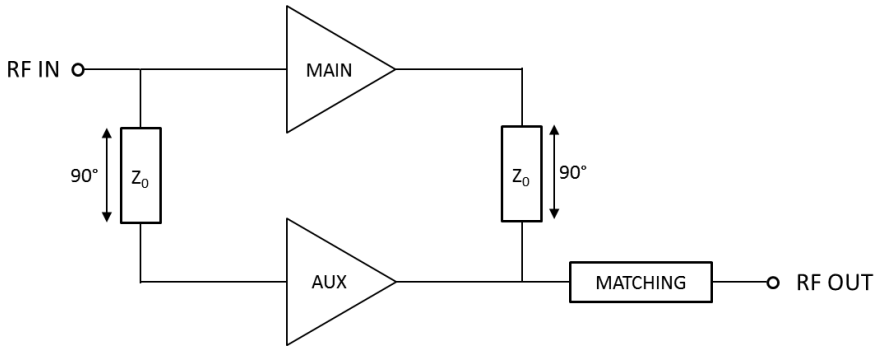

Figure 1: Doherty Amplifier Block Diagram

Figure 2 illustrates the theoretical efficiency vs output power of an ideal Doherty amplifier in blue compared to a Class B amplifier (in red). It can be seen that the efficiency at saturation is 78.5% in both cases but that the Doherty PA also achieves this efficiency at 6dB backoff. This efficiency curve has been plotted using ideal analysis and does not account for knee voltage and other realistic transistor effects. In a classic Doherty design the two efficiency peaks are spaced 6 dB apart, however it is possible to modify this spacing by changing the auxiliary amplifier's bias point or by adopting an asymmetrical design.

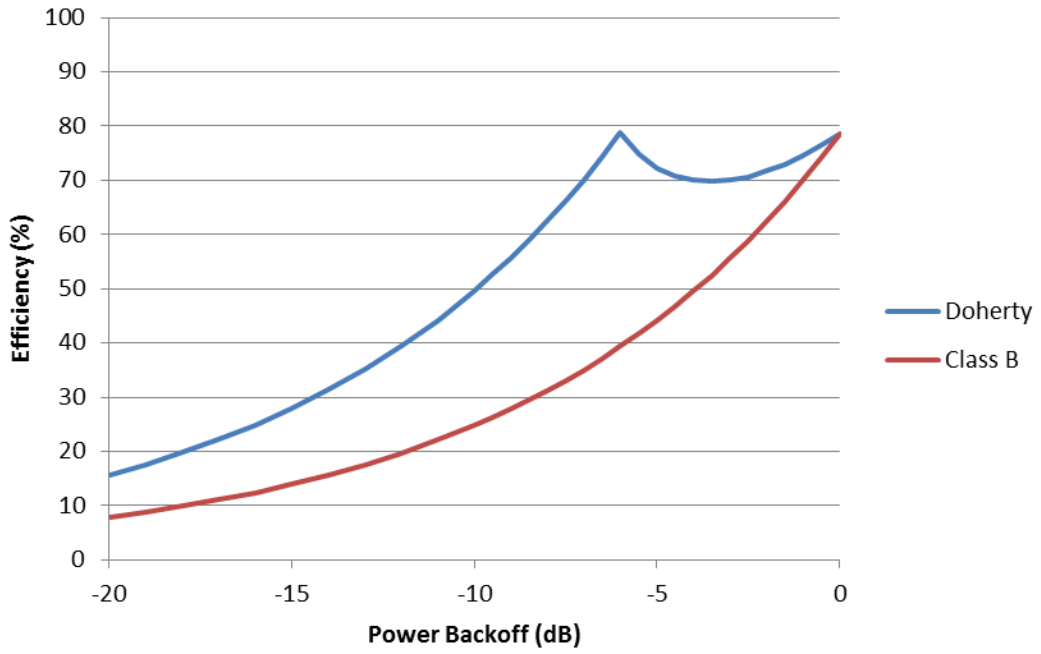

Figure 2: Theoretical Efficiency vs Output Power of a Doherty Amplifier compared to a Class B Amplifier

MMIC Design

A block diagram schematic of the MMIC can be seen in Figure 3. The Doherty PA was developed on GCS' 0.4 µm GaN-on-SiC process.

An identical design was used for the main and auxiliary amplifiers, commonly referred to as the 'symmetrical' Doherty configuration. It should be noted that a practical symmetrical Doherty amplifier (termed 'Doherty Lite' by Cripps [2]) does not exhibit the 'twin peak' response shown in Figure 2 but still shows a substantial improvement in back-off efficiency compared to the conventional Class B amplifier. Whilst it is common for the auxiliary amplifier to be capable of higher peak power than the main amplifier - the 'asymmetrical' Doherty - it has been shown that improved back-off efficiencies can be realised using the symmetrical configuration, which also has the advantage of a simpler design and better power utilisation factor (PUF) [3] [4].

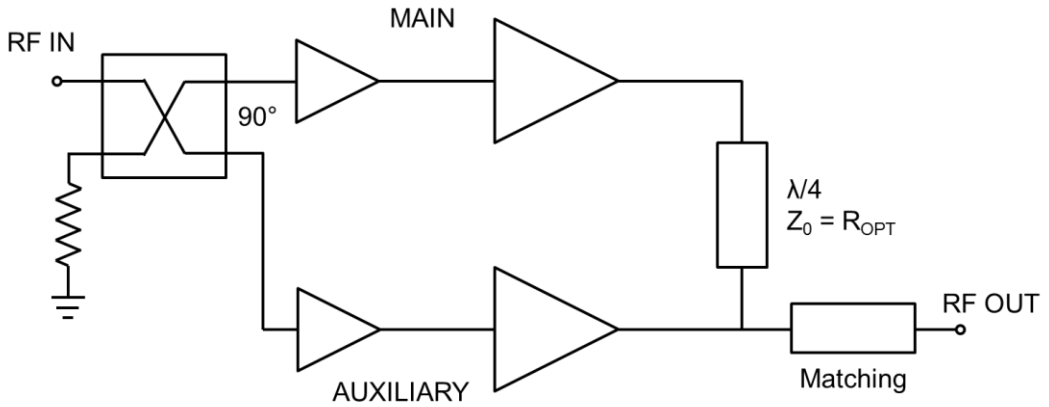

Figure 3: Block Diagram of the Doherty MMIC Power Amplifier

Each output stage consists of two parallel transistors, both driven by a single, smaller device. The transistor drive ratio between the first and second stages is carefully selected to provide sufficient linear power to the output stages without compromising efficiency.

Extensive load-pull simulations at various bias points were performed on GCS' nonlinear device models. This was to ensure that the optimal device sizes, load impedances and current densities were selected for Class AB operation, before synthesis of any matching networks took place.

The driver and output devices were stabilised using interdigitated or serpentine thin-film resistors at their inputs, which enable low-value resistances to be realised within a compact layout area. The output stage transistor drains were interlinked with a resistor to suppress odd-mode oscillations, though the output stage was kept as symmetrical as possible, to ensure the 2 mm output devices are driven equally.

In order to flatten the transistors' negative gain slope across the frequency band a passive equaliser network was included. This network was placed at the input as opposed to the inter-stage matching network (ISN) or output matching network (OMN) to preserve PAE. The driver stage's gate bias inductor was implemented in a thin, low-Q metal layer for additional gain-shaping. A lumped-element 3 dB hybrid was used to realise the equal power division and quadrature phase shift at the input of the auxiliary amplifier.

The Doherty OMN consists of an impedance transformer to transform 50Ω to $R_{OPT}/2$ and an impedance inverter, which in conjunction with the auxiliary PA performs the power-dependent impedance transformation. The network also incorporates the main and auxiliary output stages' drain bias networks. When designing the OMN, care must also be taken to ensure that the auxiliary amplifier is not 'loading' the main amplifier in low power mode.

The MMIC is "self-contained," with regards to the supplies and each supply connection is sufficiently decoupled on-chip down to low-frequencies. Separate gate bias connections allow the possibility of bias tuning of the fabricated amplifier on the lab bench. The two output stage VDD (drain) supplies are DC coupled, whereas the driver stage drains are independent. The MMIC is designed, however, to draw all drain currents from a single 28 V supply. Ground-signal-ground (GSG) pads were included at the RF input and output to allow RF on-wafer probe testing if required. The final layout of the 4.7 mm x 4 mm die is shown in Figure 4.

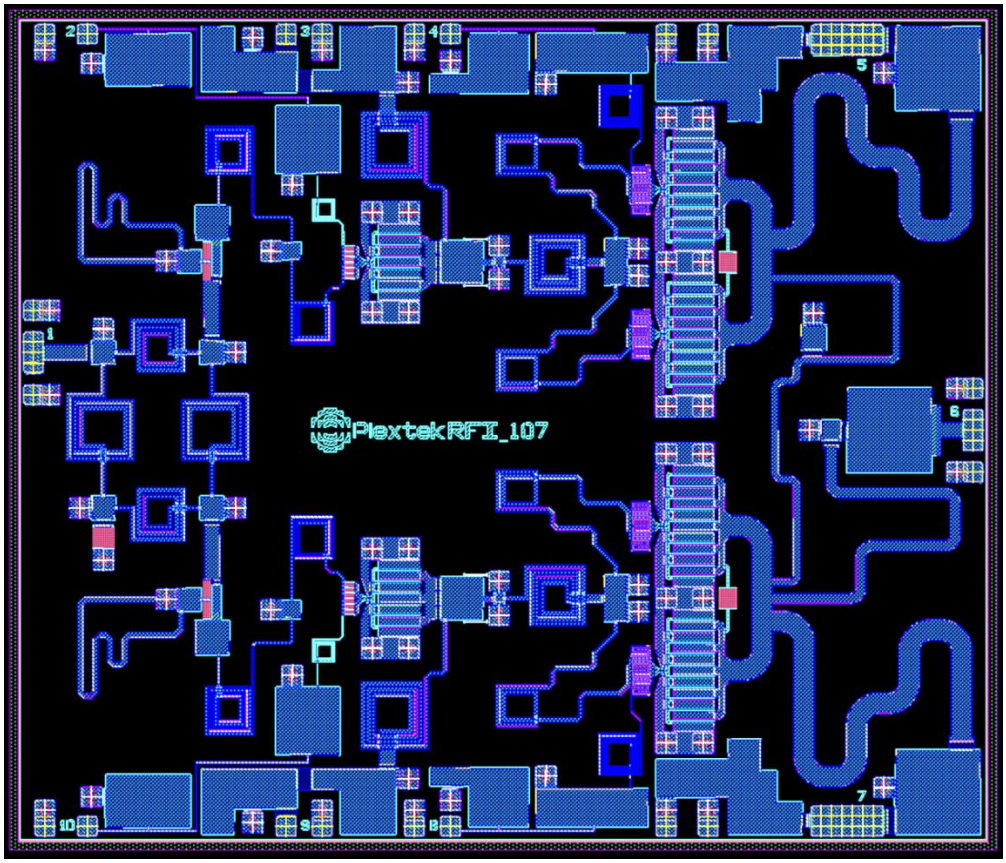

Figure 4: Pre-Fabrication Layout of S-Band Doherty PA MMIC

Input Splitter and Driver Stage Design

For a two-stage Doherty design the driver stage can either be implemented as a single transistor located before the input splitter or as separate drivers for the main and auxiliary amplifiers. It has been shown in [5] that using separate drivers for the main and auxiliary amplifiers, with the input splitter placed before the driver amplifiers, is best for overall PA efficiency.

Whilst most Doherty papers focus on the design of the output impedance inverter, it is also important to optimise the design of the input splitter. Excess loss in the input splitter will degrade gain (and hence PAE) and an incorrect phase shift at the input will result in imperfect signal recombination at the output of the PA. For this design a lumped element implementation was used and steps were taken to ensure a 90° phase shift was achieved across the full operating band, as can be seen in Figure 5. It is also necessary to achieve good isolation between the inputs of the main and auxiliary amplifiers so that the turn-on point of the auxiliary amplifier is not affected by the main amplifier. The simulated isolation of the input splitter is shown in Figure 6.

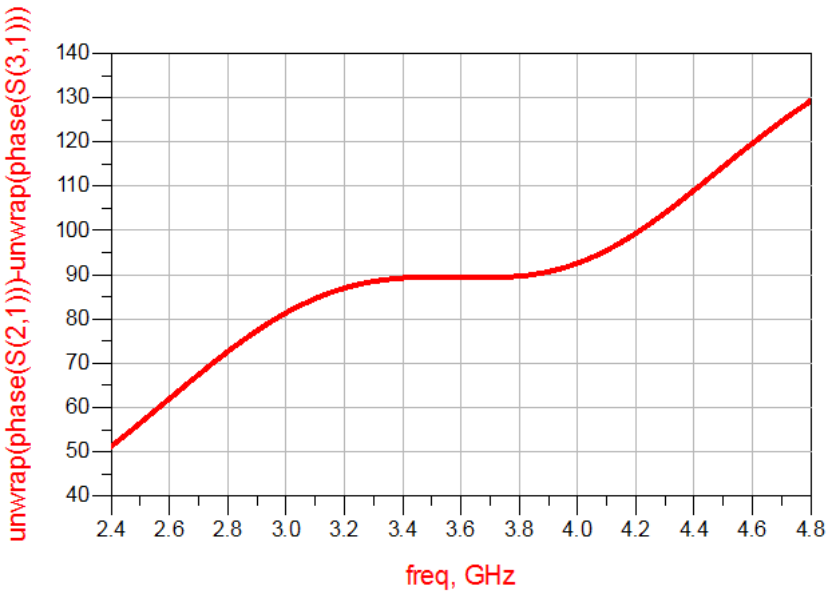

Figure 5: Phase Shift of the Input Splitter

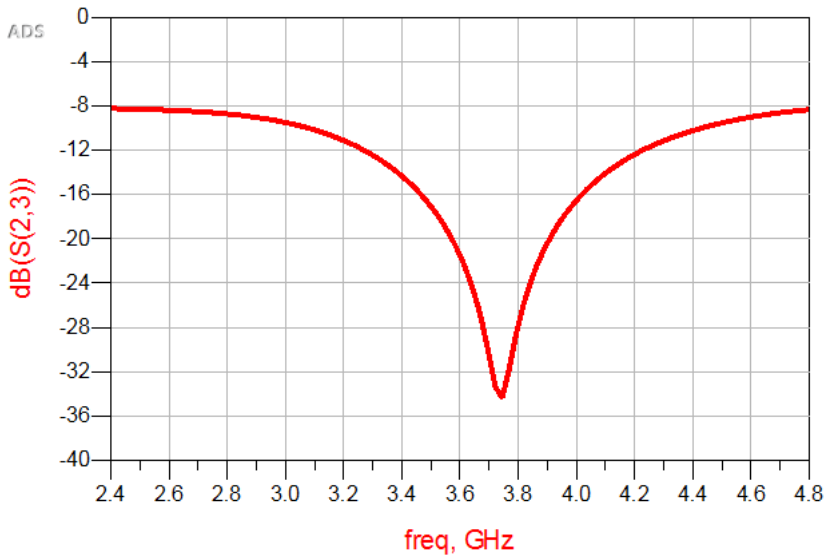

Figure 6: Isolation between Main and Auxiliary Inputs

Simulations were performed in Keysight ADS 2017. All of the passive structures were EM-simulated in Keysight Momentum and the transistor cells were simulated using GCS' nonlinear device models.

By biasing the main and auxiliary amplifier equally the MMIC can be operated in a 'balanced mode' to provide a comparison between this and the Doherty mode of operation. It should be noted that this balanced mode is not the same as a true balanced amplifier, which includes a quadrature splitter or hybrid at *both* input and output. All drain supplies are held at 28 V.

	Doherty Mode	Balanced Mode
Main Amplifier V_{GS}	-2.35 V	-2.35 V
Auxiliary Amplifier V_{GS}	-3.05 V	-2.35 V

Table 1: Bias voltages for Doherty and Balanced modes

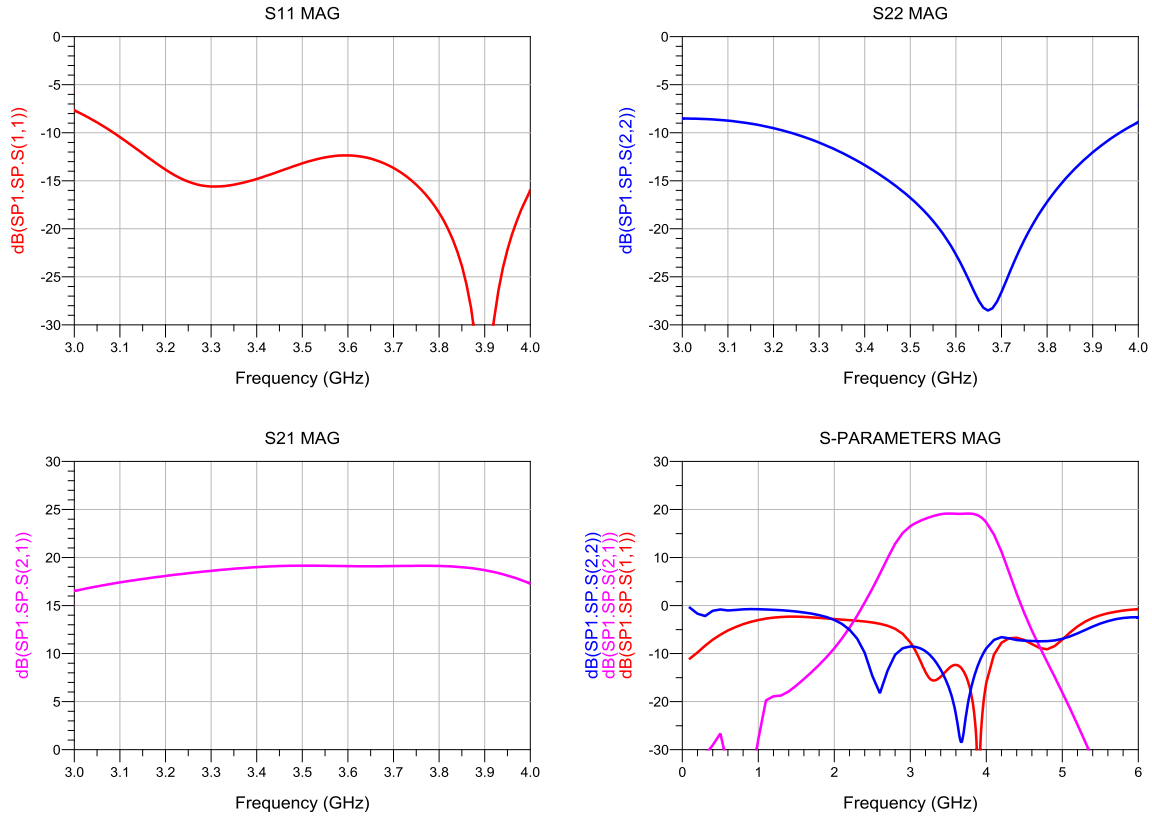

Figure 7: Simulated S-Parameters of the Doherty Amplifier

Figure 7 contains plots of the simulated S-Parameters in Doherty mode. Between 3.4 GHz and 3.8 GHz, S_{21} is > 19 dB and return losses are > 12 dB. The amplifier is unconditionally-stable in both Doherty and Balanced modes.

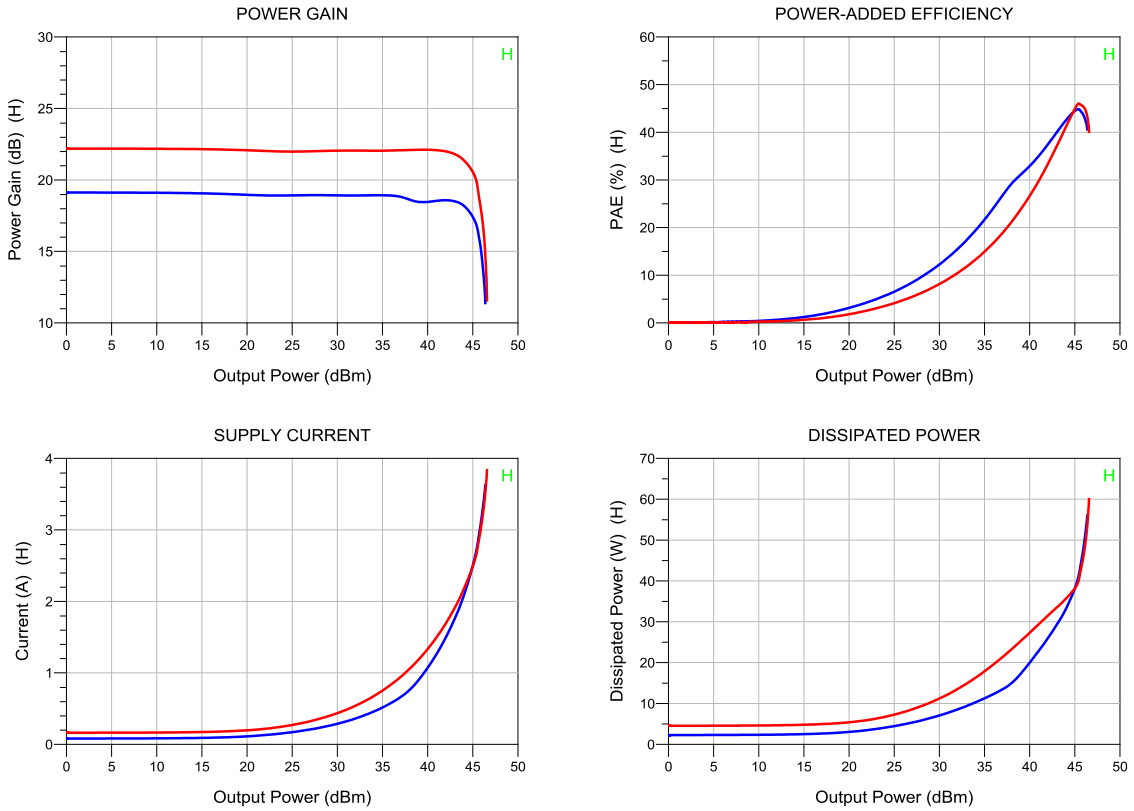

Figure 8: 3.6 GHz Swept Power Simulations – Balanced (red trace) and Doherty (blue trace) Operation

Figure 8 shows the large-signal simulation plots of the PA biased in both balanced and Doherty modes. Noticeably, Doherty operation is more efficient throughout the output power range, until convergence with the balanced-mode traces at P_{SAT}. The gain vs output power characteristic of the Doherty is quite linear, even at the point where both main and auxiliary amplifiers are in strong conduction.

Fabrication, Packaging and PCB Development

A photograph of the fabricated and diced MMIC is shown in Figure 9, with RF input to the left and RF output to the right.

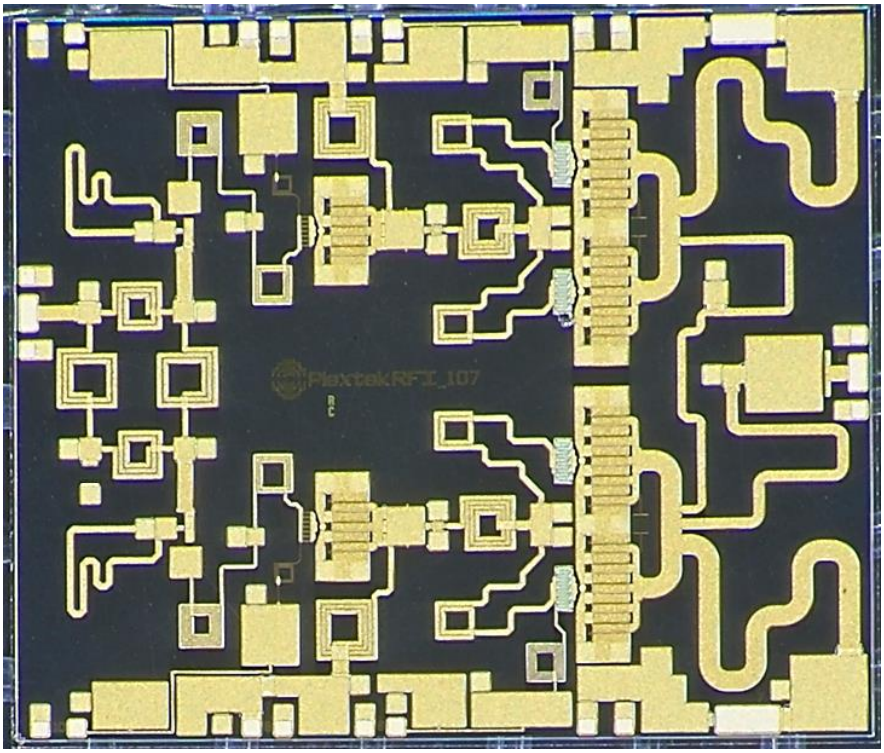

Figure 9: Photograph of the S-Band Doherty PA MMIC

A custom laminate SMT package was designed to accommodate the PA. This was an 8mm x 8mm QFN-36, which was fabricated and assembled in the UK by Filtronic. An evaluation PCB was designed to allow evaluation of the packaged part. A photograph of the evaluation PCB is shown in Figure 10.

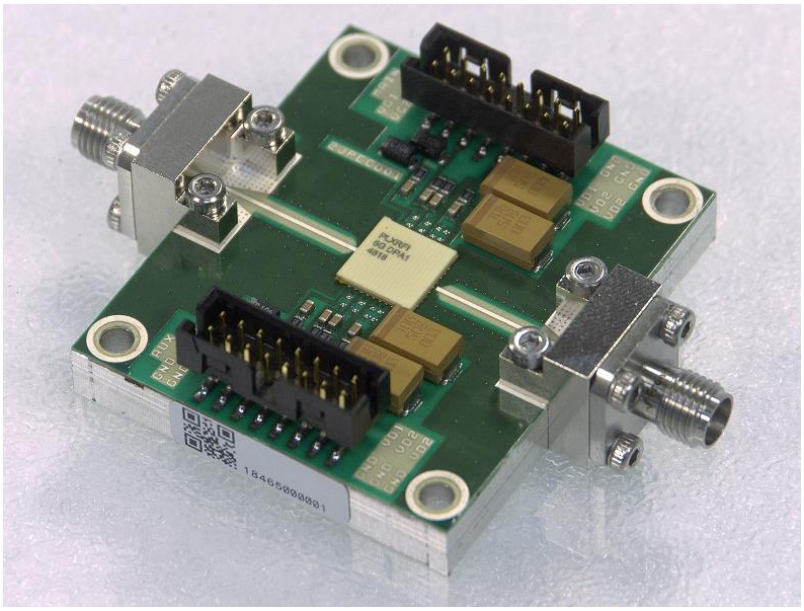

Figure 10: Photograph of the packaged PA assembled onto an evaluation PCB

The evaluation PCB was fabricated on 8-mil Rogers RO4003B on an aluminium baseplate. As well as improving the mechanical stability of the PCB, the baseplate is crucial to the thermal management of the MMIC.

Measured Performance of the MMIC

S-Parameter Measurements

A TRL calibration PCB was designed to allow the measured performance to be referenced to the ports of the package. All measured performance presented below is for the packaged PA assembled onto the evaluation PCB.

By measuring the PA in balanced mode it can also be shown how the bias of the auxiliary amplifier can be tuned for a specific application. If more gain is required the quiescent bias can be increased but at the possible expense of PAE at backoff.

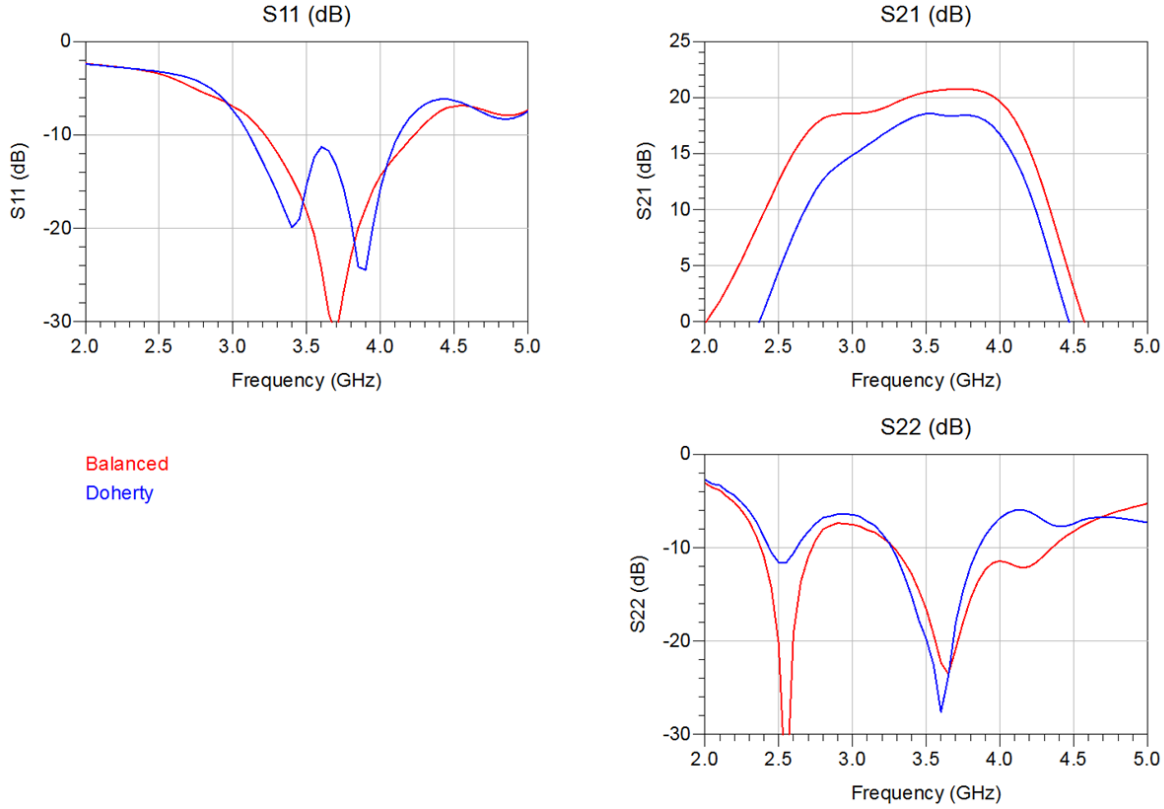

Figure 11: Measured S-parameters of 3.5GHz PA in balanced and Doherty modes

Figure 12 is a plot of the measured s-parameters (blue traces) compared to the simulated (red traces) for the PA in Doherty mode. It shows good agreement between simulated and measured small-signal performance.

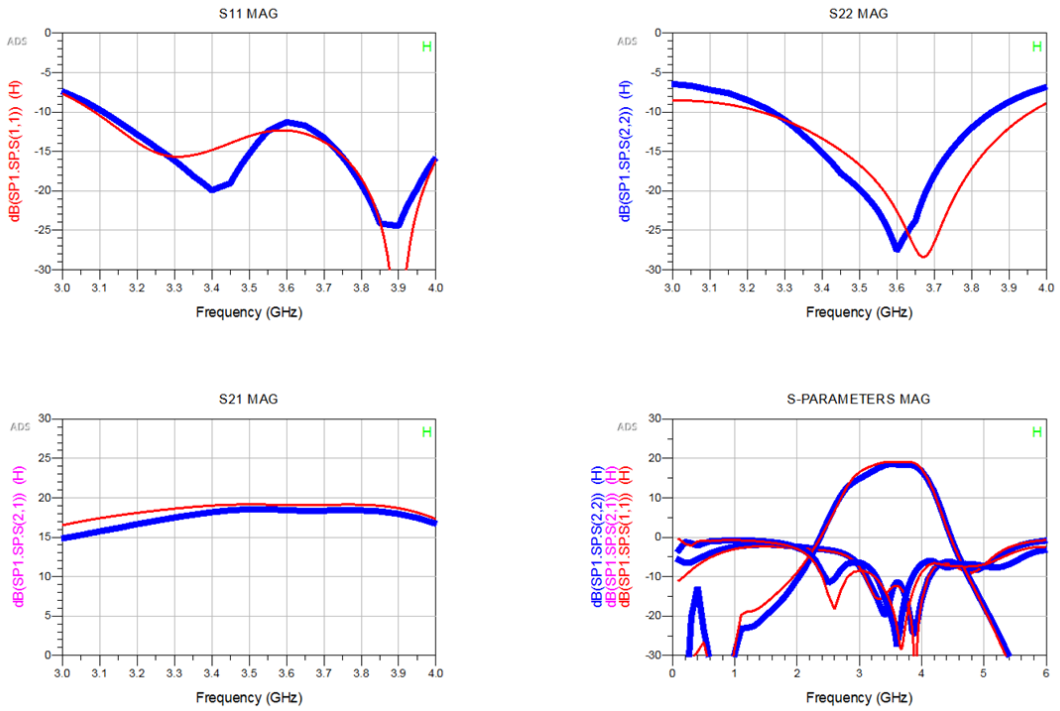

Figure 12: Measured (blue) versus Simulated (red) S-Parameters of PA in Doherty Mode

Large Signal Pulsed Measurements

When operating at its maximum output power capability, the PA is not designed to be operated under CW conditions. Pulsed measurements were made to demonstrate the peak performance of the PA. A 100 µs pulse with 10% duty cycle was used.

Figure 13 is a plot of the measured PAR versus output power. The two traces compare the performance in Doherty mode to the performance in balanced mode and clearly show that the PA exhibits significantly better PAE at backoff in Doherty mode.

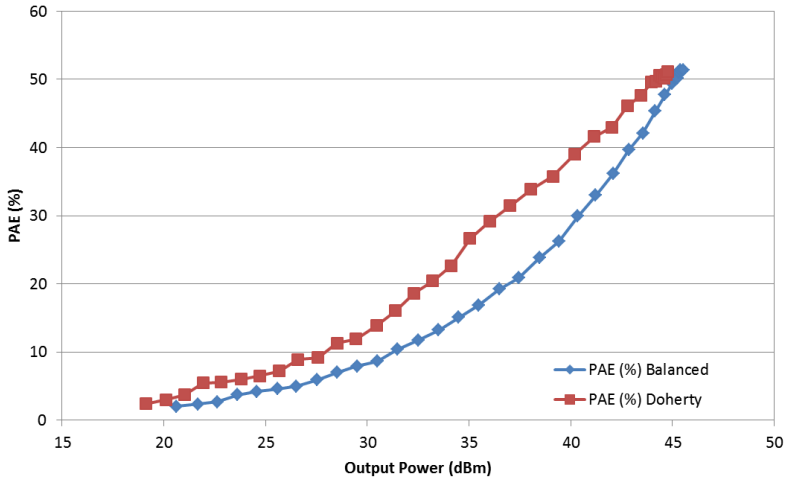

Figure 13: PAE vs Output Power for a 100µs, 10% duty cycle pulsed signal at 3.5GHz

The gain of the PA versus RF output power is plotted for both balanced and Doherty modes in Figure 14. The sharper roll-off of gain in balanced mode is evident.

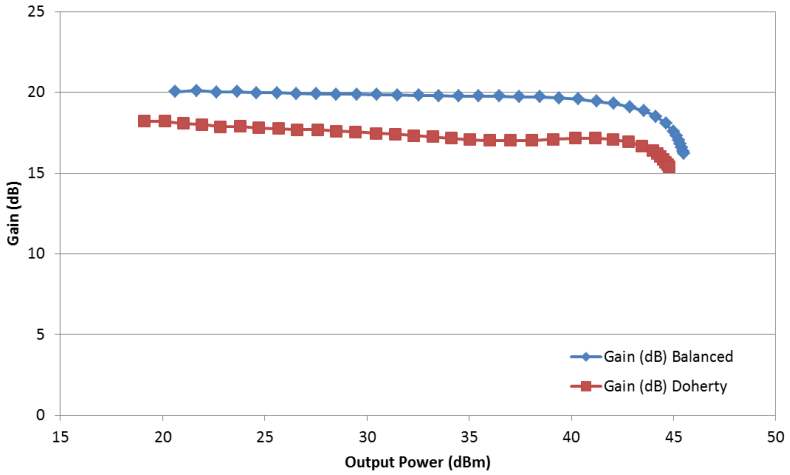

Figure 14: Gain vs Output Power for a 100µs, 10% duty cycle pulsed signal at 3.5GHz

The PAE versus output power is plotted for the Doherty mode PA across a range of frequencies (3.4GHz to 3.8GHz) in Figure 15. The measured performance is similar at the different operating frequencies.

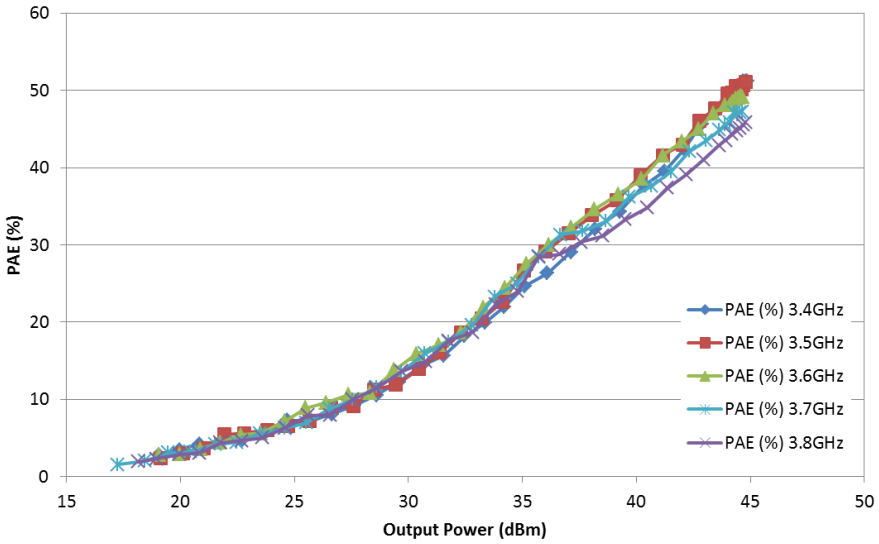

Figure 15: PAE vs Output Power for a 100µs, 10% duty cycle pulsed signal between 3.4 and 3.8GHz

5G NR Modulated Measurements

Measurements were undertaken using a 100 MHz bandwidth 5G NR downlink signal. This provides a challenging scenario with which to test the linearity performance of the Doherty PA.

As shown in Figure 16, the PA was driven with a pre-amplifier. The effect of this pre-amplifier is included in the modulated measurements, meaning that the linearity of the Doherty PA by itself is actually slightly better than the figures reported. In addition, no digital pre-distortion (DPD) was used, which would offer an opportunity for further improvements in linearity.

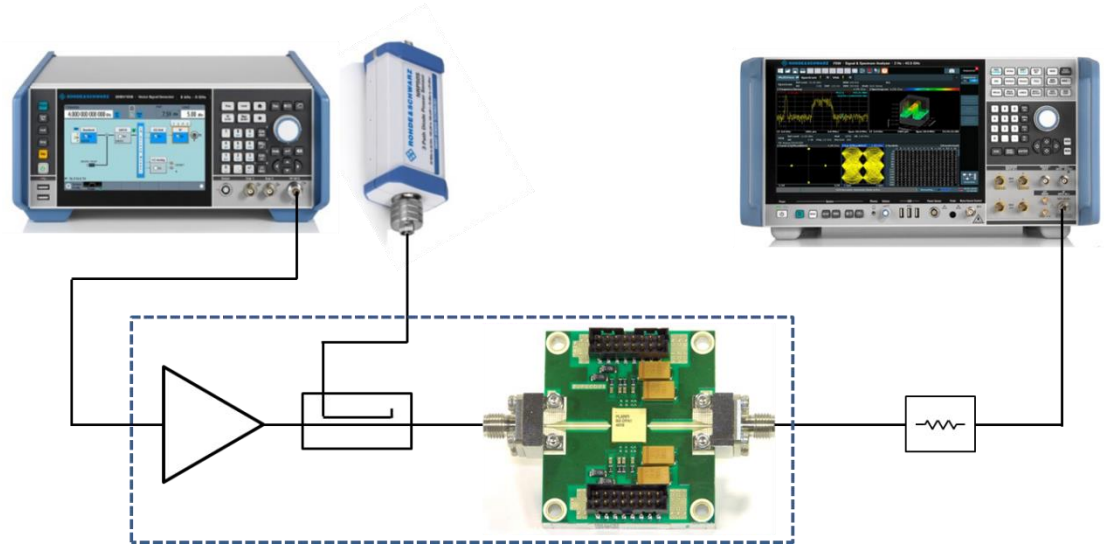

Figure 16: Measurement Setup for 5G NR Modulated Measurements

The measured ACLR (Adjacent Channel Leakage Ratio) is plotted against output power in Figure 17. Traces for the adjacent channel (ACLR 1) and the adjacent channel but one (ACLR 2) on either side of the transmission channel are plotted. At 8dB back-off (~ 37dBm out) is < -31dBc for ACLR 1 and < -41dBc for ACLR 2.

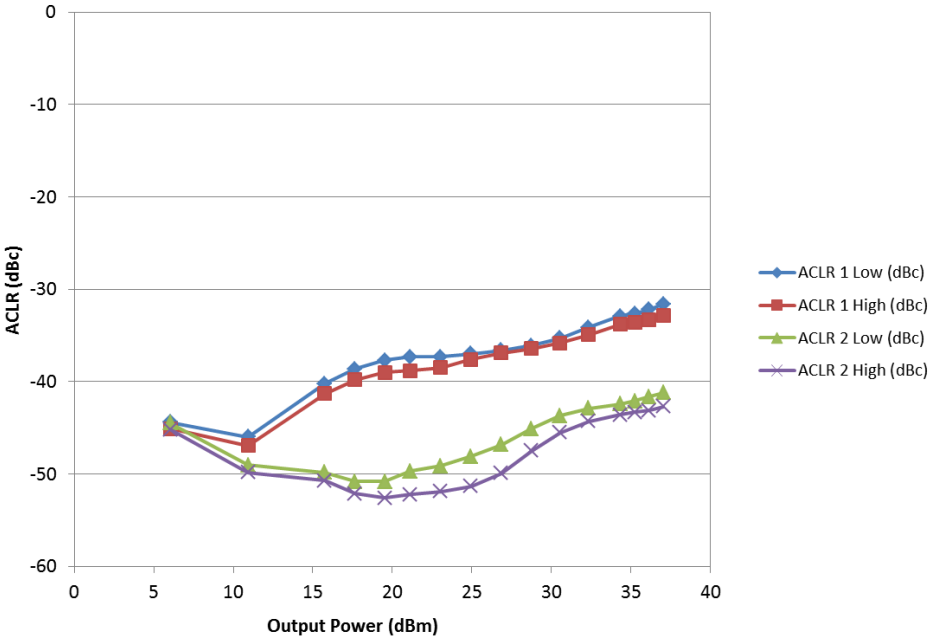

Figure 17: ACLR vs Output Power (100MHz 5G NR Signal) 3.5GHz, Doherty Mode

Conclusions

The design and evaluation of a fully integrated Doherty PA MMIC has been described. It has been packaged in a laminate QFN SMT package and measured on a representative evaluation PCB. Excellent measured performance has been demonstrated, as summarised in Table 2. This is achieved in a compact, fully integrated design requiring only low-frequency decoupling components on the PCB. First-pass design success was achieved due to careful EM-simulation of the matching networks

and accurate PDK transistor models, which is evident in the good agreement between measured and modelled performance. As well as good back-off efficiency, good linearity was demonstrated with challenging 5G NR signals and further improvement in linearity would be expected with the use of DPD.

Parameter	Measured Value
Frequency Band	3.4 to 3.8GHz
Gain	18dB (in Doherty mode) 20dB (in balanced mode)
Input return loss	>11dB
Output return loss	>12dB
P_{SAT}	45dBm
PAE at P_{SAT}	50 %
PAE at 8dB back-off	31.5 %
EVM at 36dBm (4W) P_{AVG} (5G NR 100MHz)	3.5%
ACLR at 36dBm (4W) P_{AVG} (5G NR 100MHz)	< -33dBc

Table 2: Performance Summary of the Doherty PA

Bibliography

[1] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho and B. Kim, "The Doherty Power Amplifier: Review of Recent Solutions and Trends," *IEEE Transactions on Microwave Theory and Techniques,* pp. 559-571, February 2015.

[2] S. Cripps, Advanced Techniques in RF Power Amplifier Design, Norwood, MA: Artech House, 2002.

[3] M. Ozen and C. Fager, "Symmetrical Doherty Amplifier with High Efficiency over Large Output Power Dynamic Range," 2014.

[4] S. Cripps, RF Power Amplifiers for Wireless Communications, 2nd ed., Norwood, MA: Artech House, 2006.

[5] R. Quaglia, V. Camarchia, T. Jiang, M. Pirola, S. D. Guerrieri and B. Loran, "K-Band GaAs MMIC Doherty Power Amplifier for Microwave Radio With Optimized Driver," *IEEE Transactions on Microwave Theory and Techniques,* pp. 2518-2525, 2014.