Asymmetrical Doherty Power Amplifier for 8dB Power Back Off

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Abstract

A requirement for multiple Doherty power amplifiers (DPA) covering bands within the frequency range 0.7 – 2.7GHz has led to the development of an approach for designing a highly efficient and linear DPA operating in power back-off mode (PBO) that can provide coverage in more than one band. This paper presents an approach of optimising back off efficiency for a given transistor by means of evaluating $2*R_{opt}$ 'seen' by the main amplifier cell. In addition, measurement of the passive networks is covered. This approach is demonstrated using a commercially available symmetrical LDMOS transistor on a RO4350B PCB dielectric. When evaluated using a W-CDMA 3.84MHz CHBW 7.8dB PAPR test stimulus at an RMS output power of 35.5W (+45.5dBm) the fabricated DPA achieved a drain efficiency of 47 - 50% at 8dB PBO over its operating bandwidth. ACLR was measured as >30dB and was corrected using analogue pre-distortion (APD) to ~50 -55dB.

1 Introduction

Efficiency in a power amplifier is conceptually defined as the ratio of RF output power to the total consumed power resulting from the combined sum of RF input power and DC power from a fixed DC power source, [$\eta = RF_{OUT}/RF_{IN}+DC$]. The largest contributor in the denominator of this ratio is the DC component with the RF input power only being significant in the case of a low gain amplifier. In this sense, the power amplifier as a system component can be seen as a power converter, converting a given availability of DC power to RF power with a key requirement that this is carried out as efficiently as possible. With respect to the amplifier, operating in a high efficiency mode reduces dissipated heat and in the case of a mobile operator this reduces the overall operational expenditure [OPEX] primarily through a reduction in DC power consumption and also cooling. In the case of the amplifier being cooled through convection alone then the impact is one of mechanical design; overall mass and size of the heatsink, particularly important when one considers tower mounted amplifiers and their inherent wind loading. However, from a transistor point of view then clearly a device that operates with less dissipated power can provide a higher output power for a given periphery and so in this sense overall efficiency is an important factor. The impact of modern communication standards means that modulation schemes resulting in high peak to average power ratios [PAPR] are commonplace, a typical W-CDMA scheme results in a PAPR = 7.8dB. This affects 2 key parameters of an amplifier; efficiency and linearity. Used under these stimulus conditions a typical class AB biased amplifier whilst linear in its operation, will suffer from a poor conversion efficiency that approximates to a 60% reduction relative to the peak efficiency when operated at 8dB PBO.

Whilst there are a number of solutions to efficiency enhancement such as supply rail modulation or envelope tracking [ET], there also exists a family of amplifiers referred to as load modulation. These can be realised in both active and passive formats and do not require the same level of sophisticated DC electronics 'attached' to the amplifier that ET requires. With primary examples of load modulation schemes being the 2 level Doherty power amplifier [DPA] and the Chireix power amplifier [CPA] dating back to the 1930's these have since evolved (this time period includes many years where such schemes became 'unfashionable' and languished as a lab curiosity) to include asymmetrical and multi-level DPA architectures, digital Doherty and digital Chireix variants. Furthermore, newer types have also emerged such as asymmetrical multilevel outphasing [AMO] and dynamic load modulation [DMO]. A symmetrical 2 level DPA consists of 2 equal periphery transistors, termed the main and auxiliary cells, that when combined using load modulation achieve a peak in efficiency at 6dB and 0dB PBO. Control of the PBO efficiency peak is achieved through introducing asymmetry into the periphery ratio [ξ] between the main and auxiliary cells in the amplifier, in other words deliberately creating a saturated power difference between the main and auxiliary. Using this approach then efficiency peaks at 6, 8, 10dB can be introduced and properly controlled. This paper presents and describes the design of an asymmetrical DPA for 8dB PBO that produces optimal efficiency and linearity for a given transistor.

2 Load modulation

The fundamental principle of operation of a 2 level DPA is shown in figure 1 and is commonly known as load modulation or 'active load pull'. An excellent quantitative analysis is given in [1].

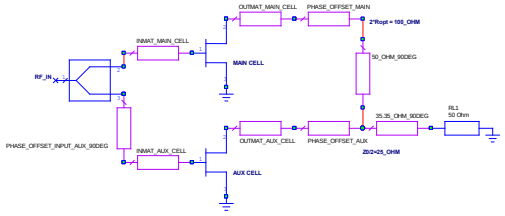

Figure 1 Conventional 2 level DPA configuration.

The conventional DPA consists of a class AB biased [main cell] and Class C biased [aux cell] amplifier both impedance matched to 50Ω. To enable the load modulation between the 2 sides the main cell is connected to one end of a 50Ω λ/4 wave inverter [node $2*R_{opt}$] and the aux cell is connected to the other end [node $Z_o/2$]. Finally a 35.35Ω λ/4 transformer is used between node $Z_o/2$ and the 50Ω output port. Figure 2 shows the effect load modulation has on efficiency for a given power back off level and how the cell periphery ratio controls the first efficiency breakpoint.

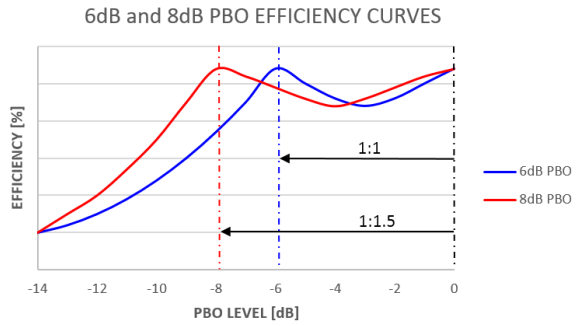

Figure 2 Efficiency curves for 6dB and 8dB back-off with corresponding cell periphery ratios.

To understand this effect qualitatively consider a sine wave applied to the RF_IN port of the DPA. The applied wave travels through the main cell 90 degrees ahead of the same wave travelling through the aux cell. Upon arrival at the inverter stage these waves still maintain their respective 90 degree phase separation creating a potential difference across the inverter. The drive level dependency of the class C aux cell means that this cell is only active in the upper part of the PBO regime and thus we create 2 states:

$$Main_{ON}/Aux_{OFF}$$

$$Main_{ON}/Aux_{ON}$$

During state $Main_{ON}/Aux_{OFF}$ no load modulation occurs and working the impedances back from the 50 Ω output port to the node $2*R_{opt}$ results in the main side 'seeing' a 100Ω impedance. In the state $Main_{ON}/Aux_{ON}$ then the voltage waveform at node $2*R_{opt}$ is 90 degrees ahead of the voltage waveform at node $Z_o/2$ and the resulting potential difference across the inverter results in the voltage being halved. This means the impedance at node $2*R_{opt}$ is also halved such as in [4]:

$$V/2 = (2*R_{opt})/2 \quad = 50\ \Omega \quad [4]$$

Hence when both cells are active in the upper part of the power back off region they 'see' 50Ω.

The effect of this on the amplifier load line is that it is modulated between these states as shown in figure 3. This creates 2 efficiency peaks, the first at power back off level for load line $2*R_{opt}$ and the second at 0dB power back off level for load line R_{opt}. In doing this the rail-to-rail voltage swing, and hence efficiency, is maintained over the back off power range. Although classically proven and defined as $2*R_{opt}$ then what is less well understood is the effect that this node impedance has on the power back off efficiency and also the interaction between the compression in the main cell and the aux cell turning on. The reality of any amplifier design is that transistor knee voltage effects [V_{knee}] and non-ideal parasitics lie between the current generator and package planes and so it is logical to conclude that node $2*R_{opt}$ = 100Ω does not always result in optimal performance between main and aux cells, and hence efficiency and linearity of the final DPA. The load line in figure 3 shows an ideal scenario [V_{knee} = 0V and $1/R_{on} = \infty$] where the load is modulated between 50Ω and 100Ω, this does not account for knee voltage effects and the resulting effect on the value of $2*R_{opt}$.

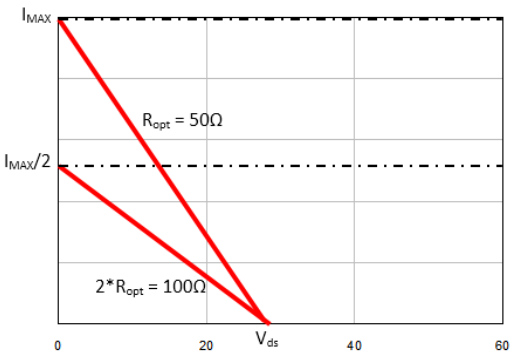

Figure 3 Effect of load modulation on ideal amplifier load line.

3 DPA design

3.1 Device periphery calculation

The design of any amplifier design should begin with a technology review and device selection based on a known output power [including all passive losses] and input signal stimulus. Of particular importance is the average output power the amplifier is required to operate at and the signal PAPR from this, a peak power requirement can be derived simply from (1):

$$P_{peak} = P_{avg(+losses)} + PAPR \quad (1)$$

In this case the transistor technology was fixed at LDMOS due to the need for the amplifier to work side-by-side with other LDMOS based amplifiers and easily integrate with an existing DC design. The application requires that the average power is +45.5dBm. Including passive losses then this increases to +46dBm. The stimulus PAPR = 7.8dB and so the peak power requirement is (2):

$$P_{peak} = 46 + 7.8 = +53.8dBm\ [239W] \quad (2)$$

Therefore the transistor peak power requirement is a minimum of 239W. [It's worth mentioning that a practical design would also account for saturated power [Psat] degradation over temperature, measurement uncertainty and also system power set accuracy, all of which serve to increase the minimum power requirement placed on the transistor]. For a linear amplifier this is a straight forward procedure but the device selection process developed here for a DPA is somewhat different due to the fact that there exists a main and auxiliary cell. As previously mentioned in the case of a DPA, output power back off is controlled by the size ratio that exists between the main and auxiliary cells, if the size ratio is known then the PBO level is defined as in (3):

$$PBO = -20.\log\ [1+\xi] \quad (3)$$

A larger output power back off can be implemented by increasing the size ratio as in table 1:

PBO [dB]	Periphery Ratio [ξ]
6	1:1
8	1:1.5
10	1:2

Table 1 Power back off vs cell periphery ratio.

In terms of the saturated power difference [ΔP_{sat}] between main and aux cells expressed in dB, the output back off level is approximated as in (4):

$$PBO = 6 + \Delta P_{sat}.10^{(\Delta Psat/20)} \quad (4)$$

From this analysis a minimum device peak power of 239W with a cell ratio of x1.5 is required.

3.2 Transistor selection

The LDMOS device used in the DPA is designed for operation in the 600 – 900MHz band and is based on a plastic package, fabricated on a Si process rated with a peak power of 270W operating from a +28V drain supply [V_{ds}], a performance summary outline is shown in table 2.

Idqmain (mA)	Vgspeak (V)	P3dB (W)	Drain Eff (%)	Gp @ P3dB (dB)	BVd (V)	Ron (mΩ)
500	0.5	~270	~60	>14	65	~90

Table 2 Transistor performance summary.

It is worth noting that more often than not the choice of device is often in itself, sub optimal and a nearest solution 'trade-off' has to be made. This is particularly true of the main transistor which, as a result, often ends up being overpowered for the task. The leading factors that cause this are; frequency of operation, device technology and peak power requirement.

3.3 Transistor model validation

A large signal compact model was obtained from the device manufacturer for use in the load pull and non-linear analysis. Validation of the transistor model begins with graphing MAG/MSG and K factor vs frequency as shown in figure 4. This shows that although the transistor is a discrete device the manufacturer has provided some internal tuning at the input to optimise performance in the 600 – 900MHz band, the transistor has been internally stabilised in band with only low frequency gain reduction being required. Note the internal resonance at ~500MHz.

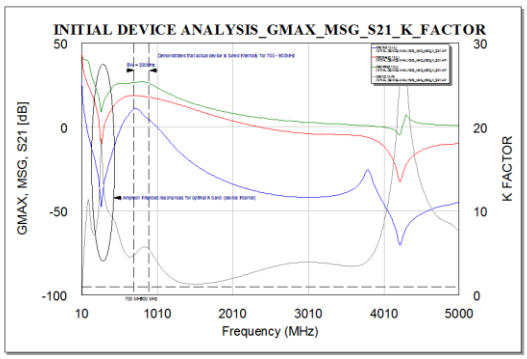

Figure 4 GMAX, S21 and K factor for transistor.

An initial manual load pull run was performed to verify the power performance parameters of the main and auxiliary cells prior to a full load pull run as shown in figure 5.

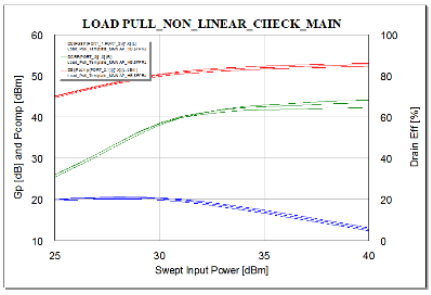

Figure 5 Initial non-linear model validation.

3.4 Optimal load impedance extraction

Design of the DPA begins with load and source pull of the transistor in NI MWO. In this case a single MDIF file has been created by 'nesting' the load and source pull gamma points together. The transistor is actually symmetrical, however a load pull analysis can be used to not only determine optimal gamma points with respect to power, efficiency and gain but also to create asymmetry between cells. Figure 6 shows the load pull contours at a constant compression and the resulting Z_{Lopt} for main and auxiliary transistors. [Note the smith chart is normalised to $Z_o = 12\Omega$ for contours].

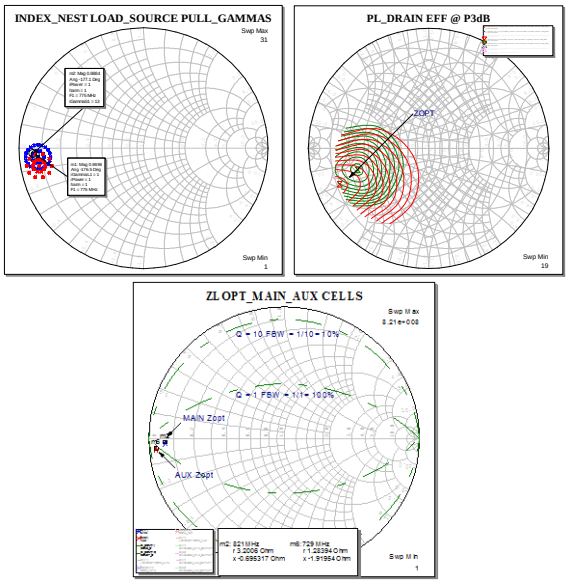

Figure 6 Nested source and load pull gamma points with load pull contours at a constant compression (top). The resulting Z_{Lopt} for main and auxiliary transistors (bottom).

The previous analysis in section 3.1 estimated that we require a cell ratio of x1.5 between saturated powers and so using a proposed efficiency match on the main transistor and a power match on the aux transistor an asymmetry can be introduced between the two. Based on the load pull analysis impedances for main and aux cells can be matched to provide a x1.5 cell ratio. A useful analysis here is the use of a swept variable load pull approach that can investigate the effect of a number of variables such as bias, drain voltage and load pull gamma point. Figure 7 shows drain efficiency as a function of gamma point, the red trace represents the active gamma, with all other grey traces representing all gamma points in the load pull file.

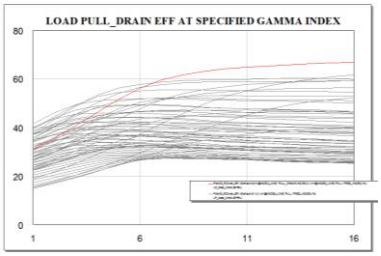

Figure 7 Drain efficiency as a function of swept load pull gamma points.

3.5 Network synthesis

Having obtained Z_{Lopt} for each cell then the load network design and synthesis was performed to realise a mixed planar / lumped element topology. The technique used in designing the networks is described in more detail in [2] and involves using a simplified real frequency technique (SRFT) to design the ideal real to real lumped element network and then convert to a planar / lumped format before EM simulation of the network. As one would expect given the frequency and bandwidth, the EM results agree closely with the predictions of the circuit-based models but as in [2] EM simulation is seen as an important step in reducing uncertainty in the fabricated design. Figure 8 shows the EM model and network insertion loss / reflection.

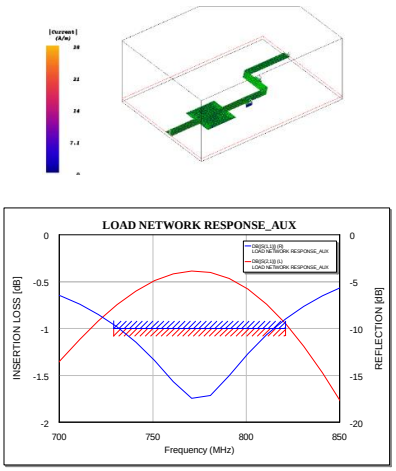

Figure 8 EM model of output matching network (top). Load network loss and reflection as a function of frequency for aux cell load network (bottom).

A further analysis can be used to evaluate the efficiency of the designed network against what is theoretically possible for the given bandwidth and transform ratio using a specific number of sections. This is done by comparing the operational power gain i.e. internal dissipative loss only to transducer power gain i.e. including effects of mismatch loss for the network, the results of which are shown in figure 9.

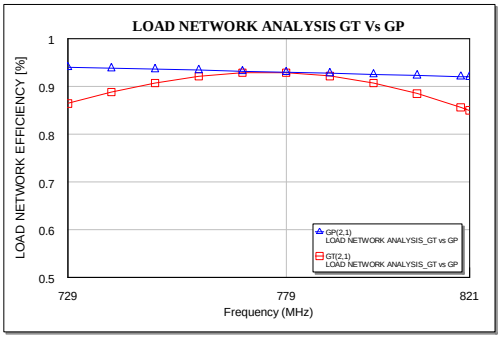

Figure 9 Load network operational vs transducer power gain comparison.

3.6 Inverter design with non-ideal R_{opt}

The knee voltage of the device can be calculated from the R_{on} parameter of the transistor. The R_{on} value is based on a drain voltage of +28V and a maximum drain current of ~7800mA. For the device then R_{on} = 90mΩ and therefore a knee voltage of 0.7V is derived. The effect of $V_{ds} - V_{knee}$ is to increase the voltage swing of the main cell and hence increase the expected output power as in figure 10.

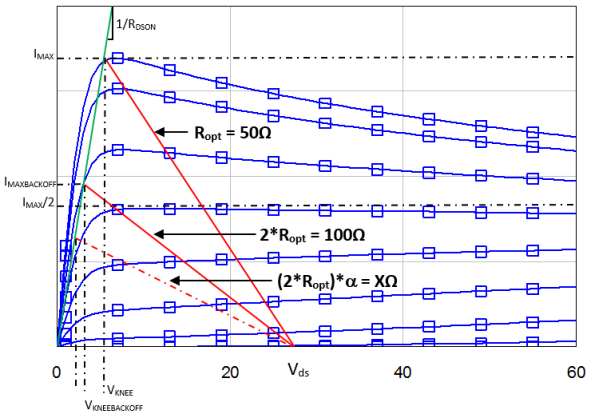

Figure 10 Effect of transistor knee voltage on amplifier load line.

In turn, this affects the efficiency at the output back off level and also the compression point of the main cell relative to the aux cell turning on. Under this non-ideal condition and in order that optimal back off efficiency be maintained, the value of $2*R_{opt}$ is increased to >100Ω to correct for the knee effect in the transistor.

In order to demonstrate this experimentally the load value at the output of the main cell was varied with 100, 115 and 125Ω as shown in figure 11.

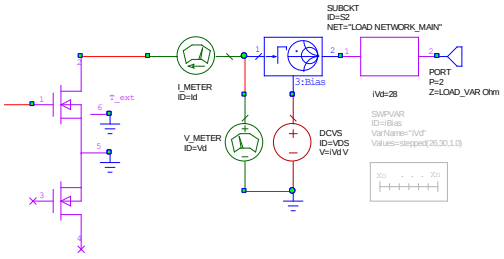

Figure 11 Load variation of main cell.

The resulting drain efficiency curves plotted for 8dB power back off are compared in figure 12. From this it can be seen that as the load is varied then due to the amplifier saturation point changing the efficiency at back off changes. At $2*R_{opt}$ = 115Ω the highest efficiency was achieved.

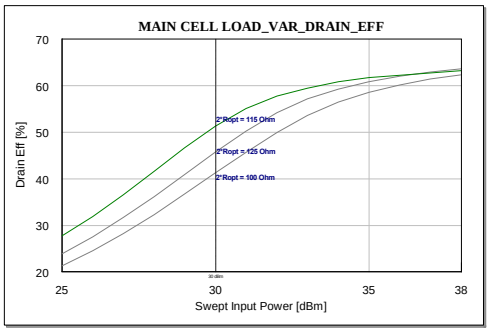

Figure 12 Load variation of main cell for drain efficiency.

Due to the over powered nature of the main cell size it does not saturate at the back off point but the efficiency at this point can be maximised as far as possible. Additionally, the compression relative to back off can also be seen to vary with the $2*R_{opt}$ impedance as in figure 13.

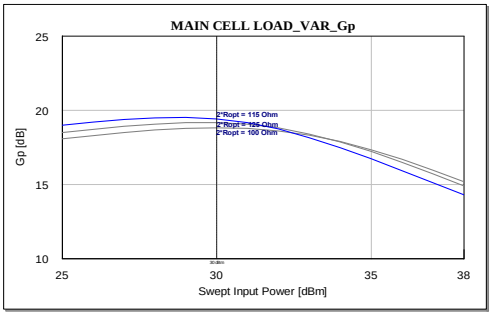

Figure 13 Load variation of main cell for power gain.

From this it can be observed that when varying the impedance of the main cell between 100 - 125Ω it

effects both the back off efficiency and the compression characteristic.

Having determined the impedance at node 2*R_{opt} then the inverter was designed based on ideal transmission lines and then converted to a planar construction for fabrication shown in figure 14. It follows that as 2*R_{opt} = 115Ω then the impedance at the combining node Zo/2 is now expected to be 21.7Ω. A λ/4 transformer was then placed between the combining node and the 50Ω output.

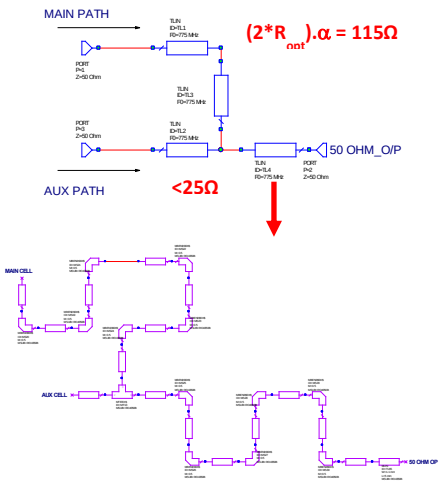

*Figure 14 Inverter realisation with modified 2*R_{opt} node.*

3.6 Phase offset design

In order that both cells of the DPA maintain their respective phase synchronisation then phase offset lines are commonly used as shown in section 2, figure 3. Moreover, it is critical that the auxiliary cell remains isolated from the carrier cell [3] at back off with respect to current leakage, if this impedance is insufficient then current is drawn from the main cell toward the auxiliary. In order to achieve this, a phase offset line can be introduced at the output of the aux cell matching network. Typically the off state impedance without the offset line is low and as such the line must rotate this impedance clockwise to a high impedance at band centre. Clearly the phase length of this line is frequency dependent and in this case the electrical length has been minimised by means of a series L shunt C topology as shown in figure 15 and converted to transmission line. This same offset line is applied at the main cell output to ensure the 2 sides sum in phase.

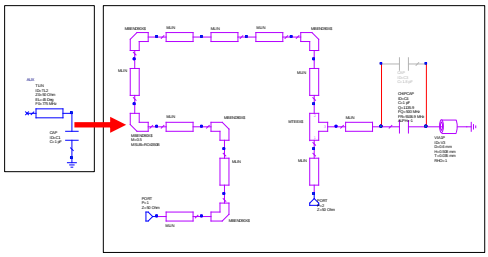

Figure 15 phase offset line design.

3.7 DPA behavioural model

A model of the DPA is presented in figure 16 showing input matching network, output matching network, phase offsets and the inverter. The model is based on a co-simulation approach that has been developed, meaning that all elements of the amplifier such as the transistor, matching networks, bias lines, phase offsets and inverter are treated as independent designs which are then combined to create an overall model.

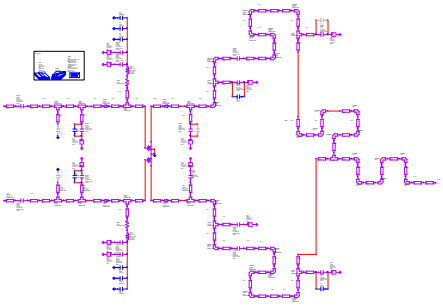

Figure 16 DPA schematic.

The model performance of the DPA is shown in figure 17 and indicates ~50% drain efficiency at power back off.

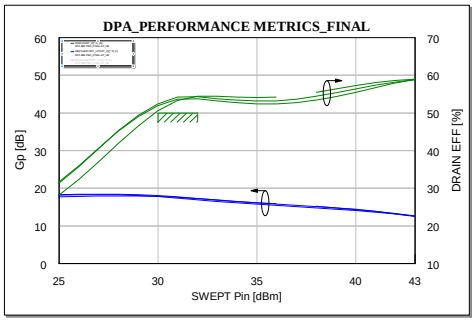

Figure 17 modelled DPA performance.

The simulated load modulation in figure 18 can be shown as a function of power and is observed to modulate the node impedance between 115Ω and 50Ω as the drive level is increased.

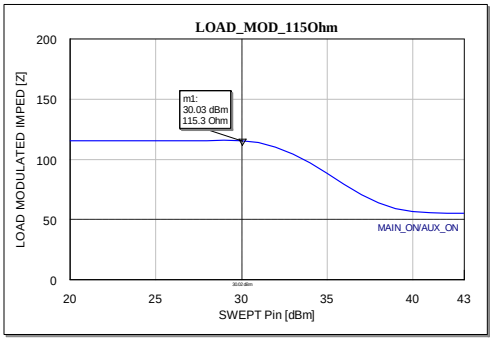

Figure 18 Load modulation value of main cell.

4.0 DPA measurement

To validate the approach, the RFPA was fabricated on Rogers 4350B 20 mil dielectric (ε_r = 3.48) as shown in Fig. 4 (a). The circuit was mounted on a jig consisting of: the source network (INMAT), load network (OUTMAT), and a copper centre section to mount the device which was required to have its source soldered down.

4.1 Passive measurements

Passive measurement and the methods used have been covered in more detail in [2] but measurement of passive networks is seen as an important part of design verification. The fabricated PCB is shown in figure 19 prior to assembly of lumped components.

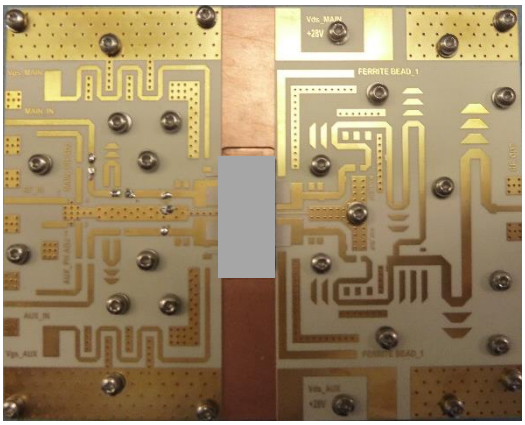

Figure 19 Fabricated DPA.

In addition to source and load impedances then the phase offset for the aux side and the resulting off-state impedance was also measured. Figure 20 and 21 shows the measured source and load impedances over the band compared to the model.

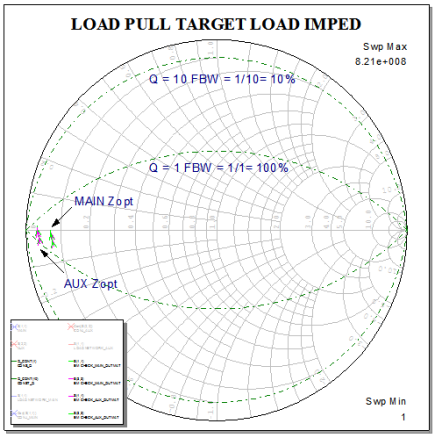

Figure 20 Load network model vs measured for main and aux sides.

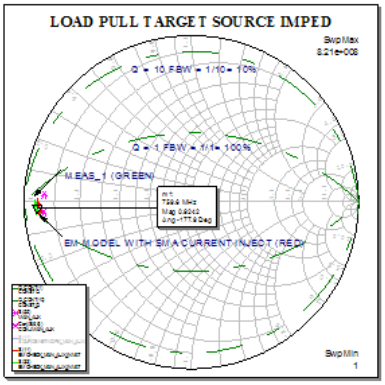

Figure 21 source network model vs measured for main and aux sides.

The off-state impedance for the auxiliary cell at the end of the phase offset looking back toward the aux cell was measured and is shown in figure 22.

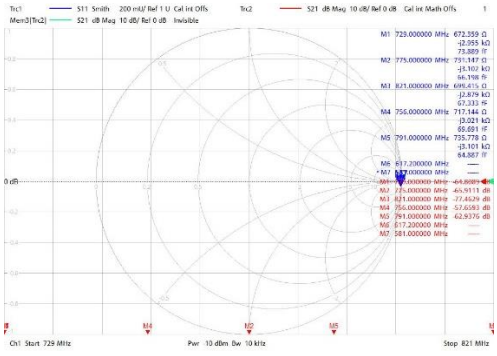

Figure 22 off-state impedance of aux side cell.

Measurement of the inverter network is shown in figure 23 and is shown to create the required 115Ω.

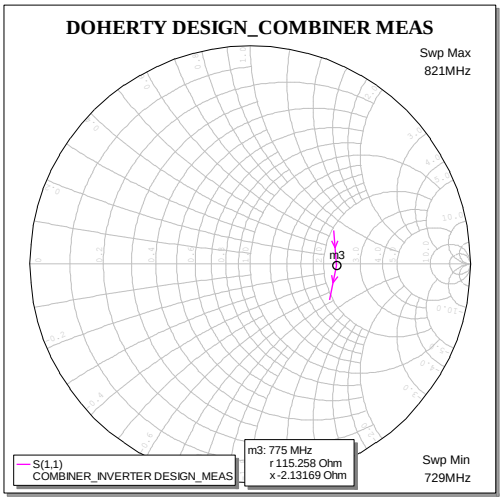

Figure 23 Combiner main cell side measured.

4.2 Small signal measurements

Linear gain and match of the DPA was measured across 729 – 821MHz therefore covering 2 band requirements of 729 – 756MHz and 791 – 821MHz as in figure 24. The same drain voltage of +28V was used for both main and aux sides with I_{dqMAIN} = 550mA and V_{gsAUX} = 0.4V.

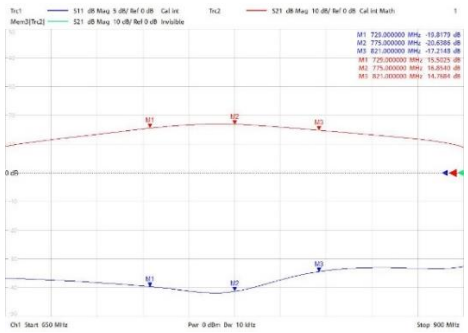

Figure 24 small signal gain measurements for DPA.

4.3 Modulated measurements

Modulated measurements were performed using the same bias as for the linear measurements. To provide a linear test signal the source was fed into a linear driver amplifier prior to being fed into to the DPA RF_IN port. Table 3 shows the measured efficiency and linearity performances using a 3.84MHz CHBW W-CDMA test stimulus with PAPR = 7.8dB. Target output power for the DPA was +45.5dBm [35.5W] with the raw linearity to be corrected by means of an analogue pre-distorter [APD] module.

Final corrected ACPR was targeted to achieve >45dB ACLR. Table 3 summarises the modulated performance.

FREQ [MHz]	Pout [dBm]	PBO [dB]	ACPR [dB]	Drain Eff [%]	DPA Model Drain Eff
729	45.5	8	31	48	51
775	45.5	8	33	50.5	52
821	45.5	8	35	47	50

Table 3 Measured ACLR and drain efficiencies.

A plot of uncorrected DPA performance measured against a 3GPP FWD spectral mask is shown in figure 25.

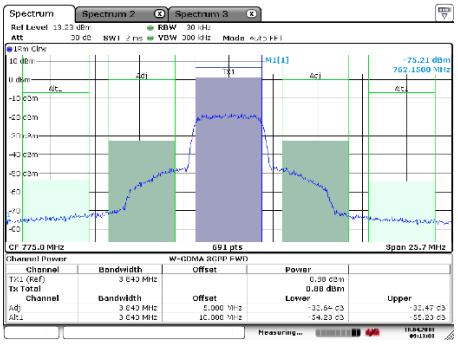

Figure 25 Uncorrected linearity measurements for DPA.

APD corrected performance for the low band is shown in figure 26.

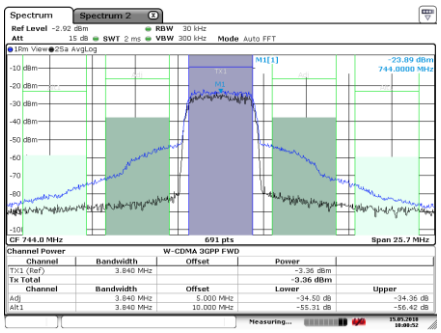

Figure 26 APD corrected linearity measurements for DPA.

4.4 Further work

The technique presented in this paper has provided an initial investigation into the effect of transistor knee voltage on DPA performance at power back off. Further work is underway to integrate this into load pull using swept variables to provide sets of contours with a varying $2*R_{opt}$ node impedance to provide further analysis and possibly performance at power back off.

4 Conclusion

A DPA covering 2 required bands with modified inverter impedance has been presented and a symmetrical transistor has had asymmetry introduced by means of a detailed load pull analysis on each side. Although the technique is limited by choice of transistor then it has been possible to optimise the back off performance and linearity of the DPA, despite an 'overpowered' main cell, by means of accounting for the knee voltage. Further increases in performance could be obtained by greater freedom in the selection of transistor technology and more importantly transistor periphery sizing of the main cell. It is also recognised that the linearity performance has been achieved, at least in part, by the larger than necessary main cell power capability.

References

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