Touch is the new click…™

- Innovision is enabling the next generation of RFID/NFC ICs
- Pushing the limits of multi-protocol, multi-frequency, standards-driven, size-engineered miniature RFID/NFC design
- Full system solutions, antenna modelling, from concept to production

Adaptation of Digital Testers for Highly Parallel Testing of Passive RFID Devices

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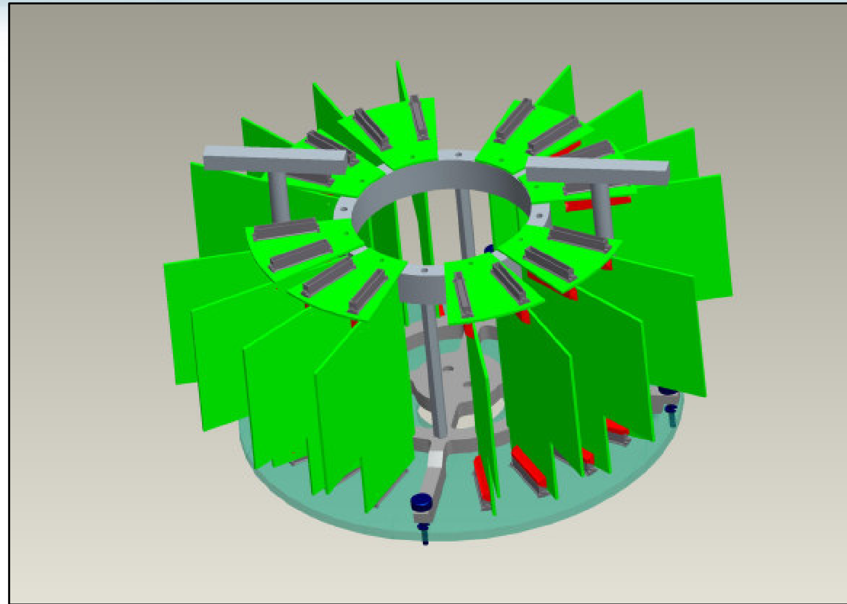

Adaptation of Digital Testers for Highly Parallel Testing of Passive RFID Devices

by
Andy Pienkowski
Innovision Research and Technology plc.

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1. The Need for Highly Parallel Testing of RFID Devices
2. Problems with Highly Parallel Testing of RFID Devices
3. Hardware for RFID Testing with Digital Testers
4. Example Vertical Test Head Layout
5. Handling UIDs within a Digital Test Environment
6. The Future of RFID Testing at IRT

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- A wafer with 70000 devices would require very long test times: >24 hours testing individual devices!
- This is prohibitively expensive for low cost (throwaway) RFID components!

Need for Highly Parallel Testing

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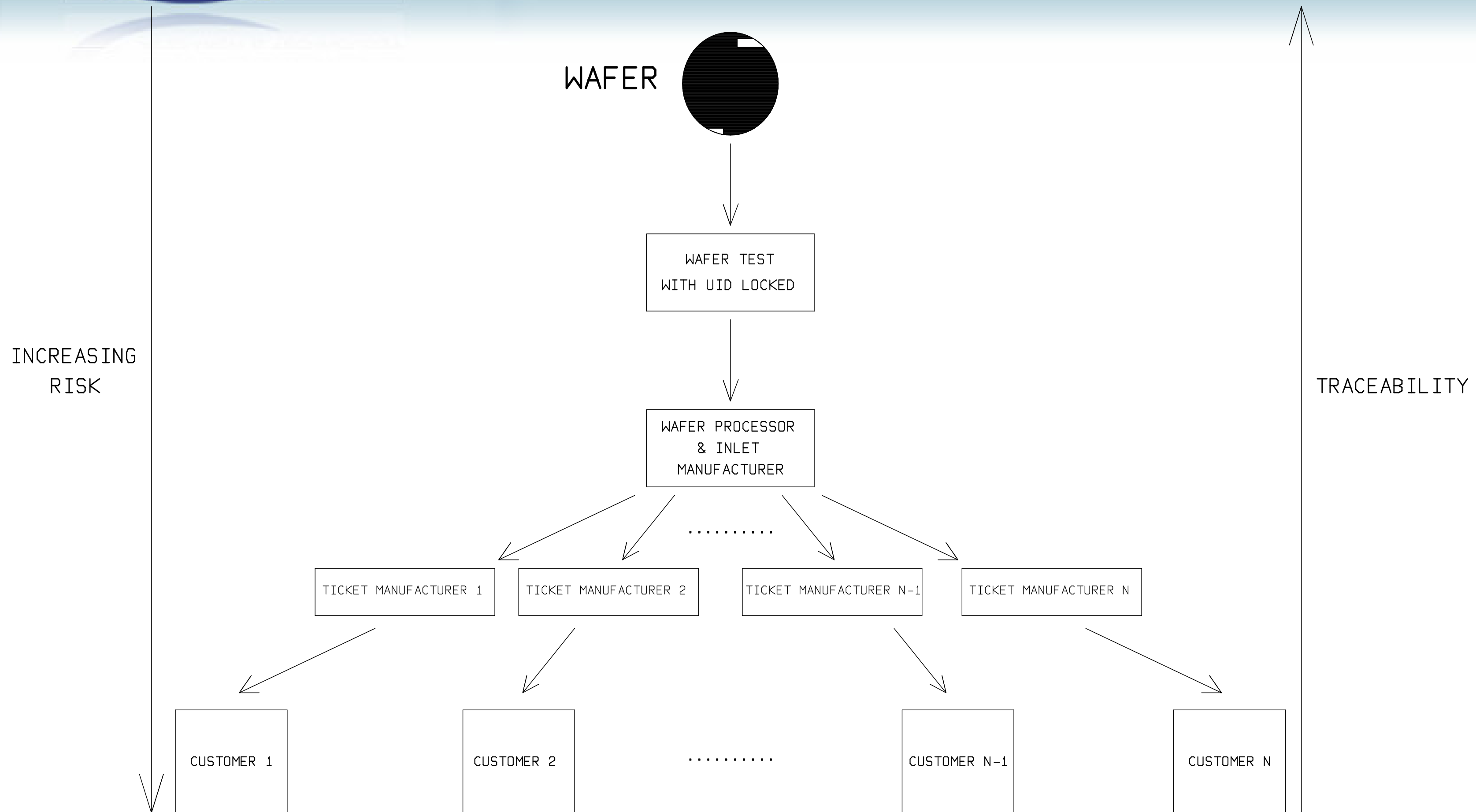

- UID "locked in" in one touchdown after other digital & parametric tests

Single Point RFID Testing

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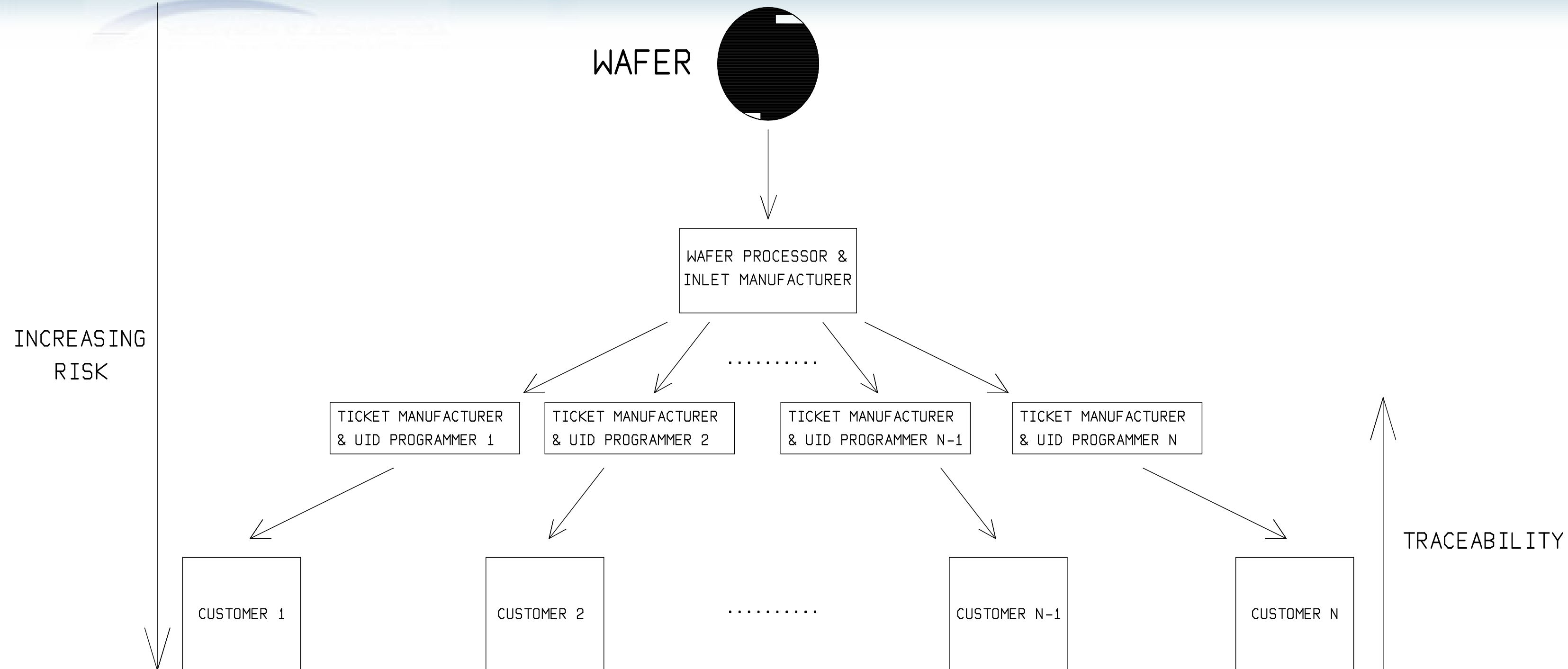

- RFID wafer not tested: processed directly as tickets
- No traceability before ticket manufacture
- UIDs are not locked before conversion to tickets

Multi-Point RFID Testing

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- Devices tested in close proximity can suffer from crosstalk
- Unique identifiers must be “locked in” to each device: digital testers traditionally test devices using the same (non-unique) procedure for each touchdown!

Problems with Highly Parallel RFID Testing

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Highly Parallel Test Hardware: Adapt Single Site Driver Functionality to a Standard Tester

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Highly Parallel Test Hardware: Adapt Single Site Response Functionality to a Standard Tester

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- Necessary to replicate single site hardware N times for N sites!
- Densely packed hardware can lead to crosstalk problems.
- How to handle unique identifiers using a tester designed to carry out the same test on all devices?

Problems with Highly Parallel RFID Test Hardware

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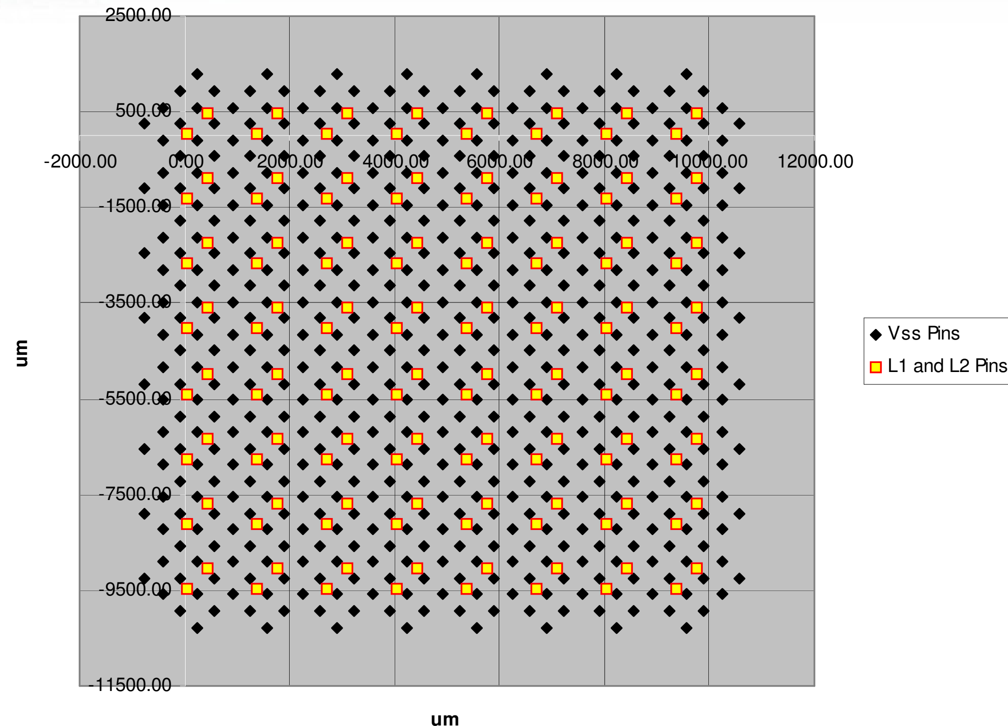

Highly Parallel Test Hardware: Example Vertical Test Head Layout

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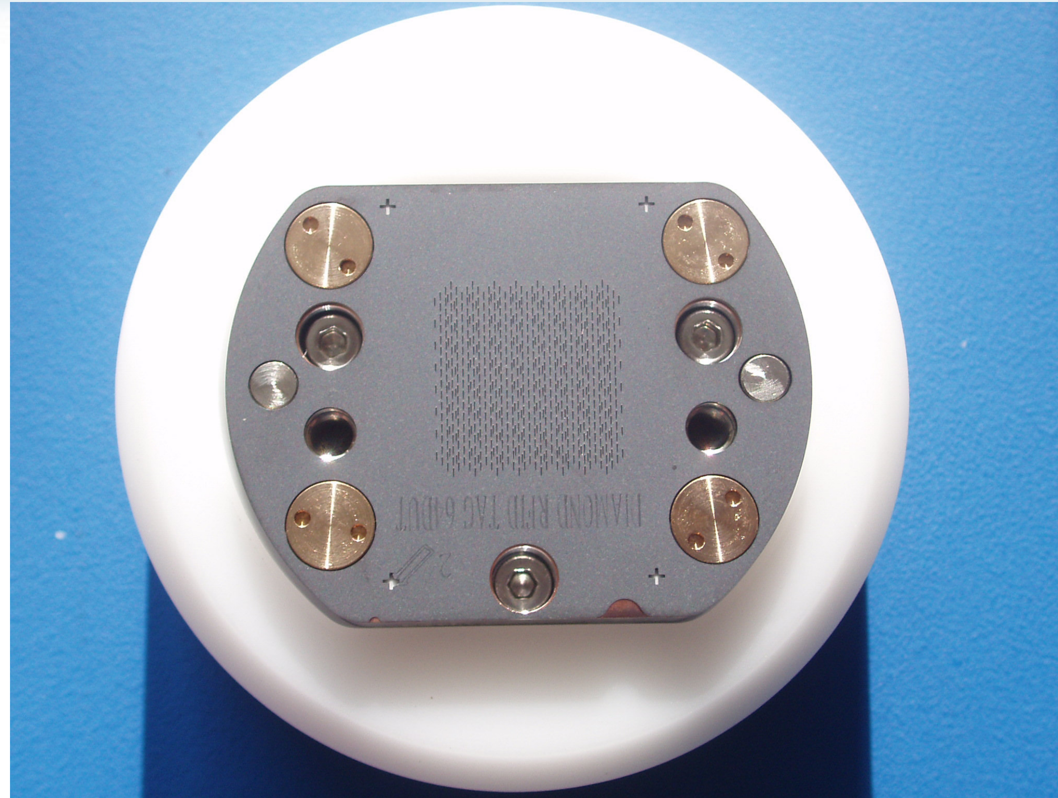

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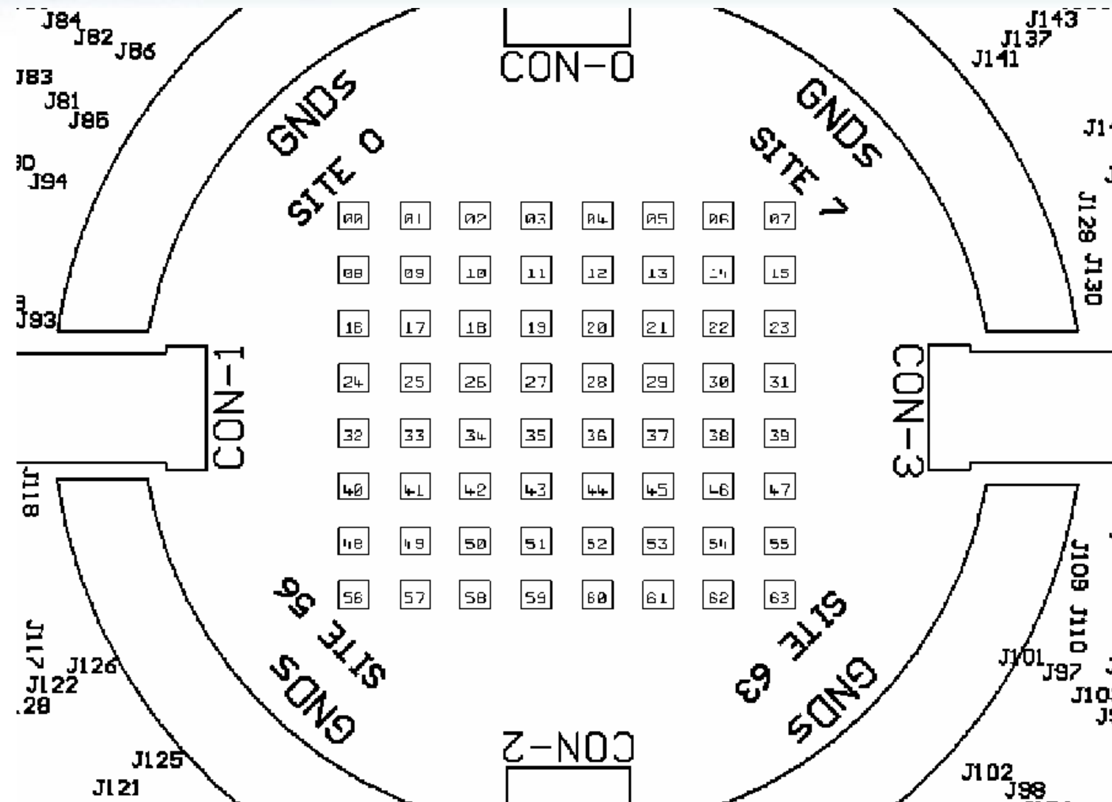

Highly Parallel Test Hardware: Example Vertical Test Head Layout

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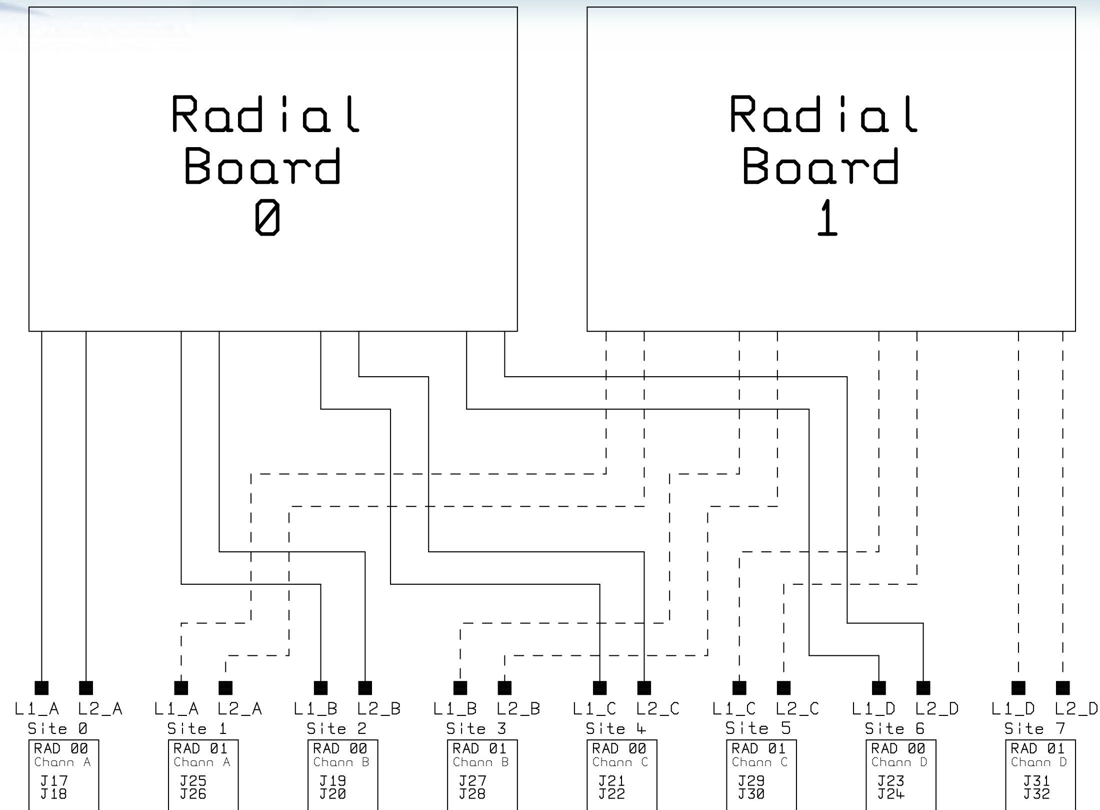

Highly Parallel Test Hardware: Cross Talk Reduction

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- Create hooks into pattern files through which data can be manipulated on the fly under program control.
- Keep the number of symbols to be manipulated per touchdown to a minimum.

Handling UIDs within a Digital Tester Environment

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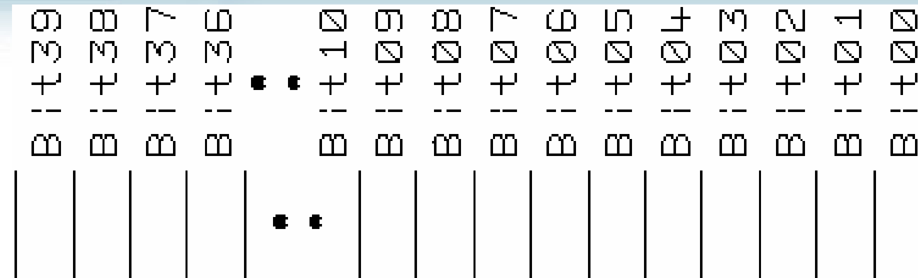

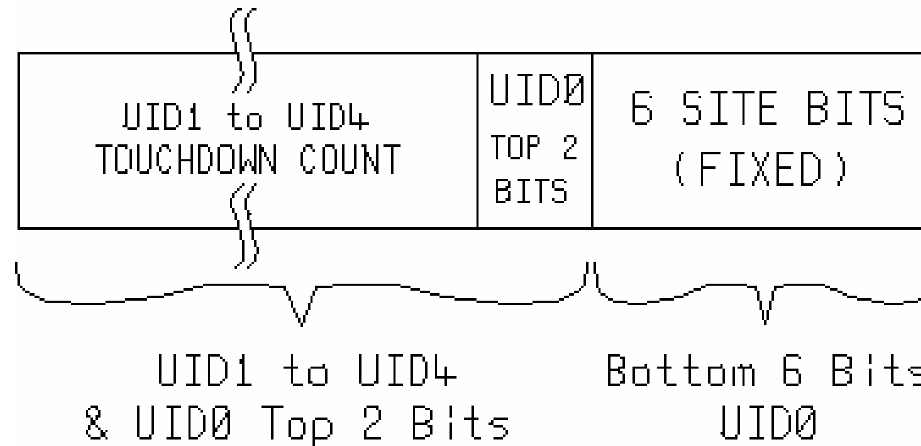

Reduced Bit Handling of UIDs within a Digital Tester Environment

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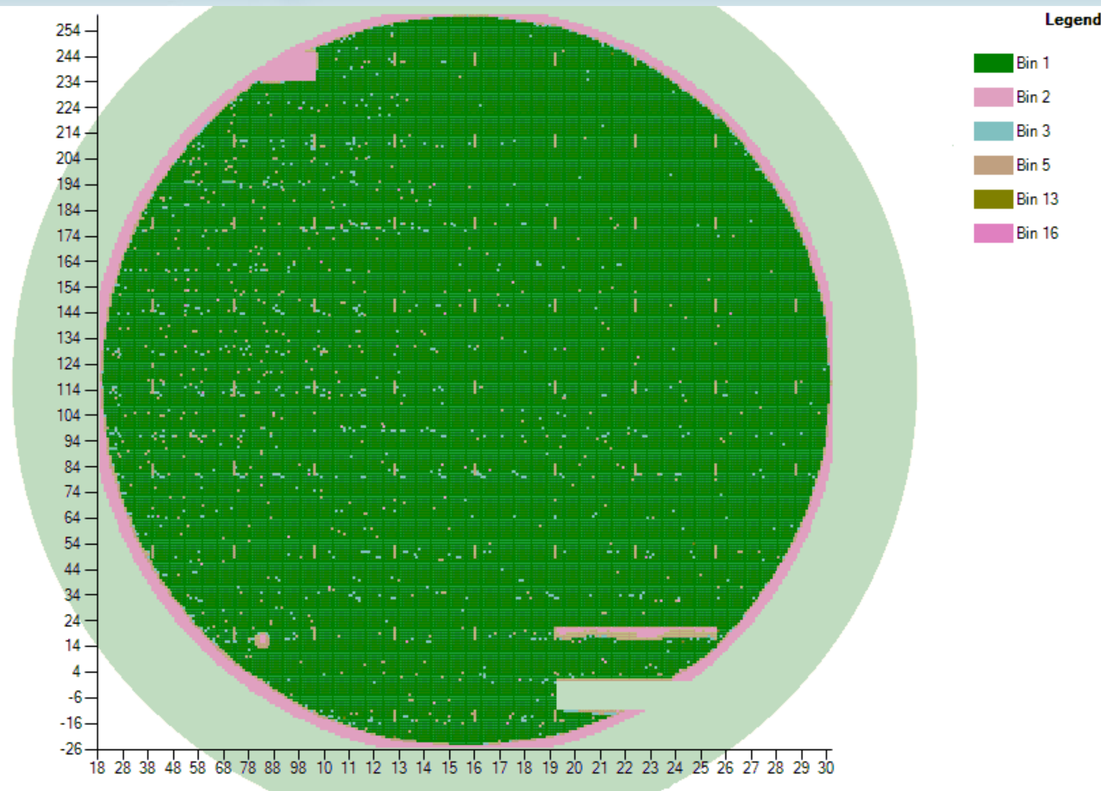

Recent Prototype Wafers – 98 – 99% Yield with test times of 2hrs per wafer – 64 site!

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What's Next?

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128, 256, 512+ Sites?

We know how!

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Andy Pienkowski
(Principal Engineer)

Innovision Research and Technology plc.

Innovision Research & Technology plc
33 Sheep Street
Cirencester
Gloucestershire
GL7 1RQ
United Kingdom

Email: info@innovision-group.com
UK: +44 (0)1285 888 200
US: +1-800 511 9539
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