WLAN System Analysis and System Design Flow

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Abstract

This paper provides an introduction to IEEE 802.11a Wireless LAN specifications and illustrates through the use of AWR's Visual System Simulator (VSS)®, an efficient means to do WLAN system level trade off studies. Orthogonal Frequency Division Multiplexing (OFDM) definition, along with its benefits, is discussed using practical analysis to clearly identify realistic scenarios.

With emphasis on the receiver, the link budget is calculated, providing exact specifications for the constituent parts of the chain. Simulation of Bit Error Rate (BER) to produce an operational system is also covered. Finally, by uniting these ideas, a possible amplifier is proposed along with the necessary error correction techniques. These proposals are demonstrated in a final design, again simulated within VSS®.

Although the presentation revolves around a WLAN application, the system analysis approach and methodology presented here is applicable to any wireless or wired application. AWR's sampled time-domain, complex-envelope system simulator, VSS®, is used throughout the presentation.

Introduction – The WLAN (802.11a) Specification

This paper specifically addresses an 802.11a design. We must first review the physical layer of an 802.11a signal. Note that four different modulation schemes are used to accommodate data rates varying from 6 Mbps to 54 Mbps. BPSK is also used for the pilot signals which are used for detection and carrier recovery.

Data Rate	Modulation	Coding rate R	coded bits per subcarrier N_{BPSC}	coded bits per OFDM symbol N_{CBPS}	data bits per OFDM symbol N_{DBPS}
6 Mbit/s	BPSK	1/2	1	48	24
9 Mbit/s	BPSK	3/4	1	48	36
12 Mbit/s	QPSK	1/2	2	96	48
18 Mbit/s	QPSK	3/4	2	96	72
24 Mbit/s	16QAM	1/2	4	192	96
36 Mbit/s	16QAM	3/4	4	192	144
48 Mbit/s	64QAM	2/3	6	288	192
54 Mbit/s	64QAM	3/4	6	288	216

Table 1: 802.11a Modulation Detail

Table 1 shows various data rates and modulation schemes and the use of several convolutional encoding rates. Block interleaving is also incorporated. OFDM is used to "transport" the information symbols. The coding and interleaving are used to mitigate the impact of multipath. The occupied information bandwidth is 16.6 MHz .

OFDM – Orthogonal Frequency Division Multiplexing

OFDM originated in the late 50's and finally gathered steam in 1966 at Bell Laboratories. It is used today because it accommodates high bit rates. OFDM is also used in DVB-S, for example. The spacing between each carrier is carefully chosen, such that one symbol does not interfere with its neighbour. A guard interval is applied to reduce inter-carrier interference (ICI) due to multipath. If analog technology were to be used to produce analog sinusoids for each symbol, a lot of chip "real estate" would be needed for the individual mixers and LO sources.

To minimize "real estate" requirements, digital signal processing in the form of the Fast Fourier Transform is used. In fact it is the inverse FFT (IFFT) that is used on the transmit end. The time domain signal of the transmitted signal is turned into an IFFT using modern DSP techniques. On the receive end an FFT transform is performed and effectively, the frequency content of the transmitted OFDM symbol is recovered. An example transmit/receive chain taken from IEEE specifications is shown in Figure 2.

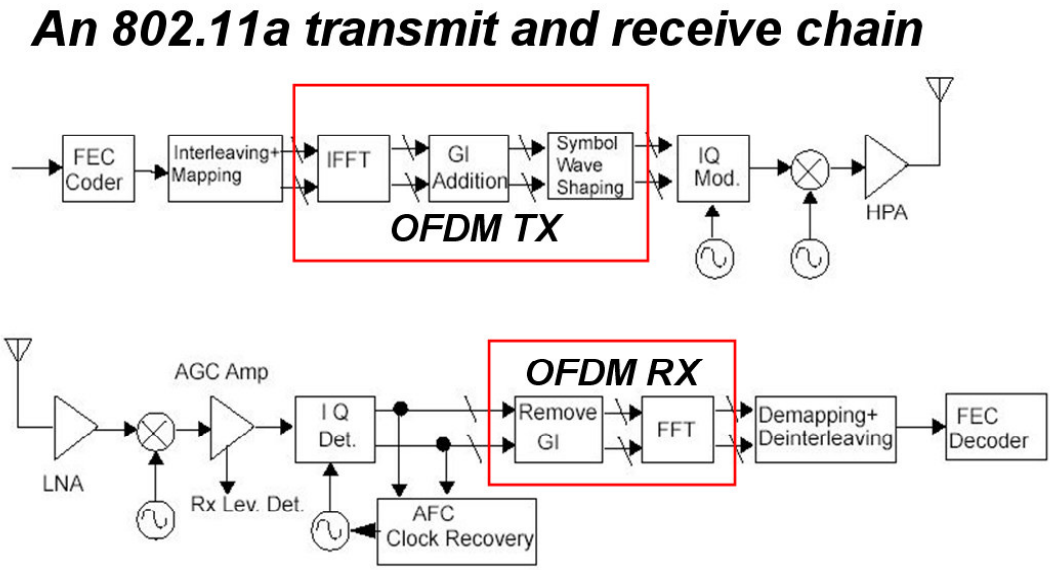


Figure 2: IEEE Example WLAN Transmit/Receive Chain

For practical reasons, a 64-point FFT is used to implement an 802.11a system, although any size FFT could be used as long at the 48 symbols are accounted for. If a larger FFT size were used, more nulls would have to be transmitted. An 802.11a signal in the time domain as well as in the frequency domain (spectrum) would have the characteristics shown in Figure 3. The 8 pilot signals are seen starting at a time equal to zero and each data symbol is preceded by a guard interval of 0.8us.

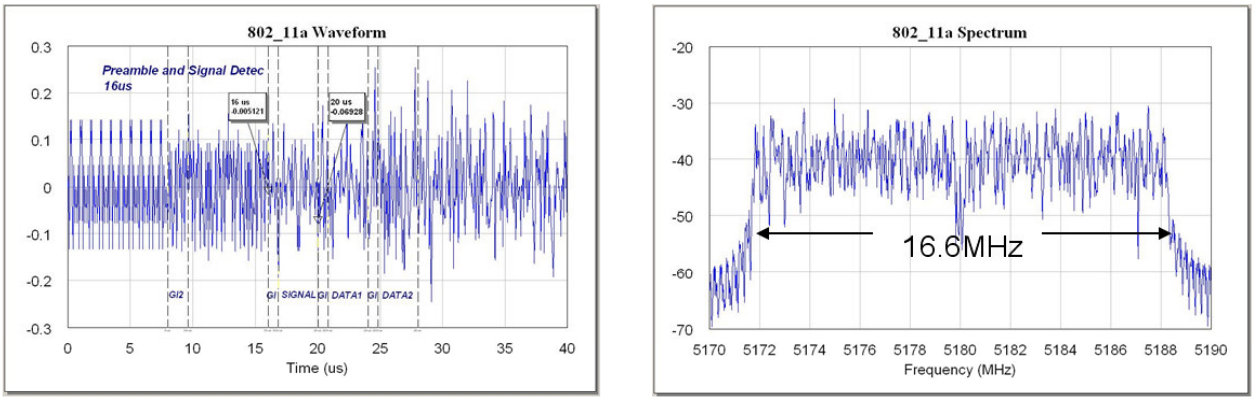


Figure 3: 802.11a Time and Frequency Domain Waveforms from VSS®

An 802.11a signal can use up to 12 channels with channel spacing of 20 MHz. The maximum output power levels for the channels are shown in Table 4. The null placed at DC in the OFDM symbol allows one to use direct conversion without being greatly affected by DC-offset – as could clearly seen in the AWR VSS® simulation software.

Frequency Band (GHz)	Maximum output power up to 6dBi antenna gain (mW)
5.15 – 5.25	40 (2.5mW/MHz) ~ 16dBm
5.25 – 5.35	200 (12.5mW/MHz) ~ 23dBm
5.725 -5.825	800 (50mW/MHz) ~ 29dBm

Table 4: 802.11a Output Power Specification

WLAN– System Design Challenges

There are serious challenges to using OFDM. Relative to 64QAM, the 802.11a 54Mbps has a higher peak-to-average ratio (PAR). As an example, consider what would happen if all 52 sub-carries simultaneously lined up, the PAR would be 17dB, which is much greater than QAM. Considering the AM/AM and AM/PM characteristics of an amplifier compared to the instantaneous power and phase of the signal, it is obvious that the peak power of the OFDM symbol can go into the nonlinear region of the amplifier, even if it has the same average power of the 64QAM signal.

Added to the PAR, one must consider the impact of the frequency offset of a local oscillator (LO). If the LO on the receive end is set to the same value as the LO on the transmit end, the RX signal would not suffer from inter-carrier interference (ICI). That is, the spectral content of a received symbol would not mix with its neighbour. If there is a slight offset between clocks, one symbol will "smear" into its neighbour.

Both of these effects can be investigated using system simulation software. Phase noise can also be simulated in VSS® by spectrally shaping a Gaussian noise source with a data file providing noise at a given offset frequency.

Error Vector Magnitude (EVM) is a measure of the inaccuracy of the IQ symbol, given these effects. The EVM specification or "Relative Constellation Error" for the 802.11a 54Mbps signal is -25dB as shown in Table 5. (On the transmit end the EVM measurement shall not exceed -25dB.) Alongside, the spectral measurement of the transmitted signal with an RBW set to 100KHz and a VBW of 30KHz shall stay within the confines of the specification mask. Although a specific spectral shaping technique is not called upon in the specifications, engineers use this technique to keep the spectrum within the confines of the mask. In addition, backing off the signal power from the 1dB compression point plays a role in keeping the spectrum within the mask.

Data rate (Mbits/s)	Relative constellation error (dB)
6	–5
9	–8
12	–10
18	–13
24	–16
36	–19
48	–22
54	–25

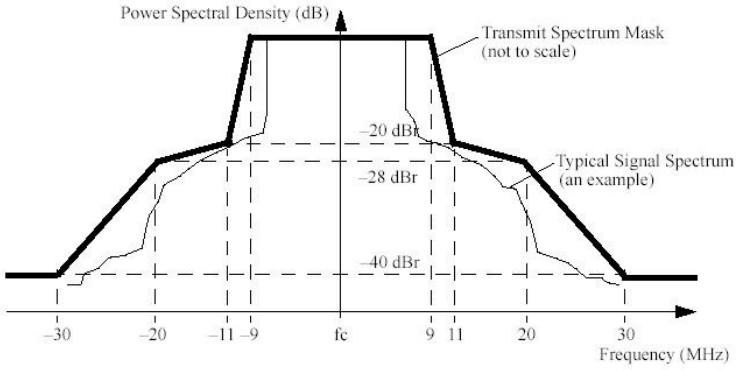


Figure 120—Transmit spectrum mask

Table 5: 802.11a EVM and Spectral Specification

VSS – System Design Simulation for the WLAN Transmitter

The VSS® design suite from AWR allows one an "up front" view of your system. Figure 6 shows the effect of these contributing factors against specification conformance.

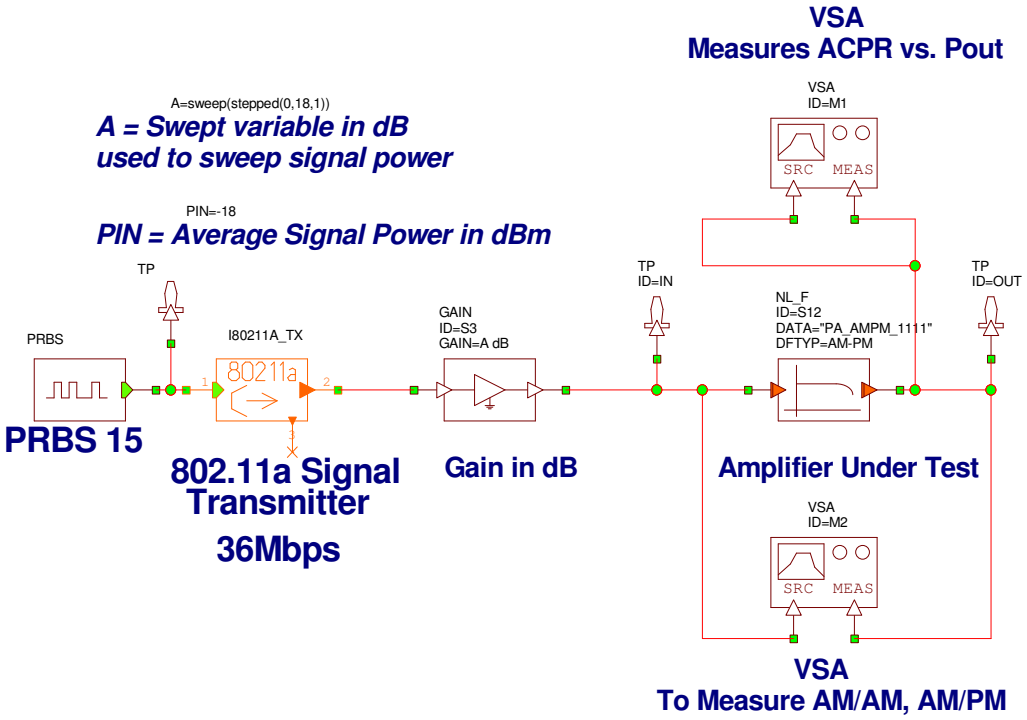


Figure 6: 802.11a Transmit Chain in VSS®

By sweeping the input power and the phase distortion, one can find the limits of design specification in order to meet the requirement design criteria. Table 7 and Figure 8 show how this ultimately affects the design limits of the individual components of the chain.

EVM versus Gain/ Phase error	0 dB	0.3 dB	0.4 dB	0.5 dB
0 Degrees	-33.7 dB	-29.2 dB	-27.3 dB	-25.6 dB
1 Degrees	-32.2 dB	-28.6 dB	-26.9 dB	-25.3 dB
2 Degrees	-29.2 dB	-27.1 dB	-25.7 dB	-24.5 dB
3 Degrees	-26.5 dB	-25.1 dB	-24.3 dB	-23.4 dB

Table 7: VSS® Simulated EVM Results

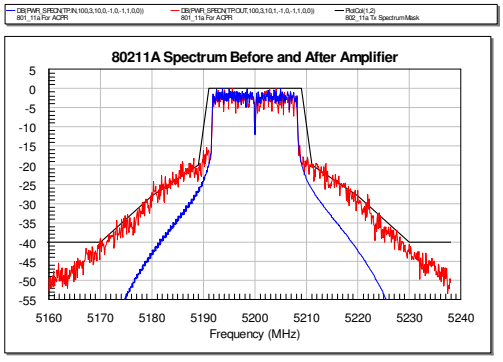


Figure 8: VSS® Simulated Spectrum

This table can then be passed to circuit designers to help them understand the confines of their quadrature mixer design. The idea is to use VSS® to get a qualitative view of the system at a very early stage. VSS® can be used from the beginning of a new design, developing specifications and/or throughout the design cycle to root out a problem from a higher level of abstraction.

WLAN– Receiver Bit Error Rate (BER)

IEEE 802.11a specifications require a packet error rate of less than 10% for all possible data rates. A packet consists of 8000 bits (1000 bytes). The bit error rate comes directly from PER:

PER < 0.1 for 1000 bytes (8000 bits)
Let P_{PC} = Probability that a packet is received correctly
Let P_{BE} = Probability that a bit is received in error
Let P_{PE} = Probability that a packet is received in error

$$P_{PC} = (1 - P_{BE})^{8000}$$
$$P_{PE} = 1 - P_{PC} = 1 - (1 - P_{BE})^{8000}$$
$$(1 - P_{BE})^{8000} = 1 - P_{PE}$$
$$P_{PE} < 0.1, \quad Solve\ for\ P_{BE}$$
$$P_{BE} \le 1.32e-5$$

Thus, we see that the receiver needs to maintain a maximum BER of 1e-5.

Receiver sensitivity: $S = NF + N_o + S/N$ is dependent on modulation technique, coding, bandwidth of signal and the noise figure of the receiver. It is the required minimum signal power to achieve a particular BER.

Data rate (Mbits/s)	Minimum sensitivity (dBm)	Adjacent channel rejection (dB)	Alternate adjacent channel rejection (dB)
6	–82	16	32
9	–81	15	31
12	–79	13	29
18	–77	11	27
24	–74	8	24
36	–70	4	20
48	–66	0	16
54	–65	–1	15

Table 9: IEEE 802.11a Table for Receiver Sensitivity

According to specifications in Table 9, a receiver detecting a 54Mbps signal should be able to achieve a BER of 1e-5 with an input power of -65dBm. Thus, using the equation for S above one can see that there is an 18.5dB margin for NF.

$$S = NF + N_o + S/N$$

$N_o = 10\log_{10}(\text{kTB/1e-3})$ in dBm. (Note : for B = 1Hz, $N_o = -174$ dBm)

For 802.11a set B = 16.6 MHz, then $N_o \cong -101.8$ dBm.

A $S/N = 18.3$ dB for 54 Mb/s ensures a (coded) BER of 1e-5

S = -101.8 + 18.3 = -83.5 dBm This is 18.5 dB above specification

How was the 18.3dB value for S/N obtained?

$$S/N = \frac{P_S}{P_N} = \frac{P_S}{B \cdot N_0}, \text{ for } B = 16.6 \text{ MHz}$$

$$\frac{E_b}{N_0} = \frac{P_S \cdot T_{SYM}/(\#bits)}{N_0} = \frac{P_S}{N_0} \cdot \frac{T_{SYM} = 4\mu\text{sec}}{6 \cdot 48}$$

$$S/N = E_b/N_0 + 6.3 \text{ dB}$$

bits per subcarrier in 64-QAM data subcarriers per 4usec OFDM symbol

Also, one can find (for example, Van Nee & Prasad, p. 65) that for 64-QAM with the rate-3/4 code in the standard, the required **Eb/N0 = 12 dB @ BER = 1e-5**. So, the required SNR for 802.11a-54Mb/s becomes:

S/N = 12 + 6.3 = 18.3 dB.

If one reads papers on WLAN design, it is very difficult to find such equations. In general, the papers reference a BER of 1e-5 and a value for S/N without giving details. We clearly state that a signal-to-noise ratio of 18.3dB is needed for a 64QAM signal with ¾ rate convolutional encoding, soft decision on the receive end and a defined trace back length. A different modulation and coding rate would yield a different S/N. In theory, one can design a receiver that can detect an -83.5dBm signal and achieve a BER of 1e-5 as long as the NF is zero. Reality dictates, however, that the NF would not be zero, so we have an 18.5 dB margin to work with.

VSS – System Design Simulation for the WLAN Receiver

For simulation purposes in Figure 10., we have folded the complete RF link into one amplifier. This amplifier is representative of the receiver's Gain, IIP3 and NF. Later, we place the complete RF link into a system analysis and use VSS® to ascertain at a very high level of abstraction the receiver sensitivity value for a BER of 1e-5.

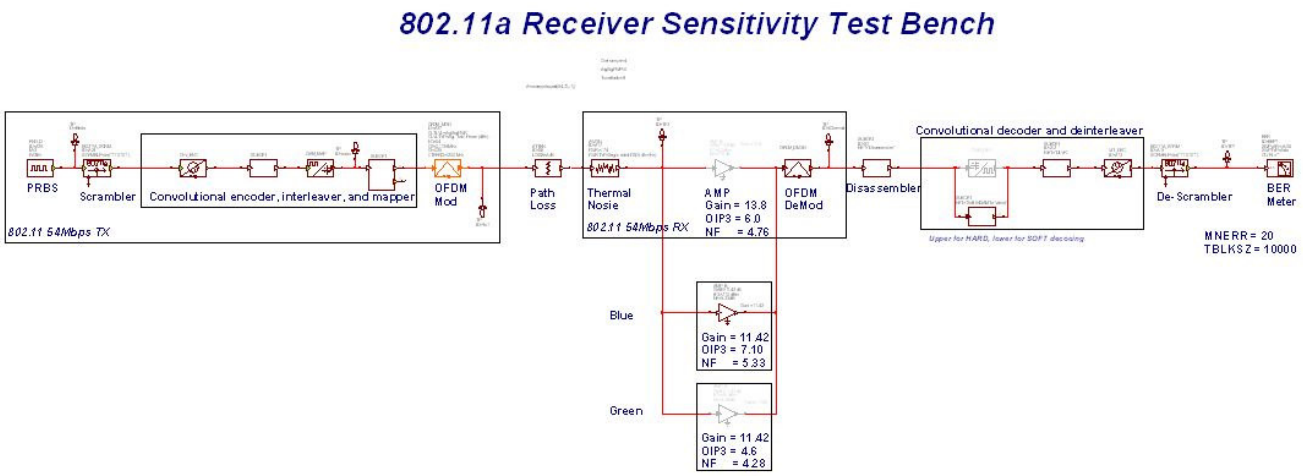


Figure 10: 802.11a Receive Chain in VSS®

This VSS® project includes the scrambling, convolutional encoding and interleaving and shows the individual blocks needed to construct an 802.11a 54Mbps signal along with the receive chain. VSS® is sweeping the signal power seen just before the receiver and as we sweep the signal power, VSS® plots BER. Each amplifier in this design represents values obtained from the RF-link cascaded measurements for minimum, average and maximum extremes of parameters. A BER simulation for each amplifier is shown in Table 11.

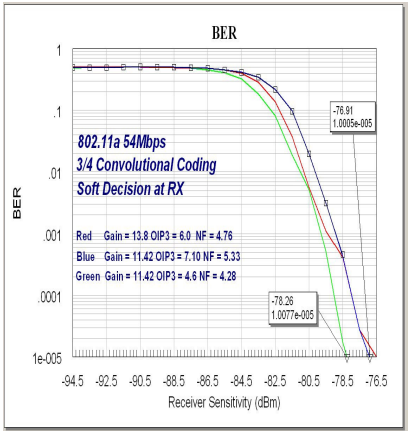


Table 11: Simulated BER versus RF Link Parameters in VSS®

As the simulation is running, we generate a BER curve using the highest NF and lowest gain value obtained from the cascaded analysis. The configuration ultimately defines the receiver's worst case sensitivity. The simulation is a raw or Monte Carlo simulation. Bits in are being compared with bits out and a BER calculation is performed. A Monte Carlo simulation is used because there is a nonlinear element in the diagram as well as a soft decision. One cannot use a quasi-analytical or importance sampling to do such BER simulations and this is true for all system simulation tools. These BER simulation methods are acceptable if one is using just encoding, but even then the methods have many constraints and are not easily set up. Nevertheless, a simulation on a 1.5GHz PC takes less than 10 minutes to get to a BER of 1e-5.

Using the amplifier with the lowest NF and OIP3 would have given a result 1dB off. The specification states that one should be able to detect a signal of -65dBm and get a BER of 1e-5. In this case we determined that the receiver sensitivity is -76.91dBm, which now leaves a 12dB margin. Thus, this eats into the original 18.5dB margin. From a system analysis perspective there is a 12dB margin to work with. This can be easily consumed depending on receiver performance. In the simulation we use an ideal receiver and the synchronization is handled automatically by VSS® (unlike other system tools where manual compensation is needed). Using engineering, one can design a receiver that has a phase recovery loop and pilot detection. From a systems perspective, however, it is imperative that designers understand up front what is achievable. After all, if something cannot be simulated (i.e. mathematically proven), there is no chance that it can be built in hardware. Initial design work saves time in the long run and it is important to consider this point. A simulation tool is used to show what does not work very early on and therefore reduce cycle times. Telling the receiver designers that they have a 12dB margin to work with aids in the design of the receiver and the selection of ADCs, for example.

As shown in Figure 12, even interference simulation can be undertaken in VSS®. We have created an 802.11a interfering signal at 5240MHz along with a 5220MHz CW interferer tone. When the combination of the interfering tone with the adjacent channel is down converted, the resulting third-order intermodulation product folds into the bandwidth of the desired signal at 5200MHz. In VSS®, the receiver will consider the primary signal as the one to detect because the second combiner has its primary input designated as node 1. This enables the receiver to detect the propagated parameters of the primary signal for auto gain, phase and delay compensation. The receiver considers the other signals as interference and the mixer produces the resulting third-order intermodulation product. As the signal power is lowered, the BER results improve. The pulse shaping used by the interfering channel also plays a role in the BER simulation. If the skirt of the interfering channel were not as steep, it would "roll" into the desired channel and affect BER simulations. The secondary OVERLAP parameter of the 802.11aTX block governs the pulse shaping of the signal.

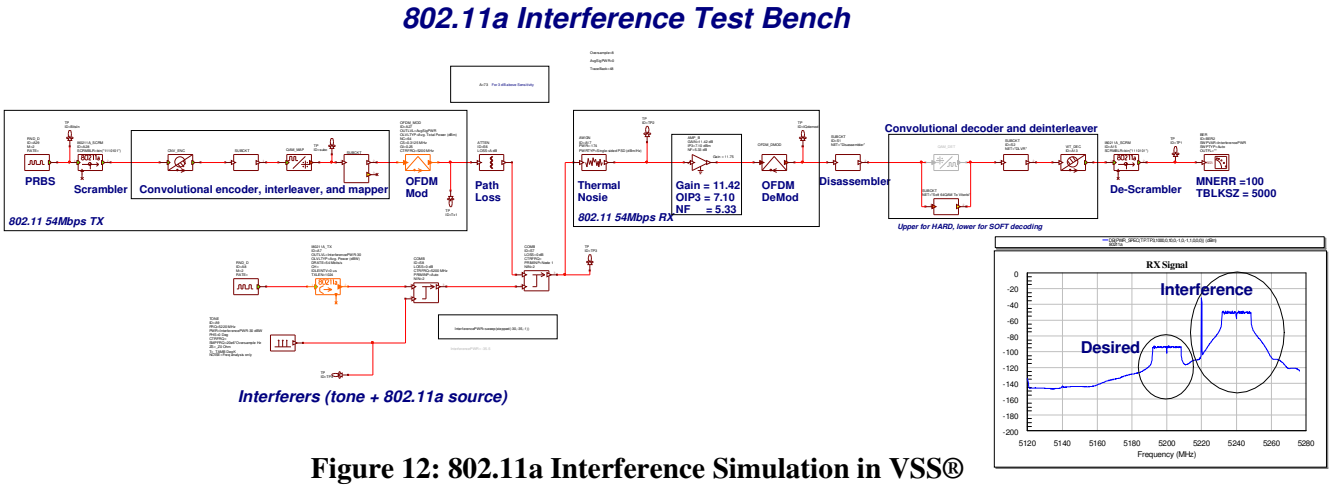


Figure 12: 802.11a Interference Simulation in VSS®

VSS – Impact of the Power Amplifier and Digital Predistortion

Why is there interest in linearizing the Power Amplifier (PA)? The motivation is to increase its power added efficiency of this amplifier. Typically, one want's to keep the signal's instantaneous power as close as possible to the 1dB compression point to increase PAE. Today's signals are more complex and have high peak-to-average ratios. As the signal's instantaneous power approaches the nonlinear region of an amplifier it becomes distorted. A spectrum plot reveals the result of operating in the nonlinear region, with third-order intermodulation products that cause spectral regrowth and higher ACPR values as in Figure 13.

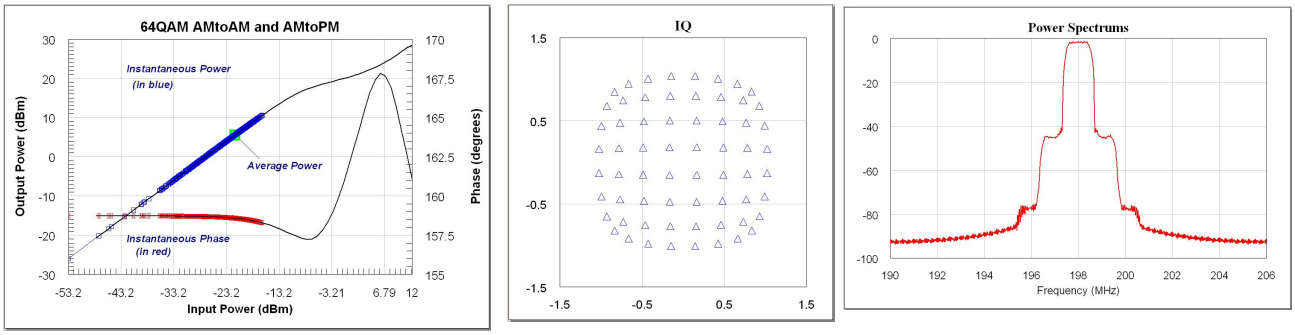


Figure 13: Distorting PA Simulation in VSS®

To avoid PA distortion (keep the operation of PA in the linear region), one could simply back off from the 1dB compression point and accept this as the solution. Since we are working with a quadrature signal, specifically QAM, mathematically one needs to make sure that the derivative of the gain and phase response of the PA are approximately zero. Simply backing off from the 1dB compression point might not be the best thing to do to avoid distortion. The further from the 1dB compression point, the less efficient the PA.

A better option is digital predistortion. The idea is to choose a function F such that H(F) is linear for all input values. Graphically, we want to create the inverse AM/AM curve and combine it with the original curve such that the overall effect after the amplifier is a linear response. The baseband signal (IQ signal) is pre distorted so as to generate the inverse AM/AM AM/PM curves. The predistorter applies zero gain to the signal in the linear region; in the nonlinear region it either amplifies or attenuates the signal. Note that the overall gain of the predistorter in series with the PA must be the same as the PA alone. VSS® includes all of the necessary components to build such mathematical digital predistortion.

Clearly, in the linear region of operation the predistorter applies little to no gain to the incoming signal. In the nonlinear region, however, the predistorter activates. After establishing the inverse characteristics one needs to derive the coefficients that will be used to pre distort the incoming IQ signal. One could use a lookup table of power points. Here, the lookup tables (I & Q) each consist of 26 coefficients used to apply the necessary gain and phase shift to the incoming IQ signal. We use the signal's instantaneous power to index the lookup table. One must first construct a circuit to calculate the signal's power. There are two LUTs, one for the inphase coefficients and the other for the quadrature phase coefficients. The instantaneous power is calculated and the appropriate coefficients are selected. The LUTs internally handle interpolation. Simultaneously, the IQ signal is being complex multiplied with the coefficients as shown in Figure 14.

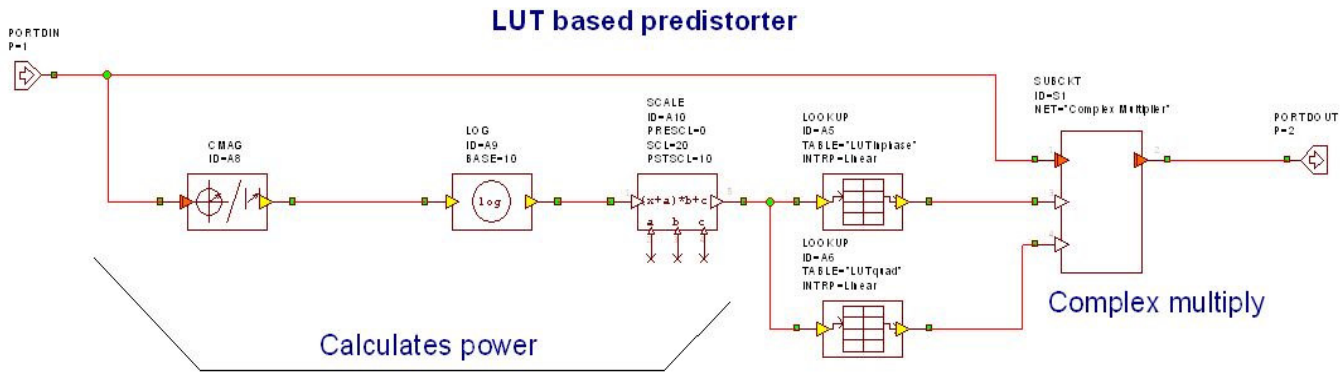
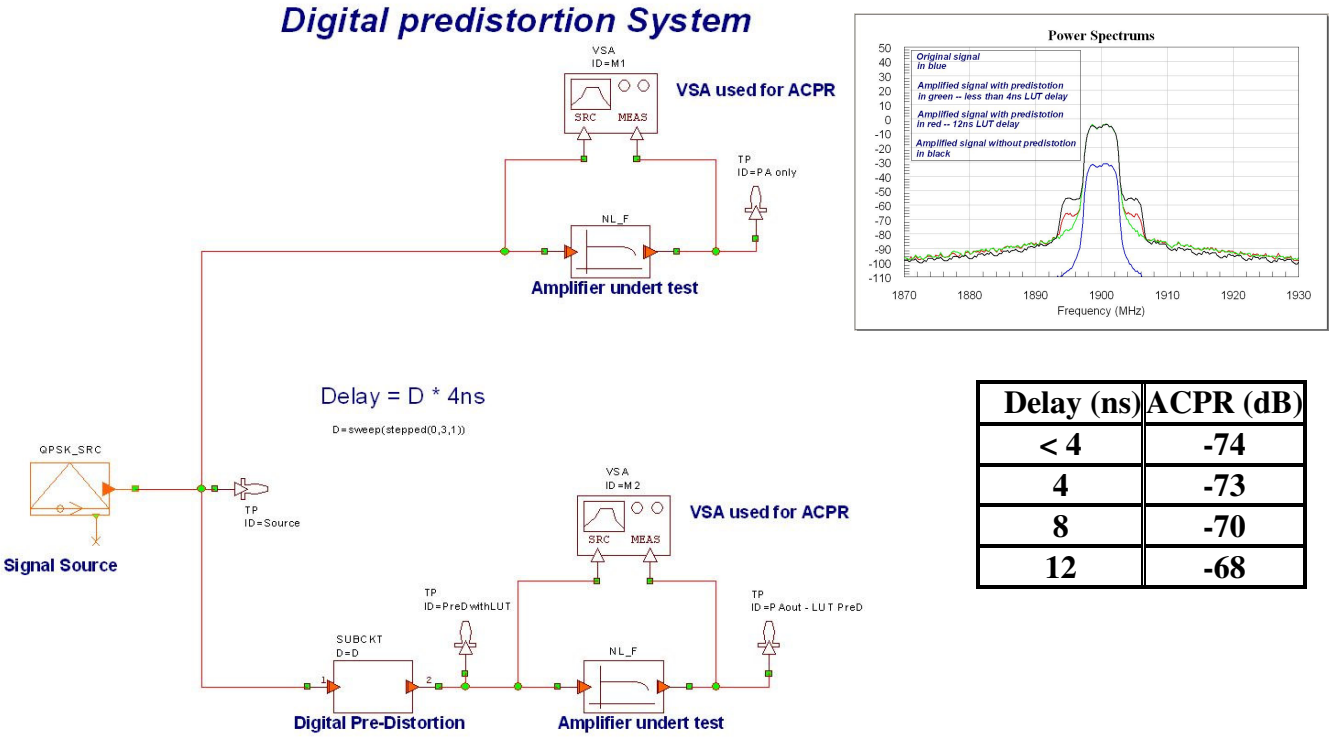


Figure 14: LUT Simulation in VSS®

The effect of LUT access time can be simulated in system software such as VSS®. The top link in Figure 15. is the amplifier alone. The second link is the digital predistorter with a variable D (for delay). The variable D is swept from 0 to 3. Each step is equivalent to 4ns. Thus, when D=0 the access time is 0ns and when D=3 the access time is 12ns. The blue spectrum is the signal before amplification. The green spectrum is being updated during the sweep of D (or the LUT access time). The red spectrum has a fixed access time of 12ns. The black spectrum is without digital predistortion.



Delay (ns)	ACPR (dB)
< 4	-74
4	-73
8	-70
12	-68

Figure 15: Digital Predistortion Delay Simulation in VSS®

The digital predistorter can be placed in the TX chain, before the transmitter PA. Ultimately, the predistorter helped with the overall receiver sensitivity number. We did not have to "back off" the signal in order to meet specification and can conclude that we have suitably linearized the PA.

AWR Design Environment – Implementing a Final Solution

Finally, to use all of these ideas in a complete WLAN card design, we start with the ideal circuit design. Using advanced library model components and the unique AWR XML libraries for electrical model, schematic symbol and physical footprint, the board design is quickly developed into a practical design, accounting for all RF affects. Consideration is given to the physical layout as the project is built providing a true simulation model for the card in Figures 16 and 17.

External EM tools such as Sonnet can be used to design the antenna. This block simply becomes another model available within the AWR Design Environment. The AWR 3D planar EM tool is also used to reduce the PA output harmonics with resonator rings buried in the PCB stack.

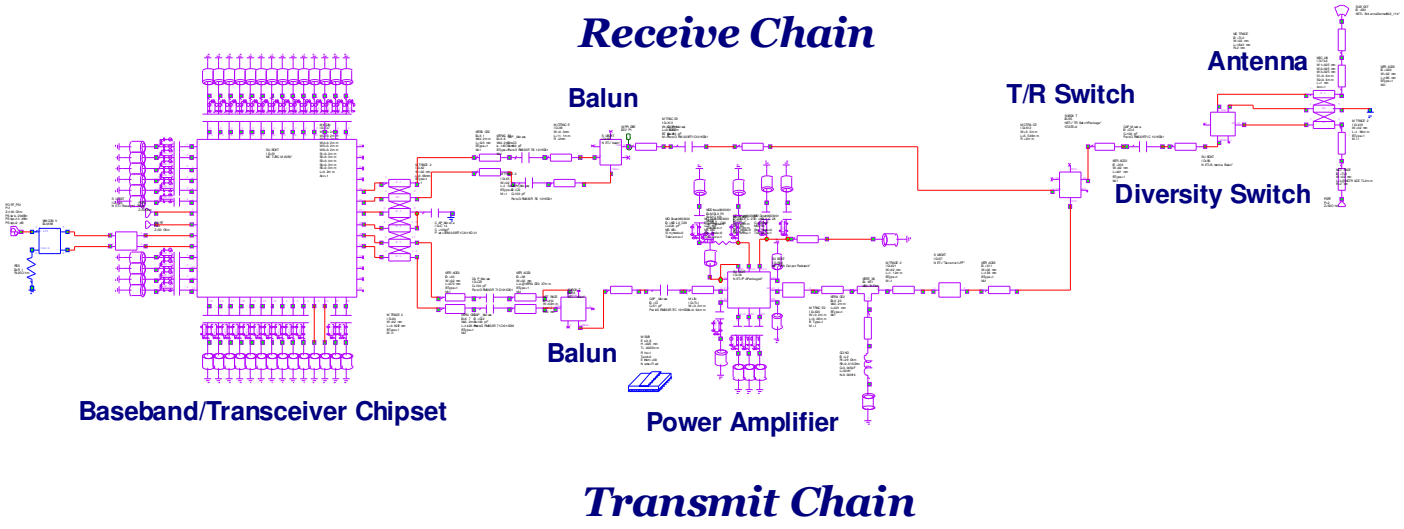


Figure 16: Final WLAN Card Design

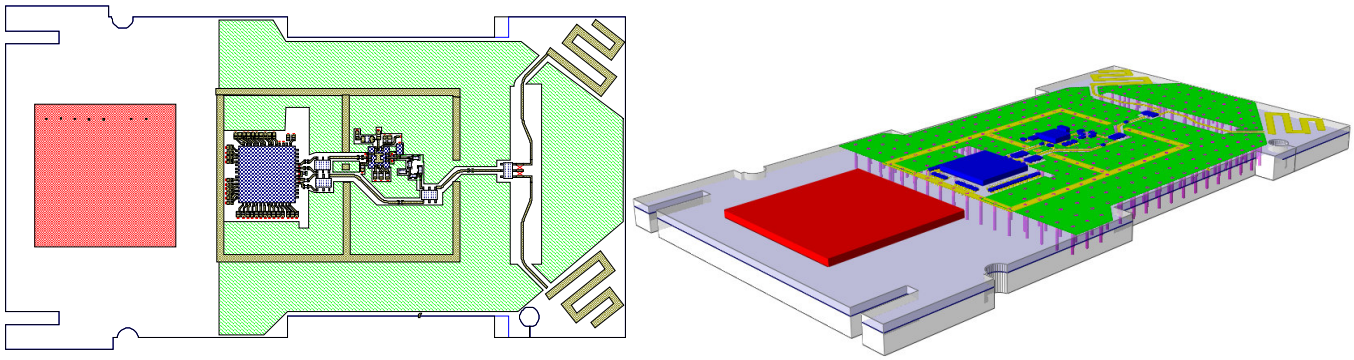


Figure 17: Final WLAN Card Design Layout

AWR Design Environment – Using Microwave Office (MWO) and VSS® Together

The biggest advantage of having circuit level simulation tools (with the layout integral with the tool) combined with a top-level system simulation tool such as VSS®, is the ability to use the final design within an extracted systems world. Passing a complex 802.11a signal though the complete MWO circuit level design is simply a case of using subcircuit hierarchy within the same design environment.

Ultimately, this confirms "proof of concept" for the designer before time and money are spent on prototyping, manufacturing, or purchasing any of the constituent parts. This provides a high level of confidence that the final system will conform to the required specification, as per Figure 18.

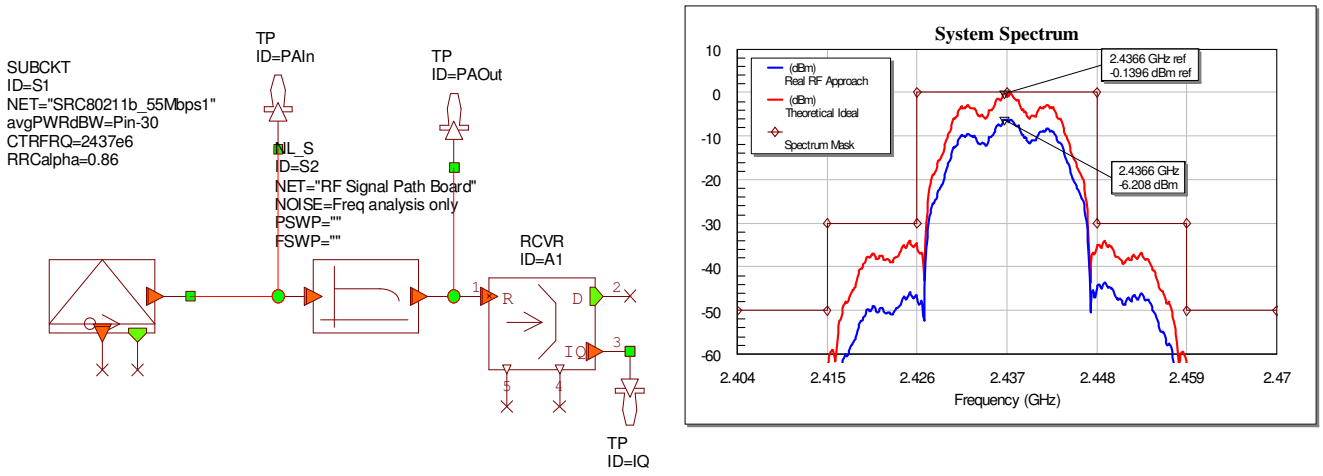


Figure 18: Final WLAN Card Design Conformance Testing

Conclusion

This paper discussed the theory of WLAN 802.11a and how such a system may be implemented. Using the AWR Design Environment, many of the specifications have been worked out and explored. Some of the technical challenges facing design teams have been described and the importance of using the correct design environment has been demonstrated.

Integrating both a circuit and system level simulation tool into the same environment has allowed a design to been proven before the cost implications of time and money are taken into account. A suitable approach to analyzing the RF-aware board has been used to optimize the design and to provide high confidence on the measurements expected once the prototypes are manufactured.

Footnotes:

- **[1]** Masoud Zargari, et. al, "**A 5-GHz CMOS Transceiver for IEEE 802.11a Wireless LAN Systems**" *IEEE Journal of Solid-State Circuits*, Vol 37, No. 12, December 2002.
- **[2]** S. Kusunoki, et. al, "**Power Amplifier Module with Digital Adaptive Pre-distortion for Cellular Phone**" *IEEE MTT-S Digest 2002*, page 765.

References

- "**Wideband Orthogonal Frequency Division Multiplexing (W-OFDM)**" WiLAN Wireless Data Communications, © 2000.
- Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications High-speed Physical Layer in the 5 GHz Band. IEEE Std 802.11a-1999
- Svetoslav Gueorguiev, Saska Lindfors, "**Design considerations for IEEE 802.11a WLAN transmitter in CMOS Technology**" *RISC group, Institute of Electronic Systems*, Aalborg University, Denmark.
- Jung Yee and Hossain Pezeshki-Esfahani, "**Understanding Wireless LAN Performance Trade-Offs**" *Communications System Design* November 2002.
- "**Improving Receiver Sensitivity with External LNA**" Maxim Application Note, December 27, 2002.
- "**OFDM For Wireless Multimedia Communications**" Richard Van Nee and Ramjee Prasad, Artech House Publishers.
- Maria Hofvendahl, "**2.4GHz Power Amplifier with Cartesian Feedback for WLAN**" *LiTH-ISY-EX-3524-2002*, Datum 2002-09-03.
- Ali Behravan, et. Al, "**Adaptive Predistorter Design for Nonlinear High Power Amplifiers**"
- Frederick B. Popovich, et. al, "**RF and Microwave Power Amplifier and Transmitter Technologies – Part 4**" *High Frequency Electronics*, November 2003.
- Allen Katz, "**Linearizing High Power Amplifiers**" *Linearizer Technologies, Inc*.
- Ali Behravan, et. al., "**Adaptive Predistorter Design for Nonlinear High Power Amplifiers**".
- Frederick B. Popovich, et. al., "**RF and Microwave Power Amplifier and Transmitter Technologies – Part 4**", High Frequency Electronics, November 2003.
- Allen Katz, Linearizer Technologies, Inc. , "**Linearizing High Power Amplifiers**"