Low Loss, Low Cost, Discrete PIN diode based, Microwave SPDT and SP4T Switches

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Abstract

This paper describes the design, implementation and measured performance of low loss microwave Single Pole Double Throw (SPDT) and Single Pole 4-Throw (SP4T) switches. The switch designs use beam-lead packaged PIN diodes, SMT resistors and capacitors and printed components on a low cost Rogers' RO4003 substrate. The operating frequency range is 12GHz to 19GHz and the measured insertion loss is 0.85dB for the SPDT and 1.8dB for the SP4T. The switch can handle RF input power levels of at least 2W without any significant compression.

Introduction

A low cost, compact Ku-band (12.4 to 18GHz) SP4T switch was required to replace an expensive, bulky connectorised part that was used in the prototype implementation of a radar system. Whilst Monolithic Microwave Integrated Circuit (MMIC) SPDT switches were commercially available as both packaged components and bare die, the insertion loss was relatively high (typically > 1.5dB at 16GHz) and the power handling capability relatively modest (P-1dB < 26dBm). Additionally such switches were only readily available in an SPDT topology, meaning that three parts would be required to realise an SP4T making the unit cost significant. Whilst a custom MMIC solution could be developed to provide a low loss, compact microwave SP4T [1] the NRE costs would be high. The solution therefore adopted was a design based around discrete packaged PIN diodes, SMT resistors and capacitors and printed components realised on a low cost Rogers' RO4003 substrate of 0.008" thickness.

Circuit Design

At RF and microwave frequencies PIN diodes behave as voltage variable resistors and can therefore be used to realise switches. The diode structure comprises a region of high resistivity Intrinsic material sandwiched between a region of P-type semiconductor and N-type semiconductor. When the PIN diode is forward biased, charge carriers are injected into the I region lowering its resistance. When the diode is zero-biased or reverse biased the I region is high resistance, in the region of several kΩ.

At low RF frequencies simple switch configurations, such as the SPDT shown in Figure 1, can be readily realised. In this case a series mounted diode is used in each arm of the switch. When one of the diodes is forward biased, and so conducting a DC current, that arm of the switch is "on". When the diode is reverse biased the switch arm is off. More complex switches, that also incorporate shunt diodes, can be realised for improved isolation or to extend the upper operating frequency of the switch [2].

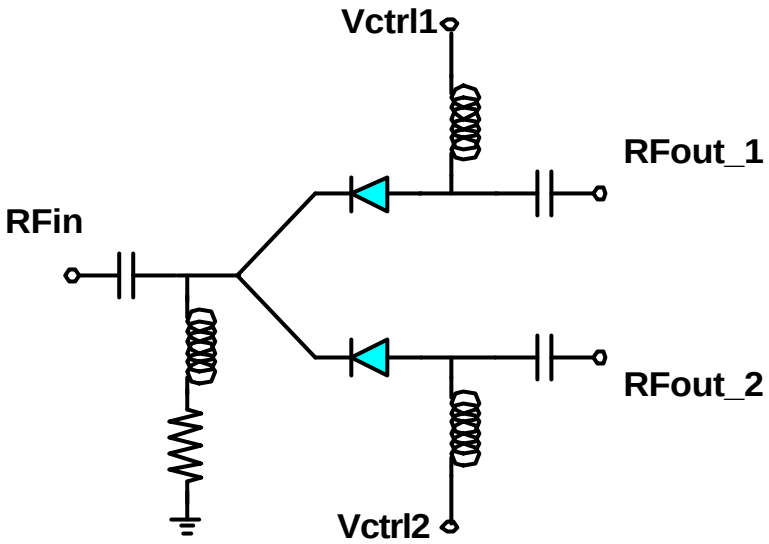

Figure 1: Typical simple PIN diode SPDT

As operating frequencies increase, two problems occur with the simple PIN diode switch topologies described above:

- The packaging parasitics start to affect the performance
- The off-state capacitance of the diodes becomes significant

The primary effects of the diode packaging are to add series inductance and some parallel capacitance. This is depicted in the equivalent electrical model of Figure 2, where Lp and Cp are the packaging parasitics and the intrinsic diode is shown within the dotted line. For low cost plastic packaged PIN diodes Lp is normally between 1nH and 2nH. At 16GHz this equates to a reactance of between 100 and 200Ω, which will clearly have a serious effect on circuit performance.

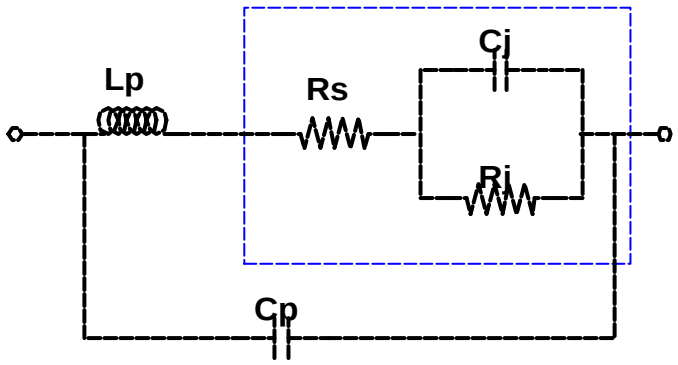

Figure 2: Equivalent model of a packaged PIN diode

Following a review of the commercially available parts, a beamlead packaged PIN diode from Metelics was selected. The beamlead package has a very small outline, shown in Figure 3, and therefore has very low package parasitics. Lp is just 0.1nH and Cp just 0.015pF.

The selected diode was designed for use at microwave frequencies and the off-state junction capacitance is therefore very low at just 0.03pF. Combined with the package capacitance this gives a total capacitance of 0.045pF. Whilst this is as low as could be expected for a packaged PIN diode it will provide limited isolation as a series element in Ku-band. In a 50Ω system a

series capacitance of 0.045pF has a loss (isolation) of less than 7dB at 18GHz. In addition to this the resistive losses of the series diode add to the insertion loss of the switch.

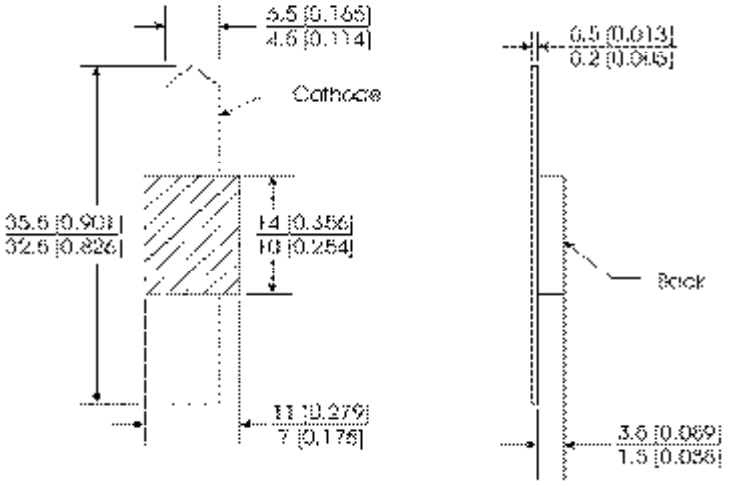

Figure 3: Metelics' PIN diode package outline dimension in mils (mm)

In light of the limited isolation offered by a series off-state diode, and given that the switch does not need to operate down to low frequencies when a series element would be necessary, it was decided to adopt a switch topology containing only shunt diodes. This topology results in a bandpass response but allows lower insertion loss as it avoids the resistive losses of series diode elements.

The design approach adopted is to absorb the off-state capacitance of the PIN diode into a Low Pass Filter (LPF) structure. The starting point is to design a conventional LPF [3] with an upper operating frequency slightly above the required operating frequency of the switch. All of the shunt capacitors are then replaced with off-state diode models, which are primarily capacitive, and the filter's performance is re-optimised. It is important to also include accurate models for the through substrate vias used to ground the diodes. Two vias in parallel were used to ground each diode in order to reduce the grounding inductance. The next step is to replace the series inductors with short lengths of microstrip transmission line. Again the filters performance is re-optimised to give acceptable insertion loss and match across the required operating band. This process is depicted in Figure 4.

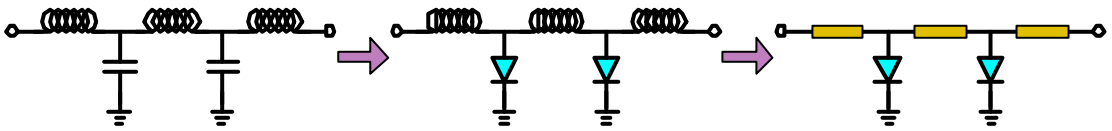

Figure 4: The design path

The first element of the LPF must be inductive as when the diodes are in their on-state (low resistance) the filter must present a high impedance at its input. This is so that two filters can be connected at the input to form the two arms of an SPDT. When the diodes are in the on-state the switch arm is "off" and provides isolation. The order of the LPF, and so the number of shunt capacitors (diodes), is a compromise between high isolation and low losses and current consumption. In the design presented here, two shunt diodes were selected.

The next step is to add the required biasing components to control the diodes. Shunt short-circuit stubs connected in parallel with the second shunt diode were used as bias chokes. The RF short-circuit for the shunt stub was realised using a radial stub. This provides a low reactance path to ground across the operating band. SMT resistors were included in the bias

feed line to limit the on-state bias current from the switch control voltage (10mA per on-state diode from +5V). SMT shunt capacitors were also used to provide RF grounds along the control line. The approach taken was to design the bias feed to present an open-circuit at the point it connects to the LPF rather than requiring the filter to be re-optimised to compensate for the bias feed.

Series SMT capacitors were added at the input of each switch arm. Output DC blocks could have also been added in a similar fashion but were not required in this custom application. SMT capacitors can be modelled as a series capacitor and inductor. The package inductance (Lp) increases with component size, and 0201 size capacitors were therefore chosen for this application in order to benefit from the low parasitic inductance of just 0.2nH. Whilst the parasitic inductance is low, it still represents 23Ω reactance at 18GHz, which could degrade the input match of the switch. However, it is possible to compensate for this series inductance by including short length open-circuit shunt stubs at the input and output of the capacitor as depicted in Figure 5.

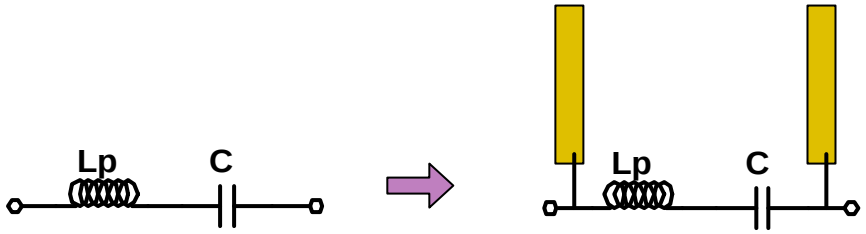

Figure 5: Compensating for SMT capacitor parasitics

The open-circuit stubs act as low value shunt capacitors. The length is selected so that the capacitance forms a low pass filter structure with the series inductance Lp. The cut-off frequency of this filter must obviously be above the required operating band for optimum performance. For this design it was found that adequate shunt capacitance could be obtained by slightly increasing the width of the mounting pads for the capacitor. The simulated return loss of the 2.2pF 0201 capacitor used to provide the DC block is shown in Figure 6, with and without compensation. The red trace (s11) is the uncompensated capacitor model, which has a return loss of 14dB at 18GHz. The return loss of the compensated capacitor is plotted as s22 (the blue trace) and shows a return loss of 23dB at 18GHz.

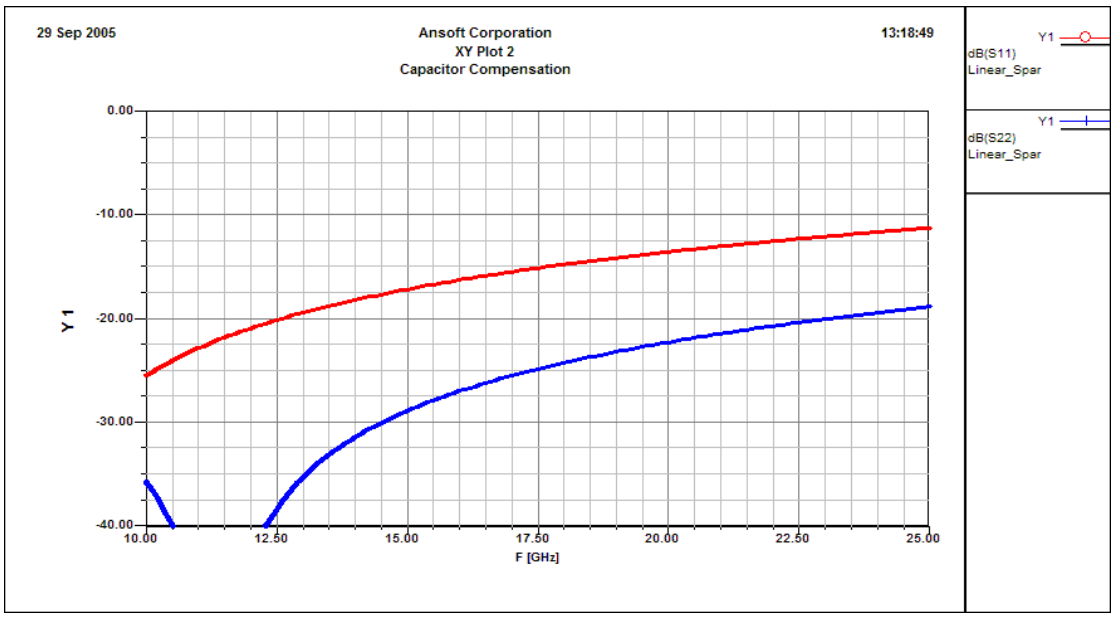

Figure 6: Return loss for a 2.2pF 0201 capacitor, with and without compensation

The compensated series capacitor was incorporated into the filter structure and the structure re-optimised for high on-state return loss (when the diodes are in their off-state) and high input impedance in the "off" state (when the diodes are in their on-state). The SPDT is then formed by connecting together two filters at the input. A schematic of the overall topology of the SPDT is shown in Figure 7. Careful modelling of all junction discontinuities and SMT component pads was undertaken throughout the design process and is necessary to ensure optimum performance.

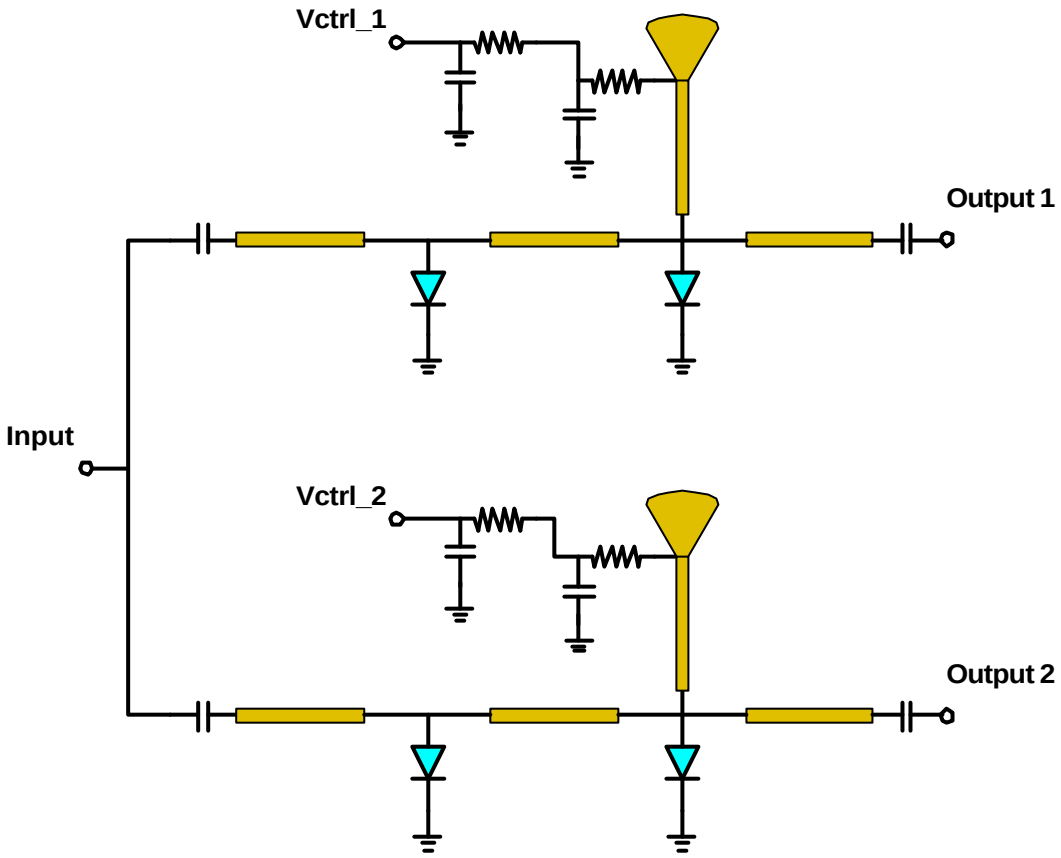

Figure 7: Final circuit topology for the SPDT

It was decided that for simplicity the SP4T would be realised with three SPDTs (an input SPDT feeding two output circuits). This allowed a simple single sided substrate to be used and gave adequately low insertion loss for the application under consideration.

Realisation

The substrate material used was 0.008" thick Rogers' RO4003 with 0.5oz copper cladding. An electroplated gold finish with a nickel barrier was used to allow attachment of both the SMT components and the beamlead packaged diodes. The current limiting resistors used in the bias feed were 0402 components. Although these have higher parasitics than 0201 resistors, they have higher power handling capability. A photograph of one of the SPDTs is shown in Figure 8, and one of the SP4Ts in Figure 9.

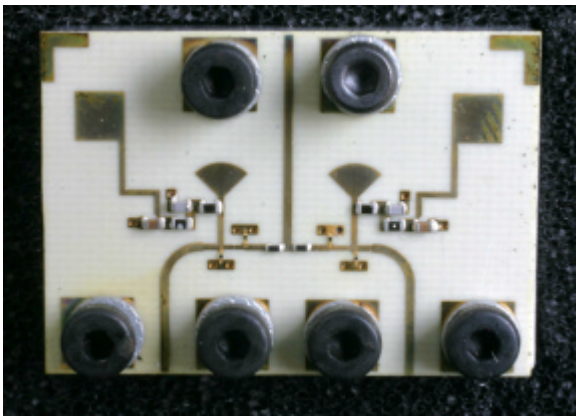

Figure 8: Photograph of one of the SPDT tiles

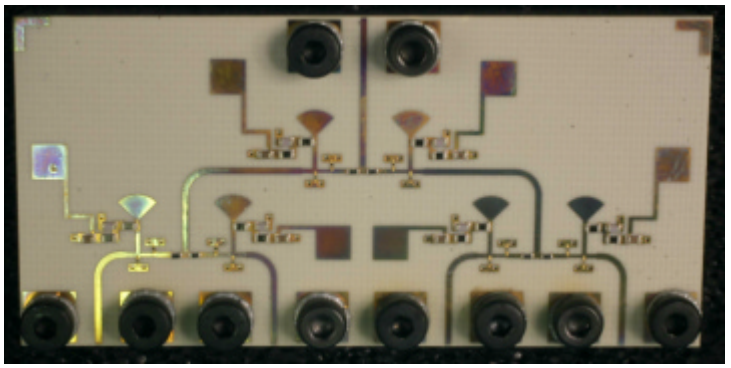

Figure 9: Photograph of one of the SP4T tiles

A connectorised variant of the SP4T including integrated drivers, allowing two line control with a standard 3.3V logic interface, was subsequently realised. A photograph is shown in Figure 10.

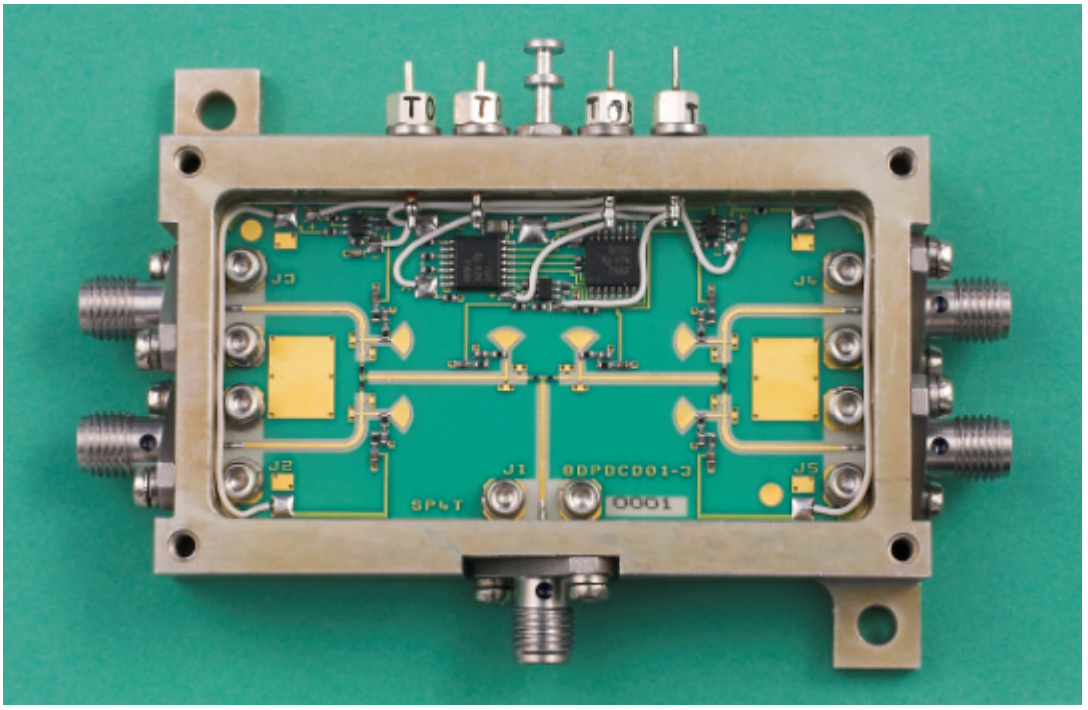

Figure 10: Connectorised SP4T including integrated drivers

Measured Performance

The switch PCBs were assembled into simple test jigs for measurement. Figure 11 shows a photograph of the SPDT in its test jig. A similar jig was also used for the SP4T. The total losses of the two connectors and the feed lines to the switch were around 0.6dB.

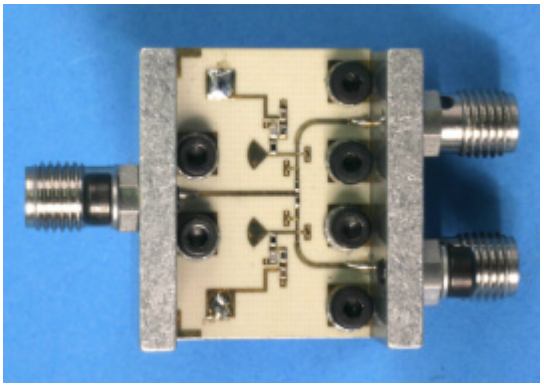

Figure 11: Photograph of SPDT in test jig

Figure 12 is a plot of the measured performance of the on-case SPDT, including test jig losses. The switch has good performance from 12 to 19GHz and at mid-band (15.5GHz) the loss is 1.45dB. Removing the 0.6dB test jig losses, leaves a switch loss of just 0.85dB.

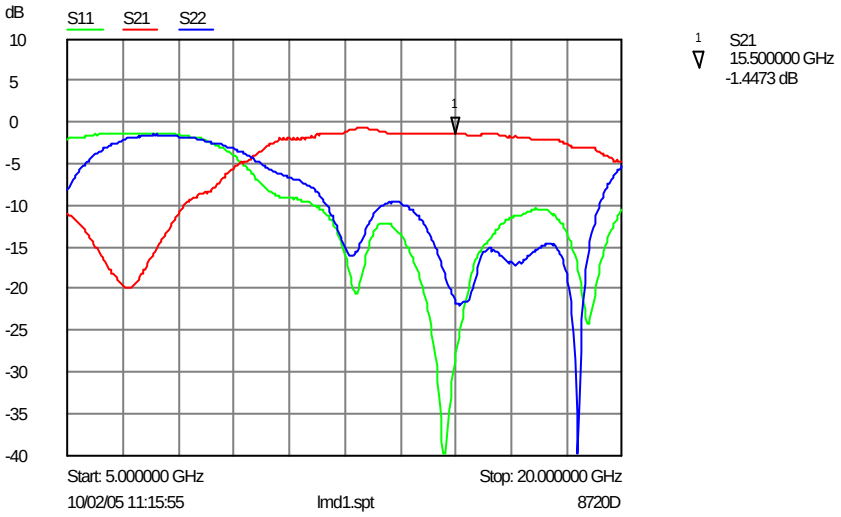

Figure 12: Measured performance of on-case SPDT, including test jig losses

The measured isolation of the SPDT is shown in Figure 13 and is 17dB at 15.5GHz.

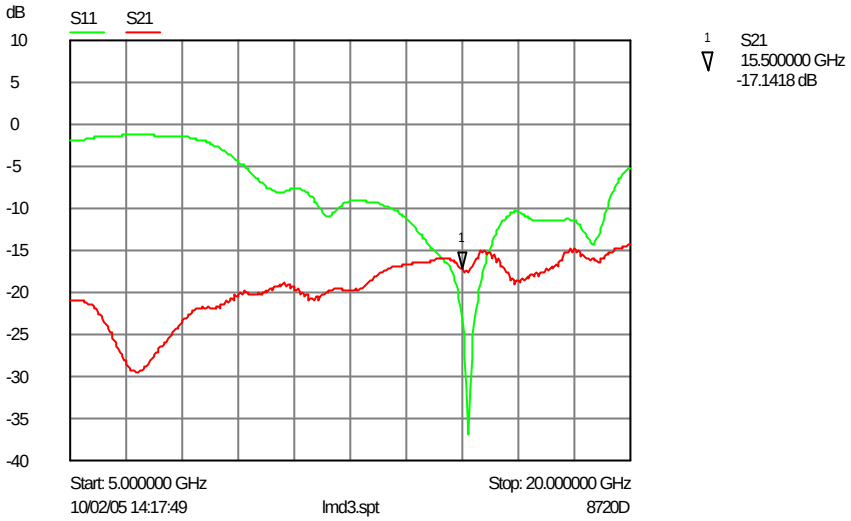

Figure 13: Measured performance of off-case SPDT, including test jig losses

Figure 14 shows the measured performance of the on-case SP4T, including test jig losses. At 15.5GHz (mid-band) the measured insertion loss, including the test jig, is 2.4dB. Removing the test jig losses of 0.6dB leaves a measured insertion loss of 1.8dB for the SP4T. This is around twice the 0.85dB loss of the SPDT, as would be expected.

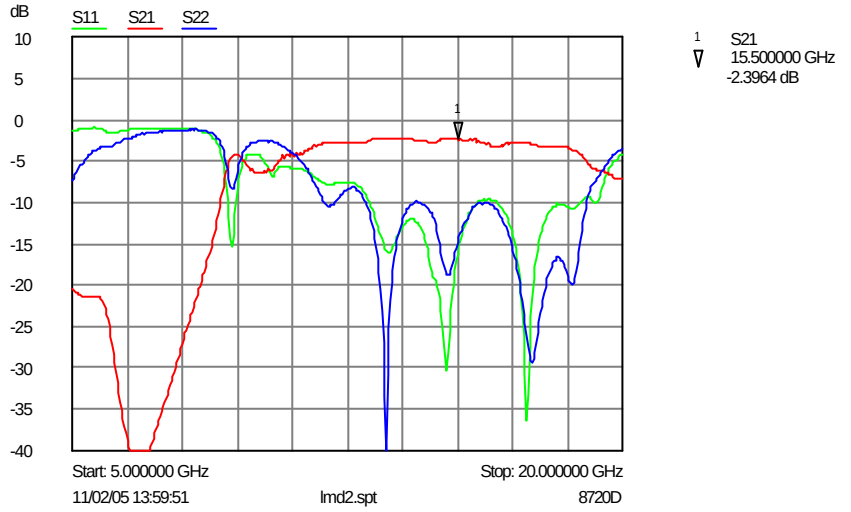

Figure 14: Measured performance of on-case SP4T, including test jig losses

The measured isolation of the SP4T is shown in Figure 13 and is 18dB at 15.5GHz.

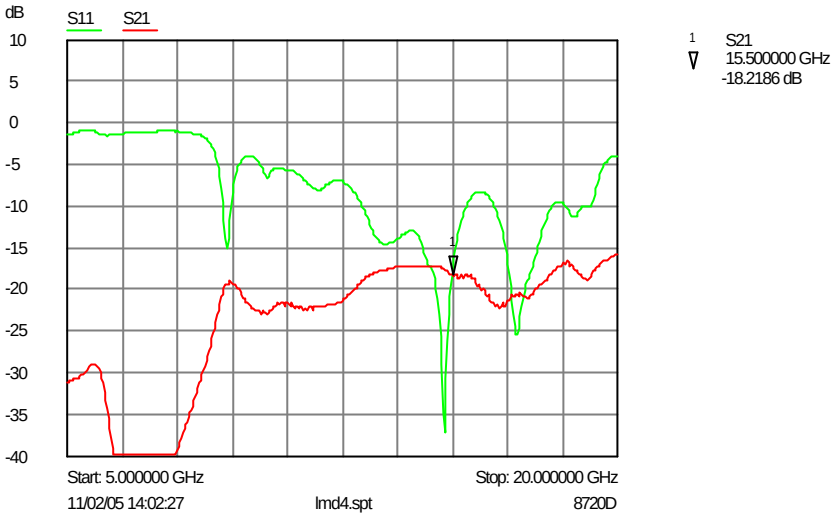

Figure 15: Measured performance of off-case SP4T, including test jig losses

The power transfer characteristics of the switch were also measured. However at the maximum output power available in the lab, at Ku band, (2W) no significant compression in the switch was discernible.

Conclusions and Summary

Low-cost, low loss SPDT and SP4T switches covering 12GHz to 19GHz have been designed, realised and evaluated. The SPDT insertion loss is 0.85dB at mid-band with an isolation of 17dB. For simplicity of layout and realisation, the SP4T is constructed from 3 SPDTs and has an on-case insertion loss of 1.8dB, around double that of the SPDT, and an isolation of 18dB. The switches do not show any significant compression at power levels of up to 2W. Measurement at higher input power levels has not yet been undertaken.

References

[1] Devlin, L.M., Dearn, A.W. and Pearson, G.A. “Low Loss MM-Wave Monolithic SP4Ts”, proceedings of the 2001 “Workshop on Design for Broadband Wireless Access”, Cambridge, England, 3rd May 2001

[2] Street, A.M. “RF Switch Design”, Proceedings of the IEE Tutorial Colloquium on “How to Design RF Circuits”, April 5th 2000, pp 4/1-4/7

[3] Matthaei, Young and Jones, “Microwave Filters, Impedance-Matching Networks and Coupling Structures”, Artech House 1980, ISBN 0-89006-099-1