# 60 GHZ TRANSCEIVER BUILDING BLOCKS AND MEASUREMENT

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**Abstract**

*The increasing demand of frequency bandwidth for broadband wireless applications results in surveys to new frequency bands, suitable for high data-rate applications. The 60 GHz band is one of the candidates for this type of applications. Due to the high operating frequency the 60 GHz topic is challenging for IC design and measurement. Integration of building blocks is important to minimise high frequency interconnects, which are uncertain design factors. Building blocks for a 60 GHz transceiver MMIC and antenna, designed and measured at TNO, are presented in this paper.*

## Introduction

The increasing demand of frequency bandwidth for broadband wireless applications results in surveys to new frequency bands, suitable for high data-rate applications. Nowadays the solutions are ultra wide band (UWB) from 3 to 10 GHz and around 60 GHz, where a large continuous bandwidth is available. Standardisation for the 60 GHz frequency band is not yet finished (reference [1]), but bandwidth limitation has to be taken into account during design.

Monolithic microwave integrated circuits (MMICs) and an antenna, designed for an integrated 60 GHz transceiver are presented in this paper. The designed blocks are meant for the 60 GHz band. Due to the high operating frequency and large bandwidth the topic is challenging for MMIC / antenna design and measurement.

## 60 GHz system and integration

Around 60 GHz an unlicensed frequency band will be defined for wireless communication systems. Systems at this frequency level are typically meant for in-house communication. The signal at 60 GHz suffers high attenuation through walls and windows, which makes it suitable for wireless communication channels in a single room without disturbing the neighbour rooms.

When designing at mm-wave frequencies, care has to be taken with high frequency interconnects between the transceiver's building blocks. These interconnects need low tolerance, are lossy and have significant influence on the system's performance. Therefore the possibility for integration is an important issue for transceiver design at mm-wave frequencies to minimise the amount of high frequency interconnects.

During the design of the transceiver MMICs, integration of the presented building blocks on a single chip is taken into account. Figure 1 presents a block schematic of the proposed transmitter MMIC.

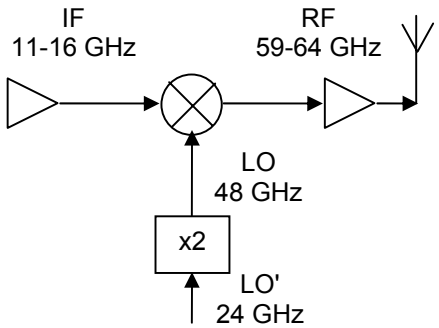



Figure 1. Block schematic transmitter IC

**Semiconductor technologies for mm-wave transceiver integration**

The transceiver systems in the 60 GHz band are meant for commercial applications. This makes design in low-cost technologies an important topic. CMOS and silicon germanium (SiGe) technology are getting more and more suitable for mm-wave applications. These technologies are getting cheaper when mass production is coming up, which is a significant parameter for commercial applications in the future.

At this moment 60 GHz applications are not ready for mass production. The standardisation is not yet finished and the development of frontends at this frequency is under investigation. This means that the volume is not yet large enough to design the transceiver system in silicon technology. Gallium arsenide (GaAs) has been used in stead, since costs for production start-up are significantly lower than for e.g. CMOS.

Gallium arsenide technology is a mature technology for microwave design and is proved to be suitable for mm-wave front-end design (reference [2] and [3]). This paper presents an EBG antenna and GaAs MMICs, designed and measured for integration of a 60 GHz front-end for wireless communication.

**Designed MMICs and antenna**

The 60 GHz front-end MMICs are designed at TNO in GaAs PHEMT technology of UMS (PH15). During the design of the transceiver circuits the minimisation of 60 GHz interface connections are taken into account. The power levels are compatible with silicon RFICs to be able to connect the mm-wave front-end to the RFICs. These silicon RFICs are developed in parallel by Philips Research in a joint project.

During the design of the circuits and antenna electro-magnetic (EM) simulators were used intensively to characterise and verify the needed components and libraries. Mostly Agilent ADS, Momentum and Ansoft HFSS were used. The results of these simulators were not consistent at 60 GHz. This means that every step and result has to be verified.

*Medium power amplifier (MPA)*

The medium power amplifier (MPA) is a four stage amplifier, which drives the antenna. For integration the antenna has to be small, which results in a low antenna gain, so a driver is needed. The MPA has to compensate the introduced loss by the passive mixer.

Good matching is crucial for the MPA design, because the available gain is limited and close to technology cut-off. Interdigitated finger capacitors are designed with Ansoft HFSS and Agilent Momentum to be able to have smaller capacitor values with the same inductive behaviour as the available library models. With these capacitors higher resonance frequencies can be achieved in the matching networks. The capacitors fingers are designed, on the edge of the process parameters, in the thin metal layer to allow smaller spacing. The fingers are 50 µm long, 10 µm wide and the edge to edge separation is 5 µm.

Figure 2 shows a microscope photograph of the designed MPA MMIC. The size of the MPA is approximately 3x1.8 $mm^2$. The MPA consists of 4 gain stages. FETs of 4x25 µm, 6x35 µm, 6x55 µm and 2 FETs of 6x45 µm are used in stage one to four respectively. The MPA has an $S_{11}$ = -10 dB bandwidth from 60 GHz to 66 GHz. $P_{1dB}$ is measured at +14 dBm and a saturated output power of +20 dBm.

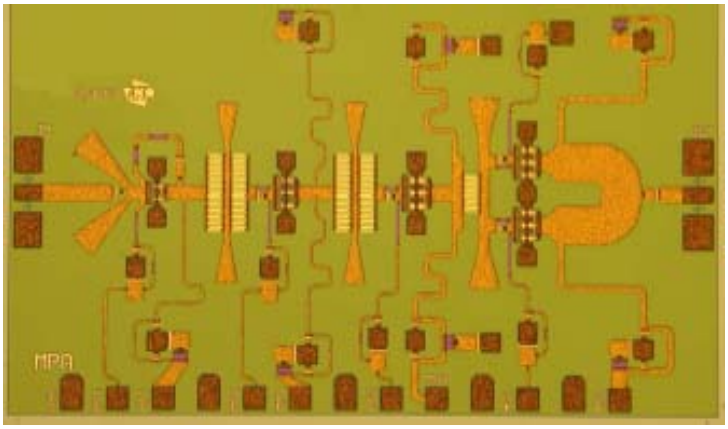



Figure 2. Photograph of the 60 GHz MPA

Small signal measurement and simulation results are presented in Figure 3. The graph shows a good match between the measurement and the simulation data. Gain compression measurement results on different frequencies are presented in Figure 4.

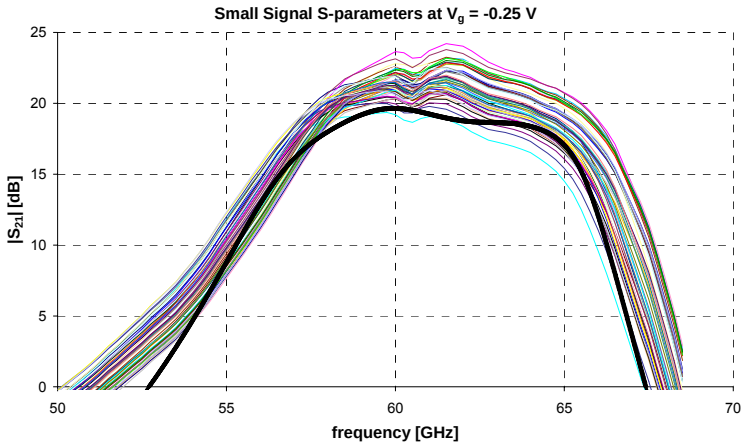



Figure 3. Measurement results of the medium power amplifier

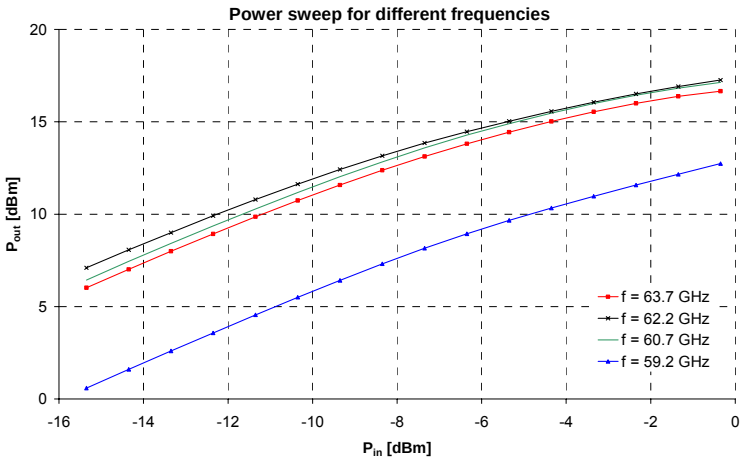



Figure 4. Measured power sweep vs frequency of the MPA

*LO chain*

The chipset needs a 48 GHz LO signal with small spurious signals. Due to the compatibility with silicon RFICs the LO frequency cannot be supplied directly, therefore a frequency doubler is added to the LO chain.

The frequency doubler consists of two FETs in parallel, driven with equal signals, 180˚ out of phase. The input of the frequency doubler is a rat-race, which generates the equal signals at 24 GHz. A rat-race with λ/4 lines would be too large; therefore it is designed as a semi-lumped circuit.

The LO-chain MMIC is about 2.9x1.25 $mm^2$. As shown in Figure 5 the LO-chain consists (from right to left) of a 24 GHz pre-amplifier, a rat-race based frequency doubler and a 48 GHz driver amplifier. The realised fundamental suppression is 35 dBc. The measured gain and output power are presented in Figure 6.

The fundamental suppression could have been better. A frequency shift in the rat-race circuit of 2.5 GHz was observed. This resulted signals at the FETs that were of unequal amplitude and not exactly 180˚ out-of-phase. Therefore the cancellation of the fundamental frequency was less than perfect.

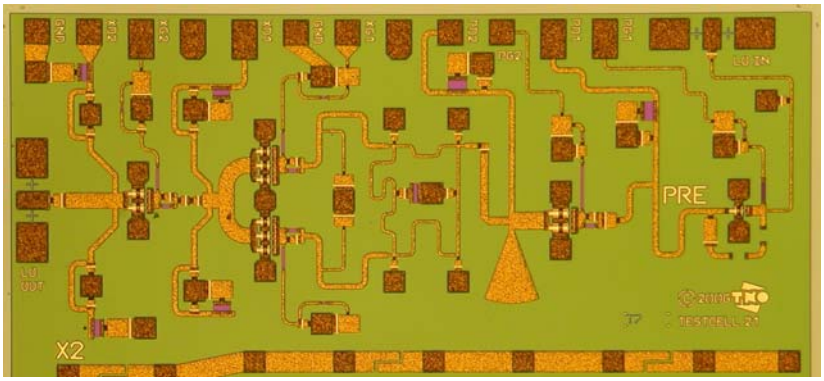



Figure 5. Photograph of the 48 GHz LO chain

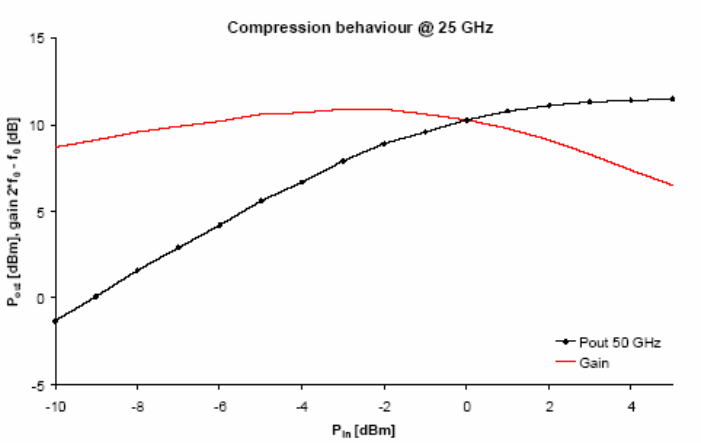



Figure 6. Measured gain and output power of one sample

*Passive mixer*

For the transmitter the LO – RF isolation is of prime importance, as the MPA would amplify and transmit out-of-band signals. To alleviate the suppression requirements of the filter after the mixer, a part of the filtering has been implemented in the mixer.

The passive mixer MMIC designed (Figure 7), consists of two diodes, pumped 180˚ out of phase. The LO – RF isolation is achieved by the rat-race hybrid. LO – IF isolation is limited. This is of minor importance since the LO lies far from the IF band. This can easily be filtered out externally. The measured conversion loss is 7 dB.

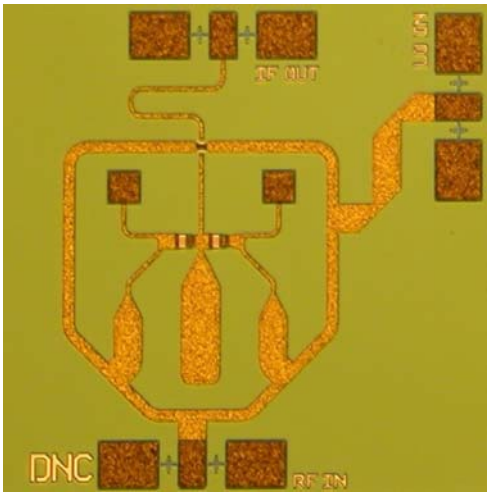



Figure 7. Photograph of the passive mixer (1.2x1.2 $mm^2$)

*EBG antenna*

A future step in integration is the integration of the antenna. A first step is to develop a small antenna structure, which can possibly be integrated. The electronic bandgap (EBG) technology seems to be a good candidate.

A balanced EBG antenna is designed for 5 GHz bandwidth at 60 GHz. The EBG technique is used to suppress substrate waves and to increase the antenna's efficiency (reference [4] and [5]). Figure 8 shows a photograph of 9 antenna samples.

The antenna is designed on high resistive silicon (Philips PiCs technology) with two metal layers and a SiN separation layer. The EBG structure is realised on the top metal layer where a metal layer which can be put on the back of the substrate will act as a reflector. A balun is integrated with the antenna to have a single ended feed, which makes measurement easier.

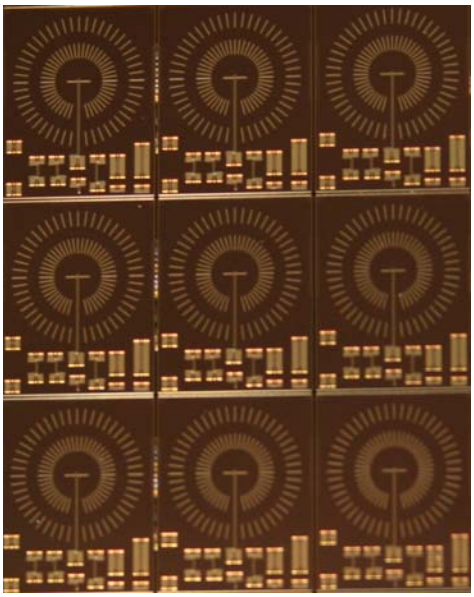
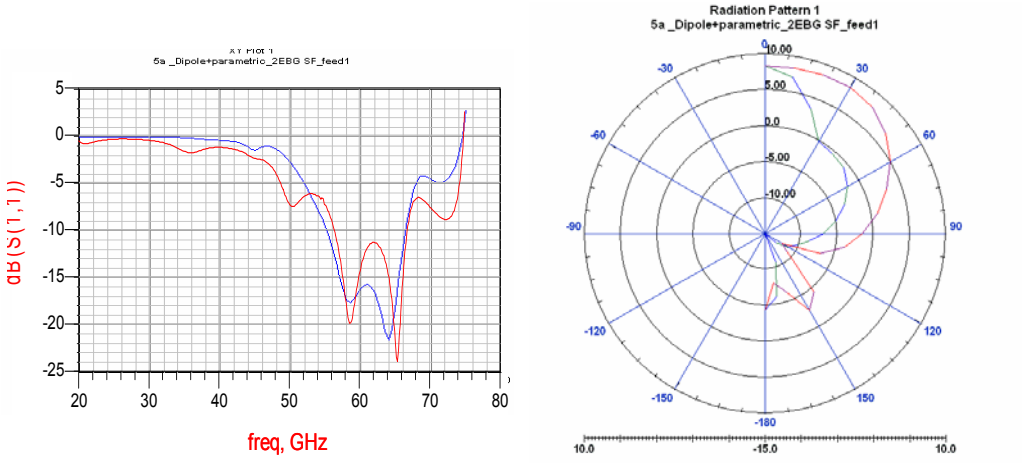


Figure 8. Photograph of the designed EBG antenna (9x)

The antenna small signal simulation results are presented in Figure 9. In Figure 9a the blue line represents the $S_{11}$ of the EBG antenna with passivation layer and reflector. The red curve represents the $S_{11}$ of the antenna with balun. The influence on the bandwidth of the balun is minimal.

The antenna pattern simulation (Figure 9b) results show in red the antenna pattern over the H-plane and green the antenna pattern over the E-plane.




(a) (b)

Figure 9. Simulation results of the designed antenna. (a) $S_{11}$ and (b) antenna pattern

**Measurement methods**

Measurement at 60 GHz is an accurate job. Calibration has to be done carefully and the cable loss is high (≈10 dB/m). Manual probing with unavoidable variations in contact location can cause significant phase offset.

On wafer measurements were carried out on the MMICs with the automated measurement setup at TNO. A 67 GHz network analyser (PNA) from Agilent (Figure 10) is used for S-parameter measurements. 67 GHz RF-probes were used and DC probes with 120 pF capacitances at the probe tip were used for stabilisation.

On all circuits small signal S-parameter measurements were done. Frequency offset measurements were carried out on the mixer and the doubler. Power sweep measurement with the PNA was done on the MPA. Because we were limited to 2-port measurements, synthesis of 3-port data from 2-port measurements was done on test structures.

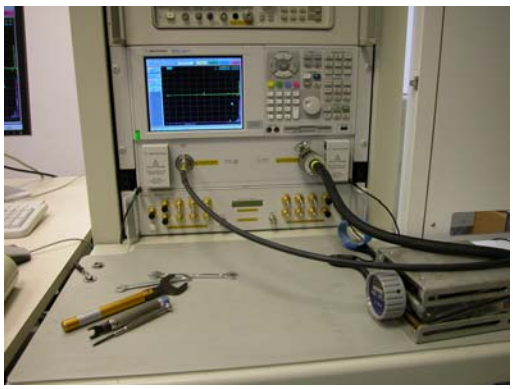


Figure 10. Photograph of the 67GHz network analyser

The antenna structures are processed and delivered on wafer which precluded measurement in a regular near field or far field range. Either the antennas had to be mounted on a board and connectorised (after dicing of the wafer) or RF on-wafer probes with microscope had to be fitted in the antenna measurement facility. A third option, which has been chosen, is to build the antenna measurement facility on the wafer probe station that is normally used for on-wafer IC measurements.

A planar XY scan has been performed at a height of a few wavelengths above the wafer surface. A standard Agilent 67 GHz network analyser has been used for the antenna pattern and input reflection measurements. Input reflection measurements show a -10 dB bandwidth of 7 GHz. Figure 11 presents a photograph of the wafer with probes.

The results of the near field antenna measurements are being validated at the moment.

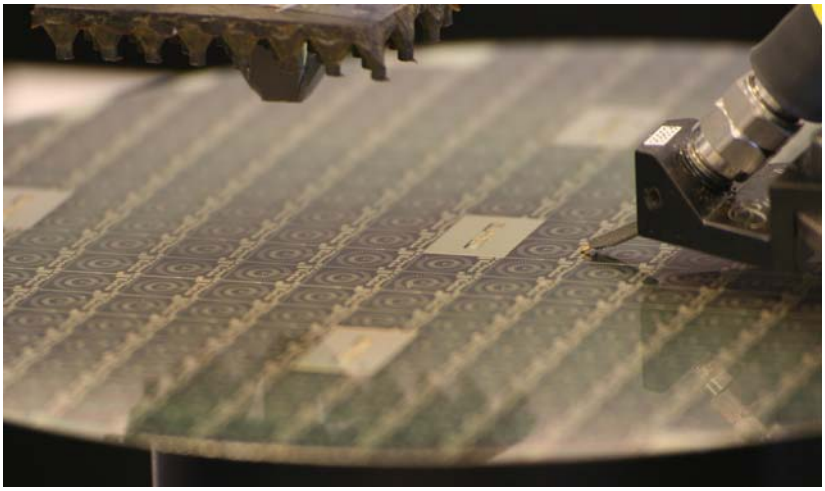


Figure 11. Photograph of a probed antenna with a waveguide probe above

**Conclusions and future development**

60 GHz frontend MMICs and an antenna are successfully designed and measured. An overall bandwidth of 5 GHz is achieved.

Extensive EM simulations are important for the design at mm-wave frequencies to characterise and verify the needed components and available library models. Accurate calibration and de-embedding are crucial for measurements at these frequencies.

CMOS technology is at the edge of 60 GHz, but is only attractive for high volume production. The maturity of GaAs technology is very suitable for 60 GHz design for lower volume products.

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