Design and measurement of a wideband InP SDLA

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Abstract

The design and measurement of an Indium Phosphide (InP) Wideband Successive Detection Logarithmic Amplifier (SDLA) is described in this paper. The circuit is realised as a Monolithic Microwave Integrated Circuit (MMIC) based on double heterojunction bipolar transistor (DHBT) technology and uses cascaded differential amplifier gain stages coupled to full wave detectors, achieving a piecewise linear approximation to the ideal logarithmic response. The MMIC also includes a limited RF output and on chip adjustment for gain and detector slope. The integrated circuit operates across 2-18GHz and provides a 33dB dynamic range with a ±1dB log error. The limited RF output signal provides a signal level of >-2.2dBm and consumes 690mW from a single -5V supply rail in a chip area of 2.58mm^2.

1 Introduction

Logarithmic amplifiers are widely used in the EW products to process amplitude information of incoming RF signals. These components are used to compress the wide dynamic range of the incoming signal into easily manageable levels.

There are several architectures for realising the logarithmic amplifier [1]: True Logarithmic Amplifier (TLA), Detector Log Video Amplifier (DLVA) and the Successive Detection Logarithmic Amplifier (SDLA). True Logarithmic amplifiers differ from the other two types in that they do not provide envelope detection, they process the RF or Intermediate Frequency (IF) signals directly to output an RF signal which is a logarithmic interpretation of the input signal. In this case both the amplitude and phase information is preserved. Detector Log Video amplifiers (DLVAs) use diodes to detect the RF signal and logarithmically amplify the resulting video signal. These circuits have a dynamic range limited by the linear/square law response of the detector diode but can be increased by using parallel detector circuits. Successive Detection Logarithmic Amplifiers (SDLAs) demodulate the input RF signal and provide a video output which is proportional to the logarithm of the input amplitude. They use multiple limiting gain stages coupled to detector circuits to create a piecewise approximation to the logarithmic response (figure 1). The logarithmic error (i.e. deviation from the ideal line) performance of an SDLA is determined by the number of stages, N, the amplifier gain, G and the detector response.

SDLAs can operate across wide bandwidths with large dynamic ranges, have excellent pulse response characteristics and can be configured with or without a limited RF output signal port. Furthermore, the use of a differential circuit configuration allows a dual RF output.

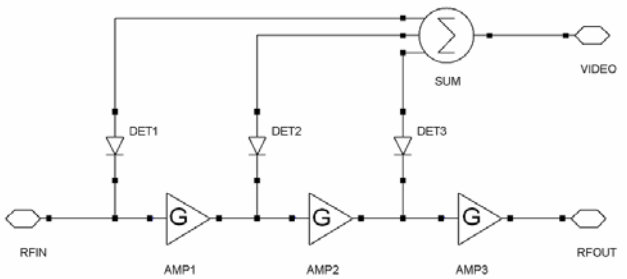

Figure 1 (a) SDLA Block Diagram

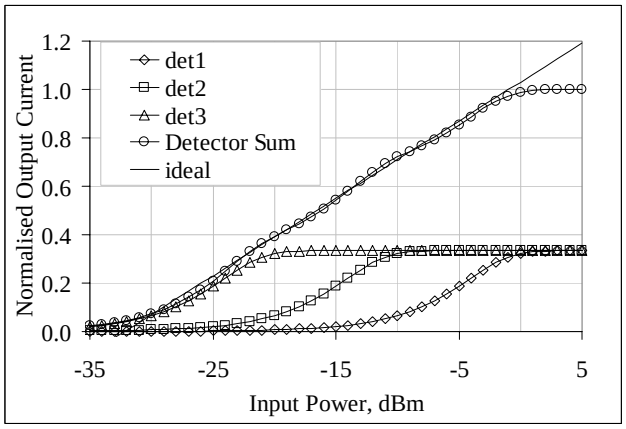

Figure 1 (b) SDLA Ideal Logarithmic Response

SDLA circuits have been demonstrated in hybrid and monolithic form, spanning differing technologies [2,3,4,5]. This class of circuit is ideally suited to monolithic processes due to uniformity of gain and detector stages, which are key in realising a low logarithmic error approximation to the ideal function. This, together with the maturing of Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT) technology providing transistors with very high f_T figures, offers the

possibility of successful implementation of SDLA circuitry in the high microwave region.
The Global Communication Semiconductors Inc. (GCS) InP SHBT and DHBT processes offer up to three-level metal interconnect for medium scale integration (MSI) and high speed (f_T and f_{MAX} >150 GHz) operation at low DC power (Vce=0.9V, Jce=1mA/μm^2). The performance parameters of the GCS process are summarised in Table1.

Parameter	Value
Beta	30
f_T (GHz)	150
f_{MAX} (GHz)	150
BVcbo (V)	8
BVceo (V)	7
BVbeo (V)	2
Vturn_on (V)	0.95
Vce_offset (V)	0.3

Table 1: Specification for GCS InP DHBT process.

2 Design Requirements

The chip design requirement was flowed down from module specifications needing to produce a Log Amp function covering a bandwidth of 2-18GHz with a dynamic range of 60dB whilst also providing a limited RF output capability. A multi-chip approach was considered to be the best option with two or more MMIC chips cascaded to provide the full SDLA circuit function. This multi-chip architecture was selected to avoid any potential stability problems associated with high gain and bandwidth on a small chip, to allow the use of interstage filtering to reduce noise levels in lower bandwidth applications and offering flexibility to make the chip available for low dynamic range detection circuits.
The design is required to have a high video bandwidth such that detection of short duration pulses is possible.
The performance is summarised in Table 2 below.

Frequency Range		2GHz-18GHz	Min
Dynamic Range	2GHz-18GHz	60dB	Min.
Linearity	2GHz-18GHz	±1.5dB	Typ.
Video Slope	2GHz-18GHz	TBD	Typ
Frequency Flatness	2GHz-18GHz	±1.5dB	Typ.
RF limited output power	2GHz-18GHz	-5dBm	Typ
Video Bandwidth		100MHz	Typ
Current (V_{EE} = -5V)	I_{EE}	150mA	Typ
Gain Variation	-40°C to +85°C	external compensation	

Table 2: Specification for the full SDLA function

3 Circuit Design

In order to design the SDLA, a system model was created to provide an analysis of the required amplifier stage gain, the detector parameters and to define the video output characteristics.

Using the requirements of section 2, and assuming a two MMIC solution, a chip with an overall minimum gain of 30dB is required. This can be achieved by several combinations of gain and number of stages (2x15dB stages, 3x10dB stages or 4x7.5dB stages etc.). In General, reducing the gain and increasing the number of stages improves the log slope linearity but at the expense of increased circuitry and supply current.

3.1 Detector Circuit Design

A useful detection circuit in bipolar technology is the full wave detector. These have previously been reported in the literature and have been used for many lower frequency SDLA designs [5,6,7,8].
The full wave rectifier circuit operation can be described by extending the analysis of the output current of a simple differential pair and then unbalancing the arms, either by a voltage offset or by unequal device sizes [7,8]. The output current of a basic differential amplifier, figure 2(a), can be described by

$$\Delta Iout = IC1\text{-}IC2 = IEE \tanh(Vi/2VT) \quad (1)$$

Adding an offset voltage (Vos) between the input terminals, as in figure 2(b), the differential output current is modified, shifting the response by the offset voltage

$$\Delta Iout = IC1\text{-}IC2 = IEE \tanh((Vi+Vos)/2VT) \quad (2)$$

Combining two of the unbalanced differential pairs with parallel inputs and cross coupled outputs, figure 2(c), the output currents can be written as

$$Ic1 = IEE/(1+e^{-(VA/VT)}) \text{ and } Ic2 = IEE/(1+e^{+(VA/VT)}) \quad (3)$$

$$Ic3 = IEE/(1+e^{-(VB/VT)}) \text{ and } Ic4 = IEE/(1+e^{+(VB/VT)}) \quad (4)$$

Where $VA = V_i+V_{OS}$ and $VB = V_i-V_{OS}$. Combining equations (3) and (4) the differential Output current is

$$\Delta Io = Io1 - Io2 = (Ic1 - Ic2) + (Ic3 - Ic4) \quad (5)$$

$$\Delta Io = IEE[\tanh\{(V_{OS}+V_i)/2VT\}+\tanh\{(V_{OS}-V_i)/2VT\}] \quad (6)$$

This function can be shown to have a square law range, making it ideal as a detector, providing a video output proportional to input signal level after low pass filtering.

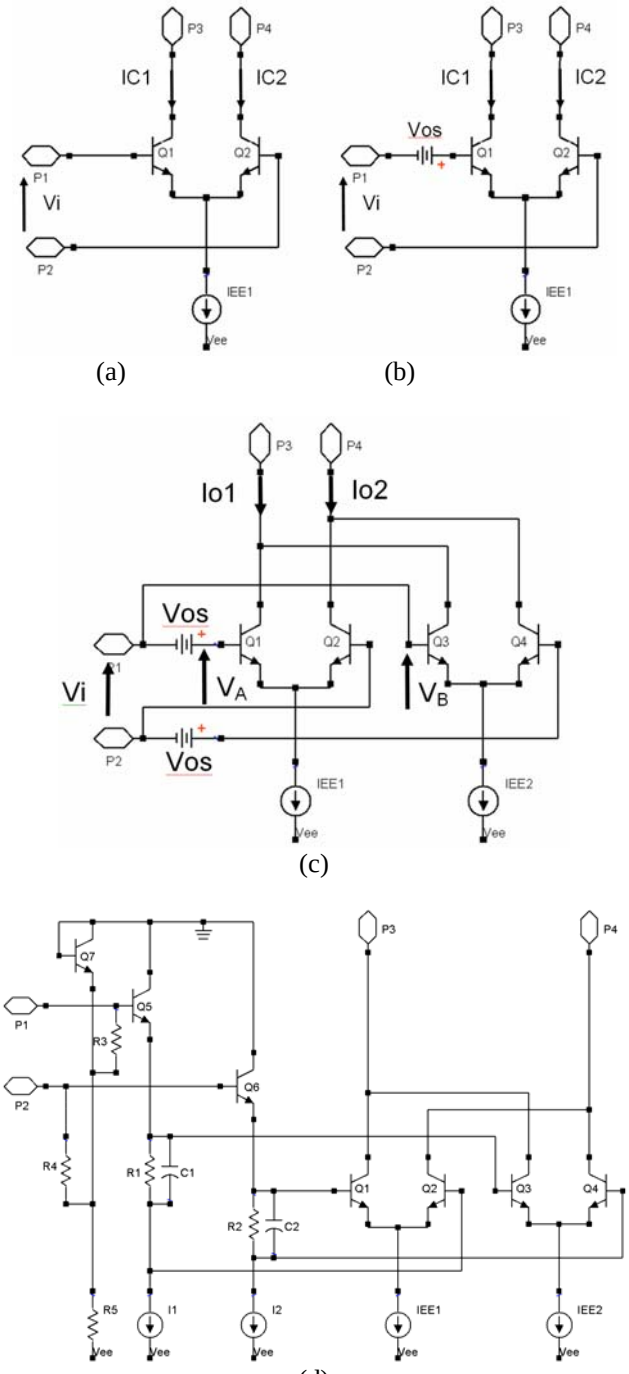

Figure 2 Development stages of a Full wave rectifier circuit from (a) Basic differential pair, (b) Unbalanced differential pair and (c) Two cross coupled unbalanced differential pairs and (d) the circuit implementation used in this design.

The circuit implementation used in this design, figure 2(d), uses an offset voltage in the base terminals, achieved by the use of current source I1 and parallel resistor capacitor network R1/C1 for the 'true' input and I2, R2 and C2 for the 'compliment' signal. The output is taken from ports 3 and 4 via simple low pass RC video filters. This circuit has been proven to work on lower frequency designs within SELEX using a GaAs HBT design. Figure 3 shows the RF performance of the full wave detector. These results demonstrate that the devices and architecture are capable of delivering performance beyond 40GHz.

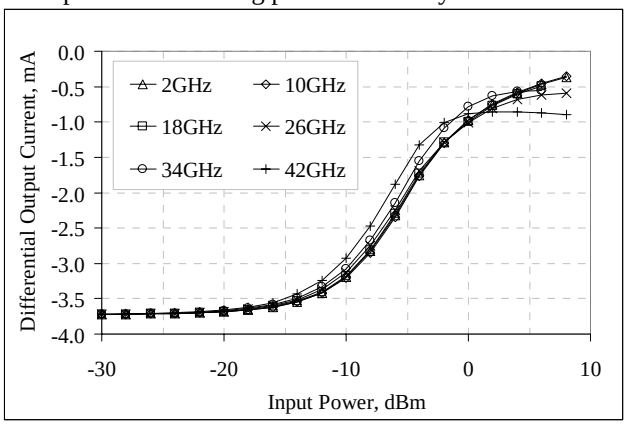

Figure 3 Full wave detector circuit simulated response.

3.2 Gain Stage Design

The gain stages are based around a differential pair configuration. The minimum stage gain of 10dB is required to satisfy the requirements of a three stage MMIC. Using a slightly higher gain is desirable in practice to add margin and cope with the gain variation versus temperature, resulting in a design with a gain of 3.5 (11dB) per stage.
The amplifier also requires a limiting characteristic above the detector response [8]. Having the gain limiting defined at a single point (the detector stage) helps reduce the effects of amplifier gain variation due to temperature and bias changes on the overall SDLA design.

The voltage gain, A_{VG}, of a common emitter differential amplifier stage is simply defined by collector resistor R_C and emitter resistance R_E, which includes both external emitter degeneration resistor and internal R_e, the thermal resistor.

$$A_{VG} = R_C/R_E \qquad (7)$$

The limiting is also defined by the value of R_C and the current in the long tail pair. The tail current cannot be increased without limit as the current density of the active devices needs to be considered, with a limit of 1mA per um of emitter width for reliable operation. Therefore a trade-off is required on the ratio of R_C and current. Using (7) and assuming a value for the external resistor R_E comparable to R_e to ensure temperature stability, the value of R_C can be set. Smaller values of R_C offer higher frequency performance in a common-emitter stage but require a larger current for a given signal swing.
High frequency performance can be improved by the use of a cascode configuration in place of the common-emitter stage within the differential pair. This allows reasonable values for R_C and the tail current to be used. Figure 4 shows the circuit diagram for the amplifier stages with the

cascode configuration defined by transistors Q1/Q2 and Q3/Q4.
The basic performance of this circuit (figure 5) allows operation in excess of 30GHz at +25°C, using standard foundry models.

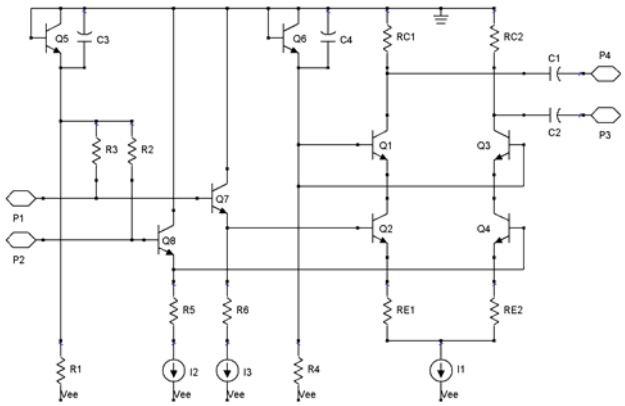

Figure 4 Cascode Differential amplifier configuration.

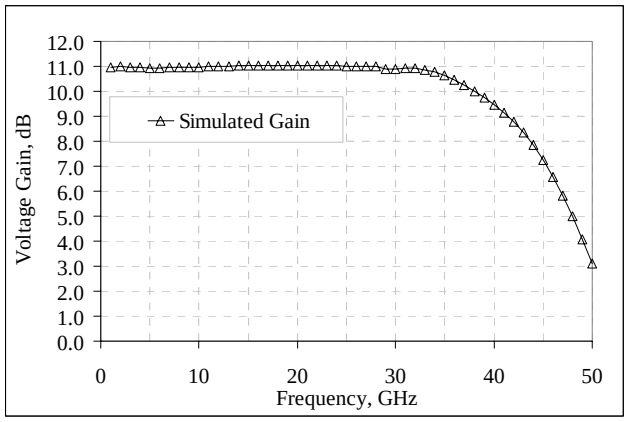

Figure 5 Simulated differential amplifier response

3.3 Full MMIC Design and Layout

Three detector and gain stages are combined together in a single chip, along with an active balun and output driver stage optimised to drive into a 50 ohm load. The effect of impedance loading is mitigated in the design by the use of emitter follower buffers between the amplifier outputs and the input of the succeeding detector and amplifier stages.

The layout of the MMIC is governed by the area to fit the active circuits along with the RF, DC/video and control pads. Further design considerations come directly from the GCS InP DHBT process. This is a vialess process thus ground connections are made using a coplanar waveguide (CPW) configuration, making it ideally suited to differential circuits. This leads to a compact active circuit area, at the expense of overall chip dimensions for the ground plane reference. These chip dimensions are also constrained to a maximum size governed by array reticule conditions and bulk waveguide modes in the frequency range of operation which are possible in some CPW layouts, especially Grounded CPW. Considering these issues, the chip size is 2.15mm x 1.2mm.

External connections are made using standard bond pads configured as GSGSG pads for RF signals. DC/control connections are made with two standard six bond pad arrays and cover functions including DC input, video output, Detector slope adjustment and amplifier gain variation. There are multiple ground connections to allow good circuit to MMIC grounding.

Simulation of the final MMIC chip is shown in figure 6 and predicts a dynamic range of 33dB with a nominal logarithmic slope of 0.25mA/dB.

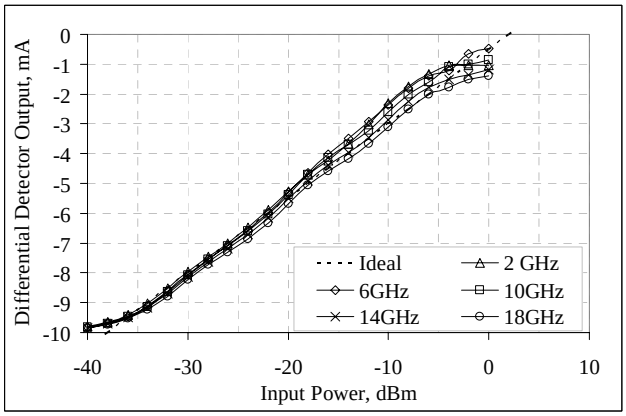

Figure 6 Simulated 3 stage SDLA MMIC transfer characteristic.

Cascading two of these chips together, using differential connections between MMICs, shows a dynamic range in excess of 65dB which meets the design requirement. The simulation results for the dual chip logarithmic amplifier are shown in figure 7.

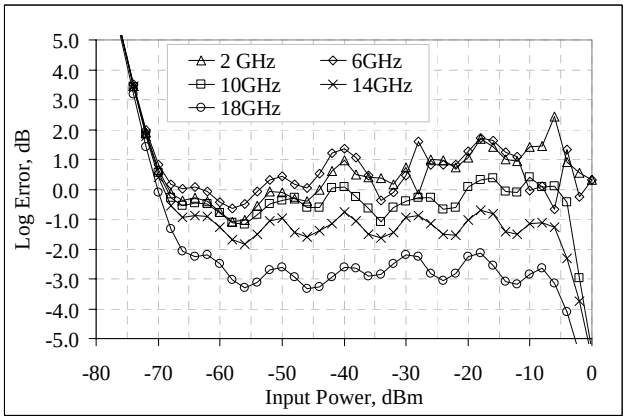

Figure 7 Simulated SDLA Dual MMIC transfer characteristic.

4 Results

Fabrication of the MMIC was completed June 2007. A photograph of the fabricated chip is shown in figure 8. The MMIC was measured RF-on-wafer (RFOW), using a Cascade Microtech summit 12000 series wafer prober and standard ACP200 GSGSG coplanar probes.

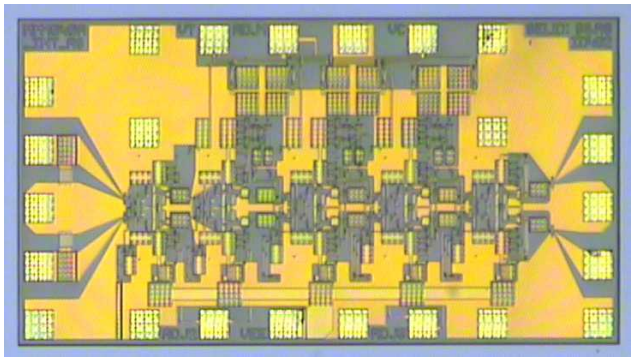

Figure 8 Chip photograph of InP SDLA MMIC

Small signal s-parameters were measured under single ended drive and are shown in figure 9. This shows good agreement to simulation for input return loss but reduced small signal gain of approximately 23dB across the band of interest. It should be noted that the gain will be 6dB lower than expected due to the single ended drive conditions.

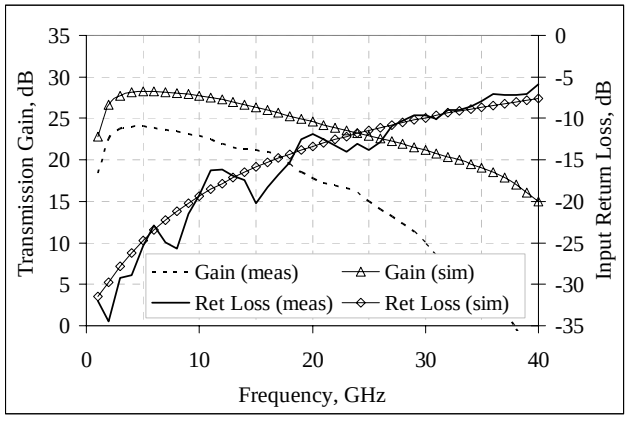

Figure 9 Small signal s-parameters.

The basic logarithmic amplifier results are shown in figures 10-13 for a fixed bias voltage of -5V, and no connection for the adjust pins. Figure 10 shows the logarithmic transfer function for the chip driven with a single ended input, along with an ideal line of 0.22mA/dB, the nominal midband slope. Figure 11 shows the transfer characteristic when normalised to this fixed line. These results show the effect of the gain roll-off noted in figure 9. Normalising the transfer characteristic to a best fit line at each frequency (Figure 12) shows a maximum error of ±1dB across a 33dB dynamic range, with slopes ranging between 0.20mA/dB and 0.24mA/dB, which is in close agreement to the simulated prediction of 0.25mA/dB.

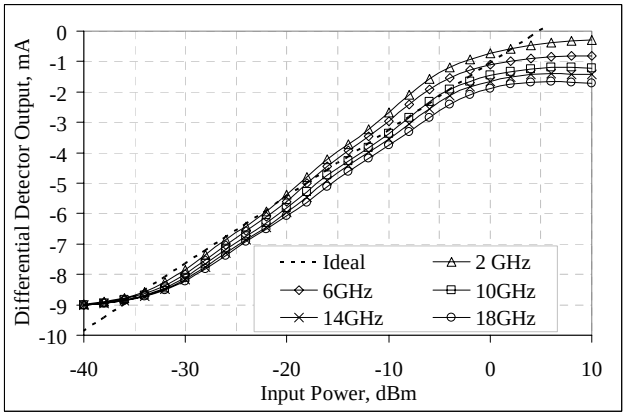

Figure 10: SDLA RFOW Logarithmic transfer characteristic.

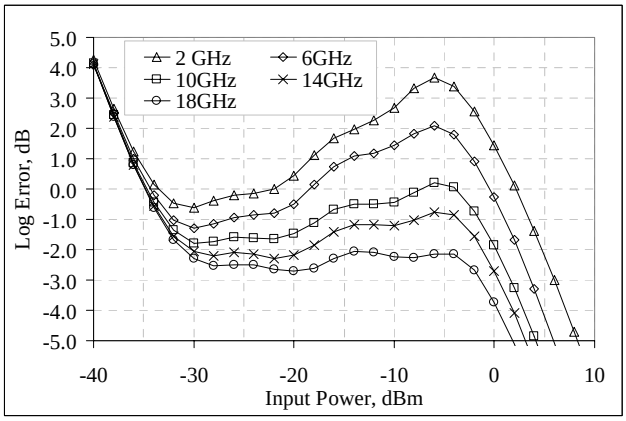

Figure 11: Normalised log error to best fit line of 0.22mA/dB.

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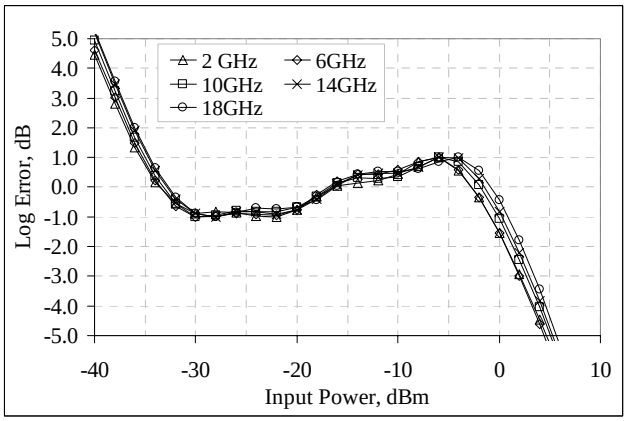

Figure 12: Normalised log error for best fit line at each frequency.

The limited RF output from the MMIC is shown in figure 13. This can be seen to be constant with frequency, varying only between 0dBm and -2.2dBm, from a single ended output.

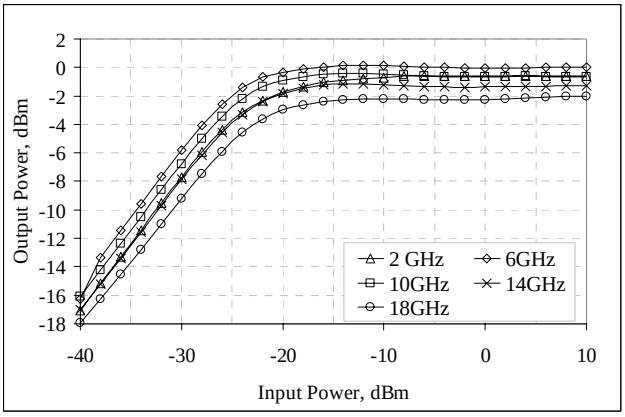

Figure 13: SDLA output power (single ended)

5 Conclusion

The design has demonstrated that SDLA performance is possible beyond 18GHz with this InP DHBT technology and circuit implementation.
Future work will focus on integration of the chips into a Logarithmic amplifier module, which includes the CPW assembly and RF launch performance, as well as refining the MMIC design to address areas of performance shortfall (slope in the frequency response) and new applications.

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