# A 9-10GHz 25W GaN Quasi-MMIC PA in QFN Package

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***Abstract*— A single stage X-band (9-10GHz) PA module has been developed using a discrete 0.25um GaN transistor with 4.8mm gate periphery, that incorporates input and output matching via discrete substrates in package. The initial demonstrator module achieves 25W of power under pulsed conditions at 9.5-10GHz with Vds=40V, a peak efficiency of 44% and small signal gain of around 12dB. The PA was assembled in a 5mm overmolded QFN package. The power density and peak drain efficiency are in reasonable agreement with the process pcm performance at this frequency, given output matching losses have to be accounted for. This work demonstrates the feasibility of prematched GaN transistors and MMIC-like modules in high volume SMT packaging and to a frequency of 10GHz.**

***Keywords - GaN HEMT, MMIC, Power Amplifier***

## I. Introduction

As an efficient alternative to a full up GaN MMIC the use of discrete matching die has recently been demonstrated at S and C band [1]. Close in pre-matching circuits with bias decoupling offer functional advantages over the conventional IMFET approaches [2-5] which typically use high dielectric substrate capacitors and inductance realized by bond wires for impedance matching. Additionally, a MMIC-like drop in solution with integrated bias decoupling can provide a superior approach, where multi pole matching/combining networks can be implemented to extend the PA's bandwidth. Removal of long series GaN die to capacitor bonds enables the sensitivity of the matching to be dictated by the passive substrate tolerances rather than bonding length variations. The component count is that of a small number of die, with a relatively low number of bonds, supplemented with the package itself. As frequency increases the disadvantage of this approach over the full MMIC becomes the sensitivity of the off die bonds, which may manifest in lower RF yields over a full MMIC, although it is better placed than an IMFET solution. Given the relative immaturity of many processes this approach also enables rapid development cycles based on existing GaN discrete arrays. With a small exception to model the off die bonds - an effective MMIC design flow is employed.

## II. Process Description and Modelling

An optically written 0.25um x 4.8mm gate GaN/AlGaN HFET on SiC provided by GCS was employed as the active device with the following parameters: Imax >1A/mm, Vbr >150V and Vto=-3V. The device was fabricated at the GCS foundry, although the process is being transferred into the M/A-Com fab. The process has back side vias, a high voltage MIM cap option and is thinned to 3mil thickness. For the passive matching an internal M/A-Com passive process has been developed. The process offers up to three metal layers, two MIM cap options, a thin film resistor, full passivation and thru substrate via after thinning to 4mil.

Characterization and modeling of the active die was carried out by initially measuring S-parameters, pulsed IV characteristics and by fundamental load pull at 10GHz. The measurements were supplemented by a preliminary CAD model based on the Parker-Skellern large signal model. Fig. 1 shows the output power loadpull contours at 10GHz of a 600um device biased at 40V and 10mA/mm achieving peak power of 36.25dBm or ~7W/mm.

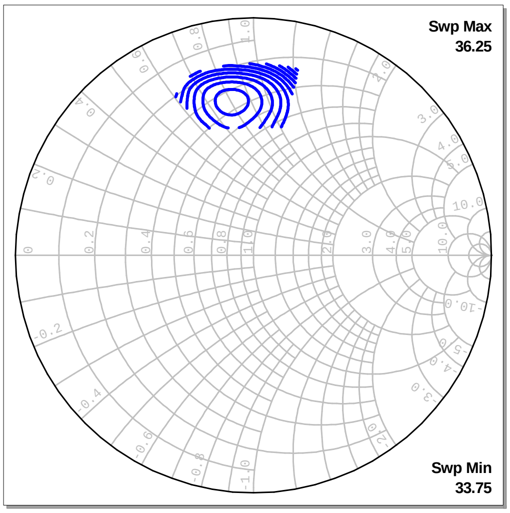


Fig. 1 Measured passive fundamental load pull contours of Pout (10GHz) measured on a 600um unit cell at 40V. Peak power is 36.25dBm, step 0.25dBm..

## III. Design

For the demonstrator PA output match, a well understood low pass topology with a close-in resonant shunt 'choke' to provide bias, was selected, with a large proportion of the design based on distributed microstrip sections. Providing the series inductance following the active device is below a certain value (depending on frequency) as per Fano[6], the shunt choke can be used to resonate with the device output capacitance and enable maximum bandwidth of the subsequent match. Other design considerations included the minimal use of MIM caps in a primarily distributed low loss output match. The on chip bias decoupling caps were doubled in series to increase breakdown voltage by a factor of two. Since the decoupling caps are low impedance in the band of interest, they need only withstand static Vdd voltages. Series RF coupling was done off chip. A simple modeling approach was taken using load pull data and S-parameter measurements on early process development die. Full EM of the output network was carried out using Axiem, and since the initial design the technique of full 3D simulation using AWR Analyst has been employed to model the bond wire transition between the active GaN and matching die. Module layout is shown in fig.2 with a photograph of an open top version of the part on 5x5mm leadframe package shown in fig. 3.

One of the main concerns of the design was the possible tolerance of the inter-die bonds and their affect for example on the load match impedance. Using the 3D EM simulations of the bond wire S-parameters versus die to die spacing, an equivalent circuit model was fitted to allow continuously variable die spacing as a parameter. The variation of bond wire lengths in a production environment was then analyzed by setting a representative tolerance on the bond inductance in the load match simulation (in our case +/-1.5mils), and carrying out a Monte Carlo simulation. Results of the simulation of load match expressed in return loss against the desired impedance are given in Figure 5. They show that the tolerances in this case were acceptable with greater than 14dB achievable in the event of the manufacturing bonding and variability of die position process extremes. Simulated small signal gain and input return loss for the module are shown in fig. 6.

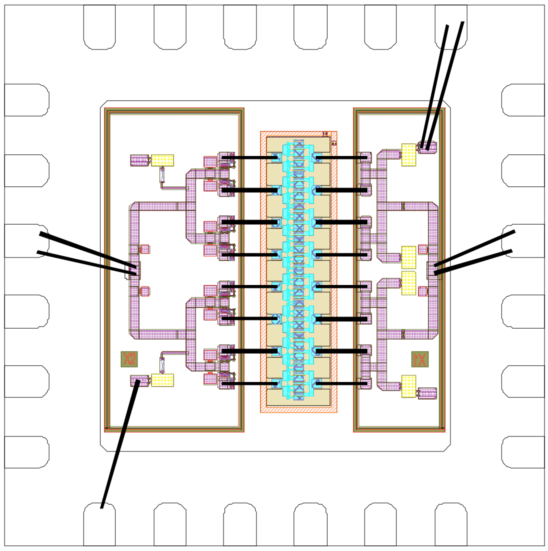

Fig. 2 Assembly layout of the 25W design showing matching die and 4.8mm discrete in package

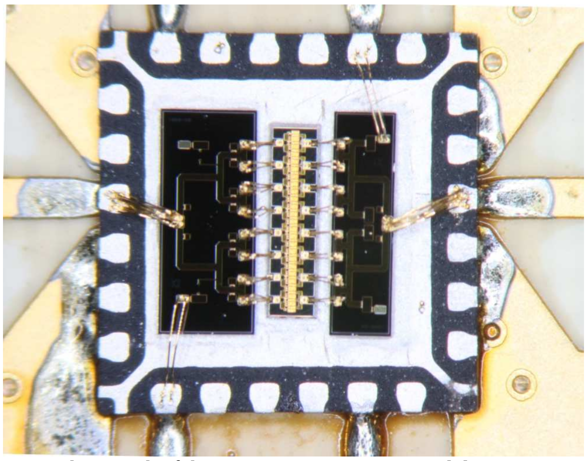

Fig. 3 Photograph of the open top 5x5mm QFN module

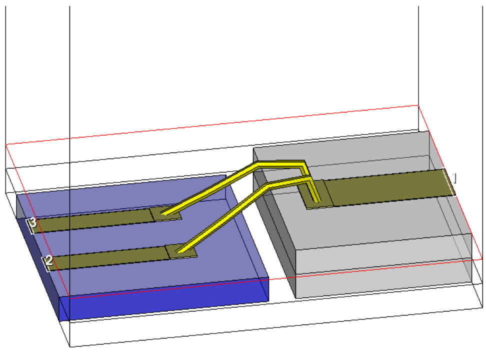

Fig. 4 GaN transition and bond wire modeling using the Analyst 3D EM simulator.

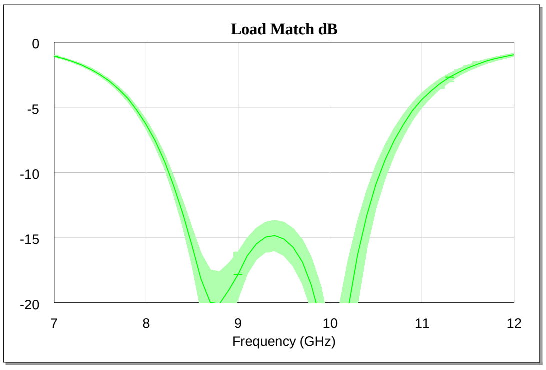


Fig. 5 Monte Carlo Simulation of bond wire length variation (to +/- 1.5mil) on output load match return loss

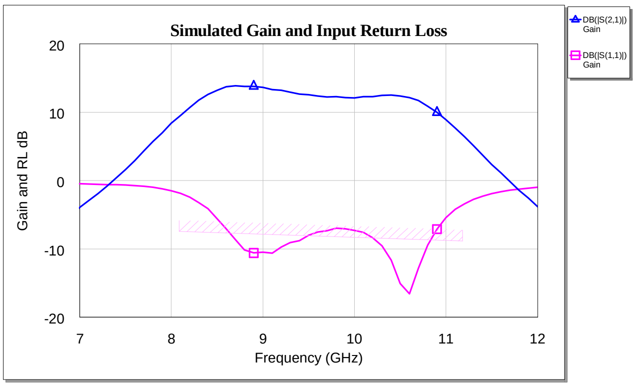


Fig. 6 Simulated gain and return loss of the PA module.

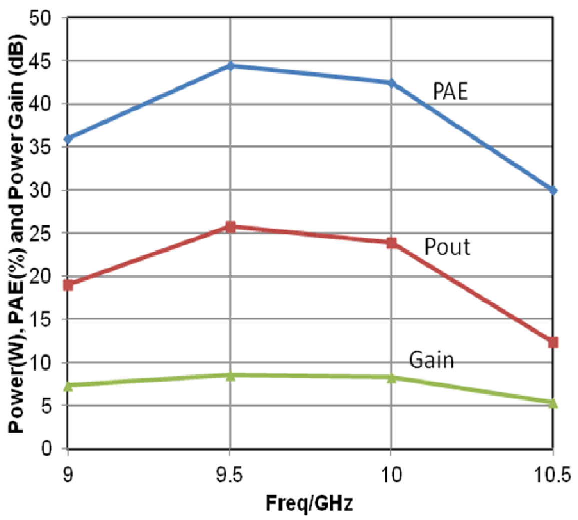


Fig 7: Output power, PAE and gain versus frequency, under Vds=40V. Pulse width 100uS, 10% duty cycle.

## IV. Results and Conclusion

As shown in Figure 7, the prototype demonstrator module achieved 25W of power under pulsed conditions at 9.5-10GHz with Vds=40V, a peak power added efficiency of 44% and power gain of 9dB. The initial input match was found to be slightly off frequency and was augmented by a single element capacitor pre-match. This was accounted for by variation in the realized transistor capacitance in comparison to that modeled by the early samples. Power density and also the peak efficiency of 44% are in reasonable agreement with the benchmark loadpull performance of the process at 10GHz given output matching losses have to be accounted for. Some improvement in efficiency could be expected by exploiting higher efficiency amplifier modes with suitable harmonic terminations. The PA module incorporates bias line decoupling and compact multi-pole combiner-matching in a low cost drop in MMIC type approach. The methodology has been performance validated and shown to enable the design of high volume assembly compatible surface mount packaged GaN based PA modules with MMIC like functionality, at a frequency of 10GHz.

## References

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