Analyzing Device Behavior at the Current Generator Plane of an Envelope Tracking Power Amplifier in a High Efficiency Mode

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Abstract—Envelope tracking (ET) amplifiers are implemented by modulating the DC voltage supply to the drain of a transistor with the objective of improving the device efficiency under power back-off conditions. However, changing the drain voltage also changes the drain-to-source capacitance (C_{ds}) of the device, causing the optimum impedance to shift. This paper investigates the behavior of the current and voltage waveforms at the current generator plane of a High Voltage Laterally Diffused Metal Oxide Semiconductor (HVLDMOS) device in an emulated ET architecture, and the trajectory of the optimum load impedance on the package plane as the drain voltage supply is varied throughout the ET operating range. An example of a class-F mode operating in an ET setting at 900MHz is shown as an example to understand the degradation of the overall drain efficiency, which was analyzed using the waveform engineering approach.

Introduction

With the emergence of small-cell transmitters in 4G network infrastructures, the use of envelope tracking power amplifiers (PA) is getting more popular as it allows for a relatively wider operating bandwidth compared to Doherty power amplifiers. The reduced power requirement in a small cell makes the power consumption of the PA now comparable to the power consumed by other segments of the small cell such as digital pre-distortion (DPD) [1]. The possibility of relaxing the required complexity in DPD implementation using ET as a baseband linearization method as discussed in [2-3] therefore makes the ET architecture even more attractive as the Doherty PA requires a significant amount of pre-distortion.

A class-F PA is characterized by its half-rectified current waveform and a squared voltage waveform, and is realized by presenting a short and an open circuit to the 2nd and 3rd harmonics respectively at the current generator plane while an optimal fundamental load is selected to find a balance between drain efficiency and output power. The half-rectified current waveform reduces the average DC current component and the squared voltage waveform increases the fundamental voltage component, a combination that improves the device drain efficiency. Previous implementations of a standalone class-F PA resulted in a drain efficiency of 78% for a 5W LDMOS device [4] and 74% for a GaN device in [5] where a continuous class-F mode PA was implemented to enable a wide bandwidth of operation.

Integrating a high efficiency mode PA such as a class-F or inverse class-F PA into the ET architecture is a desirable solution to further improve the drain efficiency of the PA in power back-off conditions, as discussed in [6-7]. However the variation of the device's drain-to-source capacitance (C_{ds}) at different

drain voltage supplies (V_{ds}) causes a shift in the required optimum load impedance. This poses a challenge in 'holding' the PA in high efficiency mode throughout the ET operating range, where the V_{ds} is varied according to the input signal envelope but the load presented to the PA remains static. It is therefore appropriate to optimize the high-efficiency mode design at the region of the drain voltage where the amplifier will spend most of its time at, based on the input signal power distribution function. This will result in a relatively higher average efficiency compared to if the PA is optimized at the maximum drain voltage [8].

This paper discusses the approach of using waveform measurements and waveform engineering to analyze the behavior at the current generator plane of the device operating in a class-F mode and the trajectory of the optimum load impedance at the package plane as the drain supply is varied. The objective is to understand the requirements for holding the PA in a high-efficiency mode throughout the ET range. Using active harmonic load pull, a high-voltage laterally diffused metal oxide semiconductor (HVLDMOS) device from Freescale that has a maximum drain voltage of 50V is set to operate in a class-F mode. To emulate an ET environment, the drain bias is varied within a selected range from 16V to 48V, for the purpose of avoiding the knee region and preventing breakdown on the high side.

Measurement Setup & Methodology

The measurements in this paper are performed using a harmonic active load pull system that is capable of controlling up to the third harmonic as shown in Fig. 1. A non-linear vector network analyzer (NVNA) is used as a receiver and an external signal generator with a power amplifier is used to generate the continuous wave (CW) input signal at 900MHz. On the load side 3 signal generators and power amplifiers are used to emulate the reflected waves, enabling load manipulations up to the 3rd harmonic. A load pull automation software is used to control the signals injected from all signal generators, acquire calibrated time-domain waveforms, and to perform data analysis.

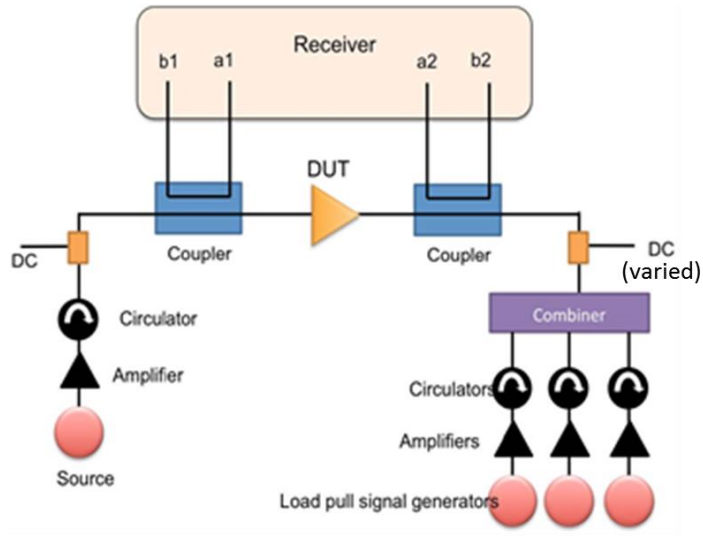

Figure 1: Active load pull system up to the 3rd harmonic

There are four scenario that are investigated to understand the impact of ET to a high-efficiency mode: (a) the ideal case where the class-F mode is maintained at all V_{ds} to obtain the best drain efficiency values, (b) when the class-F mode is optimized for output power at the peak drain voltage within the ET range which is 48V, (c) when the class-F mode is optimized for efficiency at 48V, and (d) when the class-F mode is optimized for efficiency at 28V drain voltage. This 28V drain voltage is selected because it represents the V_{ds} value within the ET range at which the device will spend most of its time when excited with an LTE modulated signal as calculated from [7].

The device is driven into 1 dB compression for each V_{ds} to ensure a valid comparison between different drain settings. This is important since at different compression levels the optimum load impedance will shift, causing an error in the load selection. The fundamental load is chosen to optimize either efficiency or output power while successfully maintaining class-F voltage and current waveforms. The 2^{nd} and 3^{rd} harmonics are terminated with a short and an open circuit, respectively at the current generator plane.

To enable time-domain waveform measurements at the current generator plane at all drain voltages, a dynamic de-embedding is needed to accommodate the variation in C_{ds}. A two-stage de-embedding approach is used to achieve this: (a) a fixed de-embedding of the device manifolds, pad capacitance, and bond wires, and (b) a variable de-embedding stage for the C_{ds} as a function of drain voltage supply. An indication of an accurate de-embedding that was used as a verification method is that the load pull contour of the output power is centered on the real axis on the Smith chart. The de-embedding process is a critical step in the analysis as it enables the optimization of class-F at any given drain voltage, and its accuracy will determine the accuracy of load selections. It also allows for the analysis of the degradation in drain efficiency within the ET range of drain voltages while a static load is set.

Results & Discussions

A. Class-F ET Optimized at Individual Vds (Ideal-Case Scenario)

This scenario provides an insight to the maximum achievable drain efficiency throughout the ET range. The device is optimized for efficiency at V_{ds} values from 16V to 48V in 4V steps. For each V_{ds}, an optimum fundamental load search is performed using a load pull grid while adjusting the drive level such that the device is driven into 1 dB compression at each measured load. Each V_{ds} uses its corresponding de-embedding value to enable the appropriate fundamental and harmonic load selections at the current generator plane. The fundamental load is selected to obtain maximum efficiency, while maintaining class-F voltage and current waveforms.

Fig. 2 shows the trajectory of the loads when translated to the device package plane. The fundamental and 3^{rd} harmonic loads shift in the direction of the arrow as the drain voltage goes up from 16V to 48V, while the 2^{nd} harmonic load stays at the same point, a result of presenting it with a short circuit. The establishment of the of the fundamental load trajectory is dependent on the resolution of the load pull grid during the optimum load search as well as the resolution in power sweep setting during the 1dB compression point search.

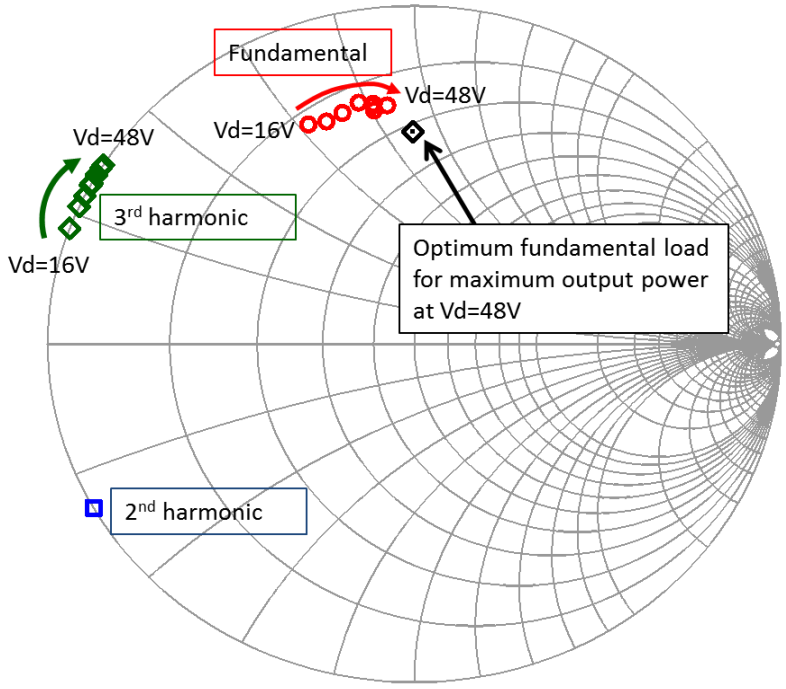

Figure 2: Trajectory of optimum loads for maximum efficiency at different drain voltages, from 16V to 48V. Also shown is the optimum fundamental load for maximum output power at 48V drain voltage.

Fig. 3 shows the time-domain voltage and current waveforms at the current generator plane for each value of V_{ds} in this scenario. The peak efficiency ranges from 71% to almost 74% depending on the output power and drain voltage (Fig. 6).

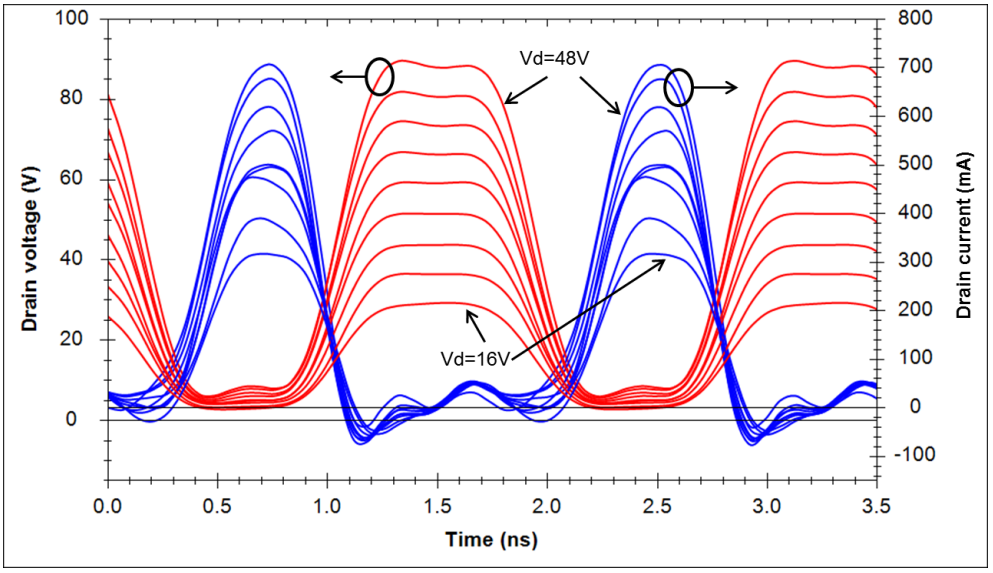

Figure 3: Time domain plots of voltage (red) and current (blue) waveforms when the class-F is optimized for efficiency at each drain voltage, from 16V to 48V in 4V steps.

B. Class-F ET Optimized for Output Power at Vds of 48V

To analyze this scenario, the optimum class-F fundamental and harmonic loads to achieve maximum output power are identified when the drain is set to 48V. Fig. 2 shows the fundamental load impedance has shifted away from the trajectory established from scenario A and does not overlap, necessitating a trade-off between output power at 48V and efficiency at any given drain voltage setting. Using these fixed loads, the device is then characterized as the drain voltage is varied from 48V to 16V in 4V steps while adjusting the drive level to maintain a 1 dB compression level. From Fig. 6 it is observed that the efficiency drops from 74% to about 69% at peak power while the output power is 39.4 dBm.

Fig. 5 shows the voltage and current waveforms for this scenario. At lower drive level and lower V_{ds} values, the device does not see an optimum impedance anymore due to the variation in C_{ds}. This causes further degradation in drain efficiency and at 10dB power back-off, the efficiency drops to 56%.

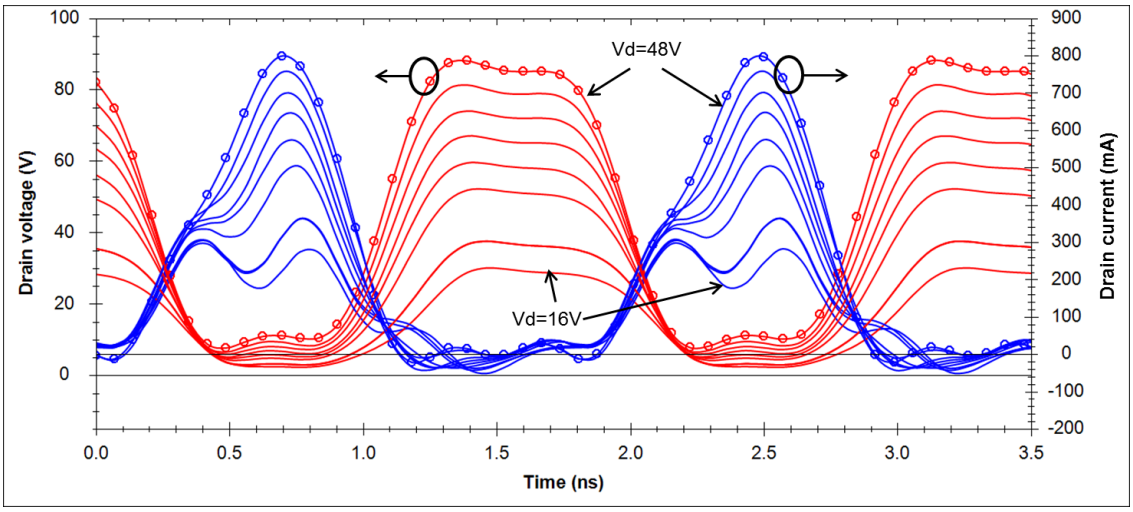

Figure 4: Time domain plots of voltage (red) and current (blue) waveforms when the class-F is optimized for output power at 48V drain bias.

C. Class-F ET Optimized for Efficiency at Vds of 48V

This scenario is similar to scenario B above except that the fundamental impedance is selected to obtain maximum efficiency instead of output power at 48V drain voltage. The maximum output power is 38.7dBm, 0.7dB lower than when the class-F is optimized for output power as in scenario B but the efficiency is 5%-point and 2%-point higher at peak power and at 10dB power back-off, respectively (Fig. 6).

D. Class-F ET Optimized for Efficiency at Vds of 28V

The next analysis looks at optimizing the class-F mode at a drain setting that represents the bias point where the PA will spend most of its time at, based on the LTE signal power distribution. This seems to be the best solution in terms of overall PA efficiency performance where the drain efficiency is maintained above 64%, with a maximum efficiency of 74% (Fig. 6). The current waveforms started to have bifurcations at higher and lower V_{ds} settings, a result of non-optimum impedance terminations.

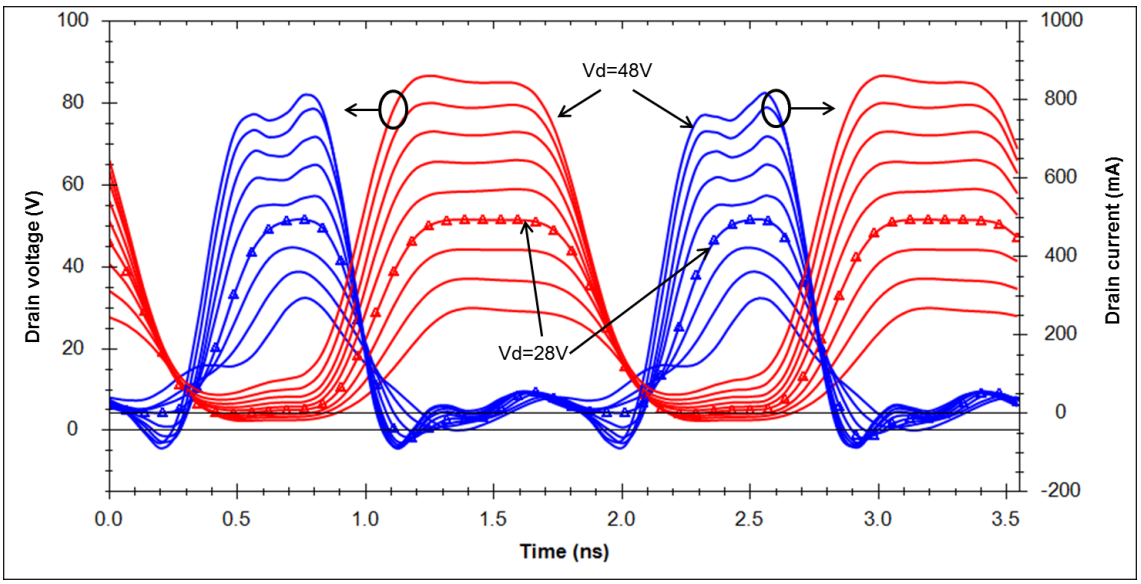

Figure 5: Time domain plots of voltage (red) and current (blue) waveforms when the class-F is optimized for efficiency at 28V drain bias.

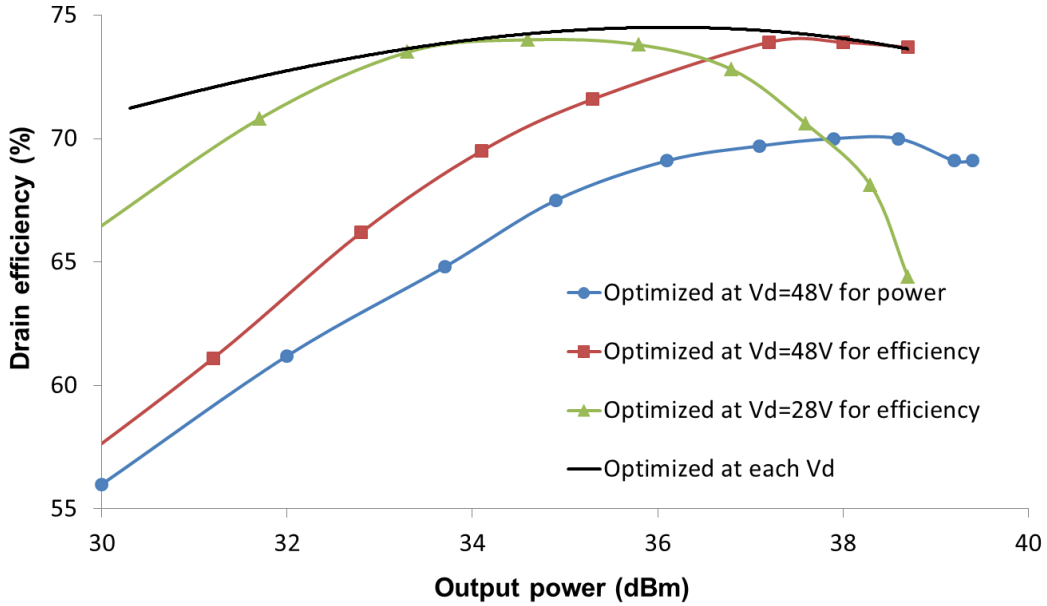

Figure 6: Overall drain efficiency from scenario A, B, C, and D.

Conclusions

An analysis of the device behavior at the current generator plane of a 50V HVLDMOS device has been presented using waveform measurements and waveform engineering approaches. The trajectory of the load impedances at the package-plane in an ET environment is established and provides an understanding of the requirements in maintaining class-F mode in an ET setting, as well as the maximum achievable efficiency. The extent of degradation in drain efficiency because of the variation in C_{ds} is also

discussed. For this HVLDMOS device with an LTE signal input, biasing the class-F at 28V drain voltage achieves the best efficiency performance throughout the entire range of output power.

With the same method and a robust de-embedding model, this analysis can be extended into other device technologies, for example GaN and into other classes of amplifier to provide design considerations for an ET architecture.

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References

[1] M. Lassanen et al, "Environmental friendly radio networks: Approaches of the European OPERA-Net 2 project", 2013 20th International Conference on Telecommunications

[2] Z. Yusoff et al, "Simple and low cost tracking generator design in envelope tracking radio frequency power amplifier system for WCDMA application", Microwaves, Antenna & Propagation, IET Vol. 7, No. 10, 2013, pp. 802-808.

[3] F.L. Ogboi et al, "A LSNA configured to perform baseband engineering for device linearity investigations under modulated excitations", 2013 European Microwave Conference

[4] A. Sheikh et al, "Systematic waveform engineering enabling high efficiency modes of operation in Si LDMOS at both L-band and S-band frequencies", Microwave Symposium Digest, 2008 IEEE MTT-S International.

[5] V. Carrubba, J. Lees, J. Benedikt, P.J. Tasker, and S.C. Cripps, "A novel highly efficient broadband continuous class-F RFPA delivering 74% average efficiency for an octave bandwidth," Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International.

[6] B. Merrick, T.J. Brazil, "Analysis of the integration of envelope tracking with continuous class-F amplifiers," Integrated Nonlinear Microwave and Millimetre-Wave Circuits, 2012 Workshop on.

[7] J.H. Kim et al, "High-efficiency envelope tracking transmitter with optimized class-F^{-1} amplifier and 2-bit envelope amplifier for 3G LTE base station," IEEE Transaction on Microwave Theory and Techniques, Vol. 59, No. 6, June 2011.

[8] B. Kim, J. Moon, I. Kim, "Efficiently amplified", Microwave Magazine, IEEE Vol.11, No. 5, Aug 2010, pp. 87-100