UNDERSTANDING THE 3 LEVEL DOHERTY

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Abstract - The Doherty amplifier is a well known technique for improving efficiency of a power amplifier in a backed off condition. The standard 2 way Doherty amplifier with a peak in efficiency at 6dB back off and full power is commonly used and well understood. With the use of increasingly complex signals comes the requirement to move the peak in efficiency to higher levels of back off whilst maintaining efficiency up to full power output. This can be achieved with asymmetrical Doherty amplifiers or by utilising N-Way Doherty techniques. In this paper we will explain from first principles the operation of the 3 Level Doherty architecture based on an NXP design that uses three LDMOS transistors of equal size. Design challenges faced with this type of amplifier are presented and compared against conventional 3-Way Doherty architecture. Test results are presented which demonstrate a drain efficiency of greater than 40% at 10dB back off

1. Introduction

Modern communication systems routinely use complex modulation techniques that result in peak to average ratio (PAR) signals of 9dB and higher. These types of signals present a difficult efficiency challenge for the output power amplifier. One of the simplest forms of RF amplifier is the class AB type. Such an amplifier is relatively straightforward to design and manufacture and can easily provide peak drain efficiencies of around 65% when operating in the 2GHz region. A problem with this type of simple amplifier is that when the RF output signal level is reduced, the output voltage swing also reduces and efficiency drops away with the square root of the output power. This means that at a quarter of the output power (-6dB), the efficiency drops to around half of the peak, 32% in this example. It is clear to see that operating at 6dB back-off and higher with a class AB amplifier results in a significant reduction in efficiency because the signal is, on average, sitting at a highly inefficient operating point. This is why Doherty amplifiers have seen a strong resurgence in modern W-CDMA and LTE systems.

The 2-Way Doherty provides an improvement over the class AB case, but with higher levels of peak to average ratio being used, it is necessary to improve efficiency at back of levels of 10dB and higher. The 3 standard Level Doherty produces peaks in efficiency at 9.5dB, 4.4dB and 0dB which is a good fit for LTE transmitters, but as we shall see, requires the two auxiliary amplifiers to be twice the periphery of the main amplifier. In this paper, we will describe the operation of a Modified 3 Level Doherty [3] that produces good efficiency over the top 10dB of operation using devices of equal periphery.

2. The 2-Way Doherty

Although well documented in the literature, it is worth spending some time revisiting the simple case of the 2-Way Doherty to help understand the 3-Level configuration.

The standard 2 Way Doherty amplifier works by splitting the amplifier into two equally sized amplifiers of half the size (of a single ended Class AB amp with the same peak power capability). The basic principle is that when the output signal level is low, only the main amplifier is active. With increasing output levels the auxiliary amplifier is progressively introduced up to the point

where full power is achieved where both main and auxiliary are contributing equally to deliver full power.

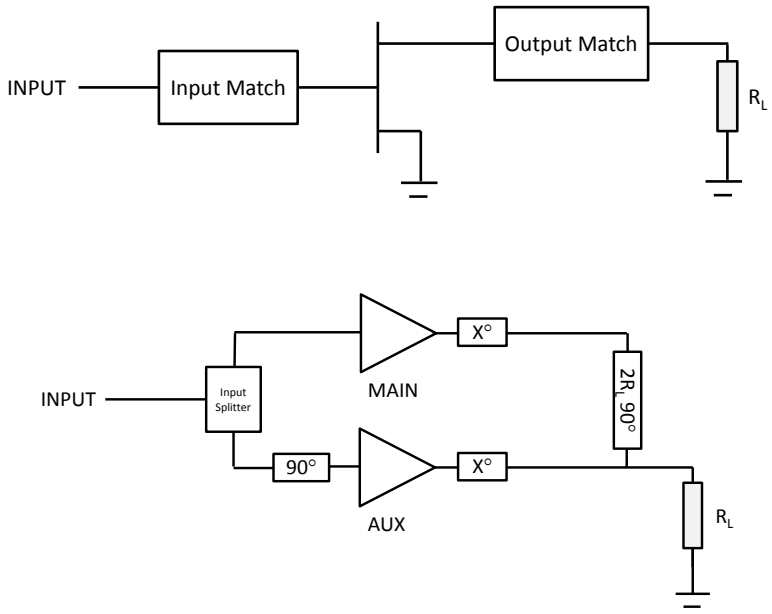

Figure 1: Single Ended Class AB and 2 Way Doherty

The 2 Way circuit is configured with the main amplifier biased in Class AB and the auxiliary amplifier biased in class C. This biasing scheme means that at low input drive levels, the main amplifier conducts and the auxiliary amplifier is off. As input levels are increased, the main amplifier drive level also increases and when the output power is a quarter (-6dB) of the amplifier maximum, the auxiliary amplifier starts to conduct current.

At low signal levels when the auxiliary amplifier is not active, the main amplifier (Assuming R_L = 25 Ω) "sees" 100 Ω. This means that it reaches full voltage swing at half power. Full voltage swing means that the main amplifier provides maximum efficiency at half its output power. At this point, the amplifier as a whole is delivering a quarter (-6dB) of its peak power capability with maximum efficiency. This is the first point on our efficiency curve in Figure 4.

As input drive level is increased from the 6dB back off point, so the current contribution into the load from the auxiliary increases. This increased current being injected means that the impedance looking into the load increases. The 50 Ω impedance inverter between the load and the main amplifier ensures that that main amplifier sees a reducing load as the current contribution from the auxiliary increases. So, in this regime, as output power increases, there are two processes taking place. The first is that, due to the load modulation from the auxiliary, the main amplifier is effectively increasing in size, that is, it's capability to produce power is increasing, but all the time it is running at maximum voltage swing and hence maximum efficiency. The other process that is taking place is that both the main and auxiliary amplifier are contributing to the total output power. As drive level increases, so these processes continue up until the auxiliary is at maximum output power (if devices are equal in size) and the currents into the load from the main and auxiliary are equal. At this point the main and auxiliary amplifiers both see 50 Ω.

The key concept to understand in the operation of the Doherty is load modulation. The explanation given in [1] provides an excellent description of the principals involved and the key elements are repeated here for clarity.

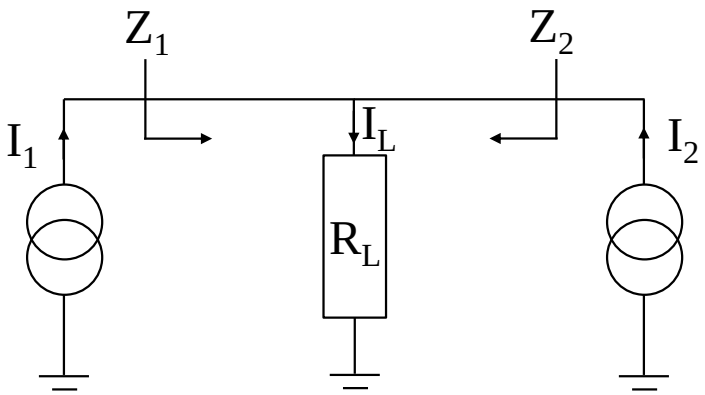

Figure 2: Load Modulation (Inverter Removed)

Figure 2 represents the simplest possible case where two current sources are feeding into a common load. When $I_2 = 0$, then the impedance Z_1 is simply equal to R_L. If a current is injected into the load from I_A then the impedance Z_1 is modified to:

$$Z_1 = \left(1 + \frac{I_2}{I_1}\right) R_L$$

Equation 1

If I_1 and I_2 are equal, then then $Z_1 = Z_2 = 2R_L$. With the addition of an impedance inverter as shown in Figure 3, this circuit becomes the 2 Way Doherty. The addition of the inverter causes the impedance seen at the main amplifier, Z_m, to reduce when the current from the auxiliary is injected into the common load. When the auxiliary is off then $Z_m = Z_0^2 / R_L$

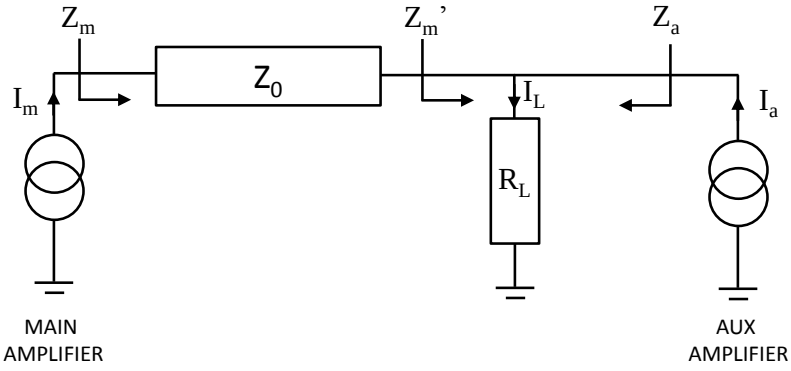

Figure 3: 2 Way Doherty Schematic

The theoretical efficiency curve for a 2 Way Doherty is shown below in Figure 4.

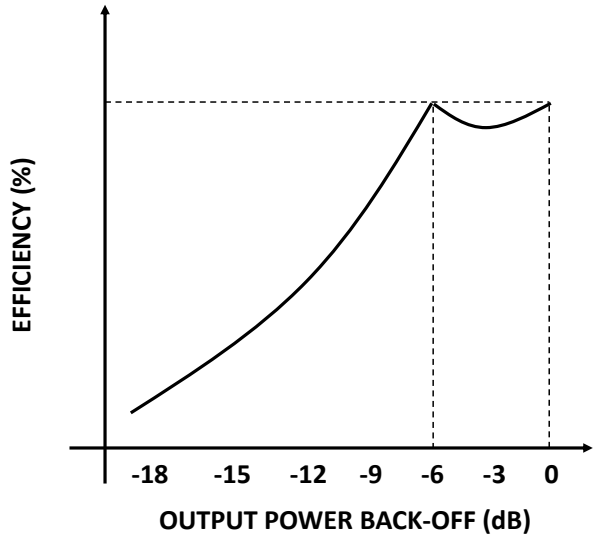

Figure 4: 2 Way Doherty Theoretical Efficiency Curve

3. The Conventional 3 Level Doherty

The conventional 3-Level Doherty is a direct extension of the 2 Way design and is shown in Figure 5.

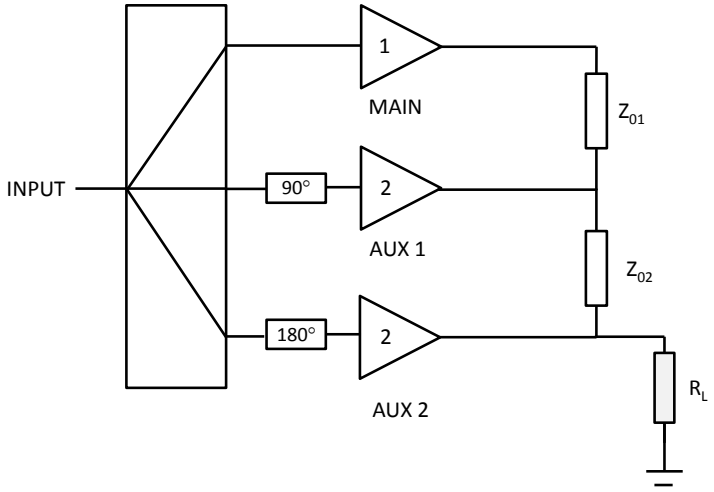

Figure 5: Conventional 3 Level Doherty

By adjusting the relative device periphery between the main and auxiliary amplifiers, it is possible to achieve a variety of different positions for the efficiency peaks. The designer can use the equations defined in [2] to locate the efficiency peaks as required. In this paper, we are concerned with signals with around 10dB of PAR. The relative levels of device periphery to achieve an efficiency peak at -9.5dB, -4.4dB and 0dB for the conventional 3 Level Doherty is 1:2:2 where the first digit is the main amplifier followed by Aux 1 and Aux 2 i.e M:A1:A2.

For this configuration, Z_{01} is required to be 70.7 Ω, Z_{02} = 33.3 Ω and R_L = 20 Ω. At the first efficiency peak the main amplifier will see an impedance of 90 Ω. In order to match the output to 50 Ω an impedance inverter of value $\sqrt{20.50}$ = 31.6 Ω is required.

In essence, the conventional 3 Level Doherty behaves as a 2 Way Doherty up to the second peak (-4.4dB) in efficiency and then from the second peak to full power the main and auxiliary 1 amplifiers are behaving like a main amplifier which is being load modulated by the current contribution from auxiliary 3.

However, there are two main drawbacks of the conventional 3 level Doherty. The first is that different device sizes are required to provide efficiency peaks in the 10dB back off region, which leads to added complexity. The second is that the load modulation of the main amplifier stops in-between the second and final efficiency peaks. This means that the main amplifier is driven into extreme saturation over the last 6dB of output power [3].

4. Modified 3 Level Doherty With Equal Sized Devices

The modified 3 Level Doherty design from NXP [3] achieves similar performance to a conventional 3 Level Doherty but without having to accommodate output transistors of different sizes. Using transistors of equal sizes for the main and auxiliary stages has a number of practical benefits, including the use of a single "unit cell" RF design. The basic amplifier unit cell for the main and auxiliaries can be of the same (or very similar) design which reduces development time. Also, having three of the same parts rather than two different parts on the bill of materials leads to economies of scale, which is important for what are likely to be the most expensive components in the amplifier. The configuration also leads to proper load modulation of the main amplifier whose load impedance, as we shall see, steadily reduces as drive level is increased.

A schematic diagram of the modified 3 level Doherty is shown in Figure 6.

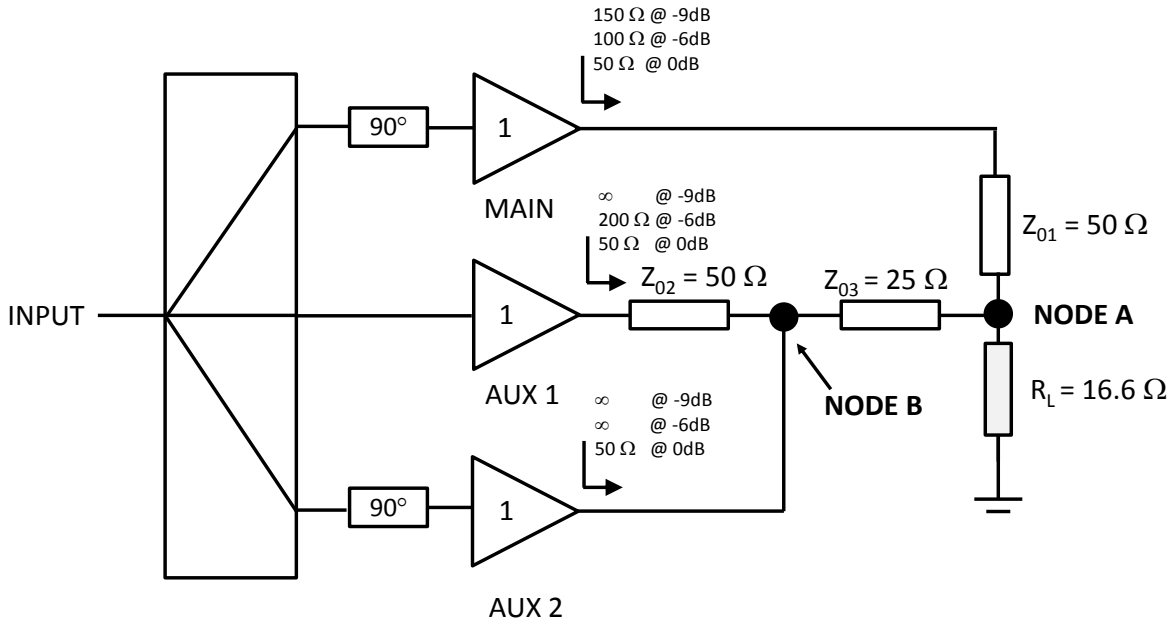

Figure 6: Modified 3 Level Doherty Schematic

The best way to understand the operation is to start at low signal levels and progressively increase the input drive level and discuss the operation at each efficiency peak and refer to the efficiency curve in Figure 7.

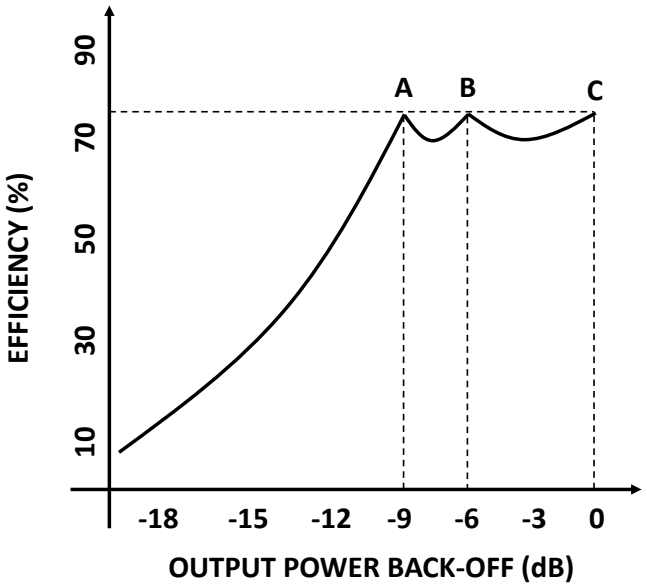

Figure 7: Theoretical Efficiency Curve For Modified 3 Level Doherty

Each amplifier depicted as a triangle in Figure 6 is termed a "unit cell". Each unit cell in this example delivers maximum output power when driving a 50 Ω load. The unit cell also contains phase offset lines to ensure that the electrical length of an auxiliary (and main) stage is 180 degrees from the active device to the point at which the amplifier is connected into the Doherty combiner circuit. This ensures that when the auxiliary amplifier is switched off an open circuit is presented to the Doherty combiner and the minimum power is dissipated in the auxiliary output matching circuits. The main amplifier is biased in a class AB mode, Auxiliary 1 is biased at around 0.7V and Auxiliary 2 is biased at around 0V when using enhancement mode LDMOS transistors. These values provide the required progressive switching of the Auxiliary amplifiers. Note, that the load value is 16.66 Ω in this example, this is transformed up to 50 Ω with a 28.8 Ω quarter wave inverter.

At low signal levels, in the regime before point A is reached, only the main amplifier is active. The impedance presented to the main amplifier unit cell at this point is 150 Ω.

At point A the following conditions apply:

Stage	**Impedance Presented to Unit Cell**	**Power Delivered into Output Load.**
Main	150 Ω	33% of $P_{MaxMain}$
Aux 1	∞	0
Aux 2	∞	0
Total Power in Load		11% of P_{Total}
Power Delivered/Total Power Capability (Back Off Level in dB)		10Log(0.33/3) = -9.6dB

Table 1: First Efficiency Peak Parameters

As the input drive level increases, so we move to the region in between point A and B in Figure 7. At point A, Auxiliary 1 switches on and starts to deliver current into the common output load

R_L. This increase in current in the common load causes the impedance seen from the main amplifier at Node A to increase. The action of the inverter $Z_{01,}$ in the main path, causes the impedance seen by the main amplifier to fall. This reduction in output impedance results in the main amplifier being able to deliver more power into the common load whilst remaining in voltage saturation.

As drive level is increased, so this process continues until the current in the load due to the auxiliary is half that of the current in the load due to the main and the following condition is reached:

$$\frac{I_{A1}}{I_M} = 0.5$$

Equation 2

This condition is point B in Figure 7 and is our second efficiency peak. At this point, applying Equation 1, the impedance seen from the main amplifier looking into Node A is given by :

$$Z_{M\_NodeA} = R_L\left(1 + \frac{I_{A1}}{I_M}\right) = \frac{3}{2}R_L = 25\Omega$$

Equation 3

So, the impedance seen by the main device looking into 50 Ω inverter Z_{01} is 100 Ω.

Also, the impedance seen from the Auxiliary branch looking into Node A is given by:

$$Z_{A\_NodeA} = R_L\left(1 + \frac{I_M}{I_{A1}}\right) = 3R_L = 50\Omega$$

The impedance at node B looking from Auxiliary2 is therefore 12.5 Ω (due to Z_{03}) and the impedance seen by Auxiliary 1 unit cell amplifier is 200 Ω. Since the main amplifier and auxiliary 1 are both running at voltage saturation, they both deliver maximum efficiency, hence the peak in efficiency. The parameters for the amplifier at this second efficiency peak are given below.

Stage	**Impedance Presented to Unit Cell**	**Power Delivered into Output Load**
Main	100 Ω	50% of $P_{MaxMain}$
Aux 1	200 Ω	25% of $P_{MaxAUX1}$
Aux 2	∞	0
Total Power in Load (Max = 3)		25% of P_{Total}
Power Delivered/Total Power Capability (Back Off Level in dB)		10Log(0.75/3) = -6.0 dB

Table 2: Second Efficiency Peak Parameters

The bias of Auxiliary 2 is set such that it starts to turn on and deliver current into the output load when Equation 2 is satisfied. The increase in current further reduces the main impedance and allows it to deliver more power. The increased current into the load also reduces the load impedance seen by Auxiliary 1 so this device delivers more power and further increases load current. This increase in current continues until the contribution from each amplifier is equal and the following is satisfied:

$$I_M = I_{A1} = I_{A2}$$

Equation 4

The two auxiliaries deliver a total normalized current of 2 into the load and the main delivers 1. This is point C in Figure 7. At this point, the impedance from the main branch looking into Node A is now

$$Z_{M\_NodeA} = R_L\left(1 + \frac{I_{A1+IA2}}{I_M}\right) = 3R_L = 50\Omega$$

So the main amplifier sees 50Ω and delivers full power. The impedance seen from the auxiliary branch looking into Node A is given by

$$Z_{A\_NodeA} = R_L\left(1 + \frac{I_M}{I_{A1} + I_{A2}}\right) = \frac{3}{2}R_L = 25\Omega$$

Since Z_{03} is a 25Ω inverter, so the impedance looking into Node B is also 25Ω. This is the correct impedance for two 50Ω loads in parallel. The parameters for the amplifier at this third and final efficiency peak are given below.

Stage	Impedance Presented to Unit Cell	Power Delivered into Output Load
Main	50 Ω	100% of $P_{MaxMain}$
Aux 1	50 Ω	100% of $P_{MaxAUX1}$
Aux 2	50 Ω	100% of $P_{MaxAUX2}$
Total Power in Load (Max = 3)		100% of P_{Total}
Power Delivered/Total Power Capability (Back Off Level in dB)		10Log(1) = 0 dB

Table 3: Third Efficiency Peak Parameters

As well as the design of the output network, there are a number of practical design considerations of this type of amplifier that need to be considered. The first is that the gain of the 3 Level amplifier is inherently quite low because of the 3 way input split. This results in the small signal gain being a minimum of 4.7dB lower than that obtained from a single ended device. This is less of an issue at lower cellular bands, but can become a problem at higher frequencies where gain is at a premium. The quarter wave transformers used extensively in this design, limit the bandwidth to around 4 to 5% maximum, so is only currently applicable to narrow band applications

5. A 2.14 GHz 3 Level Doherty

In order to demonstrate the concept a 2.14 GHz version of the NXP 3 Level amplifier was designed and manufactured. A photograph of the amplifier is shown below in Figure 8.

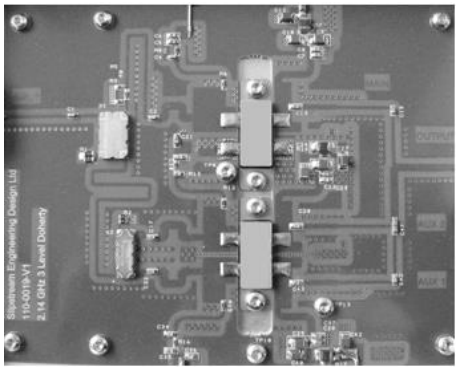

Figure 8: 2.14GHz 3 Level Doherty

The 3 way input splitting (-4.7dB) is achieved by using a 5dB directional coupler cascaded with a 3dB hybrid coupler. The transistors used are twin LDMOS devices running from 28V (normally used for push pull or balanced applications) with one of the transistors not used in the upper device. The output power of this amplifier cannot be published here, so the results are presented as back off levels from full output power, which in this case is classed as around 2dB output compression. As can be seen, the design objective of 40% drain efficiency at 10dB back off has been achieved over the band of interest. Although not shown here, the small signal gain of this amplifier was around 16dB with a power gain at full power of 14dB.

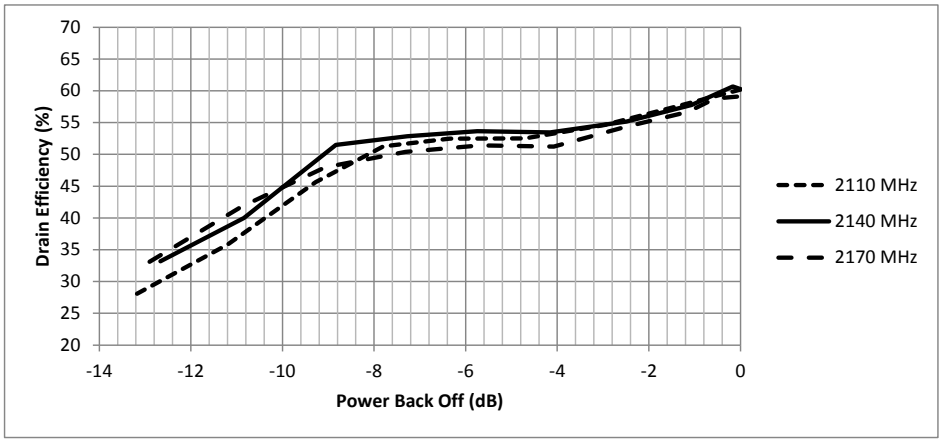

Figure 9: Experimental Results For a 2.14GHz 3 Level Doherty Amplifier

6. Summary

An overview and explanation of the operating principle of the Modified 3 Level Doherty form NXP has been presented with experimental results of a fabricated amplifier shown.

7. References

[1] RF Power Amplifiers for Wireless Communications – Steve C. Cripps, Artech House, 1999

[2] A Mixed-Signal Approach Towards Linear and Efficient N-Way Doherty Amplifiers W. C. Edmund Neo et al, IEEE-MTT VOL. 55, NO. 5, MAY 2007

[3] 3 Way Doherty Amplifier With Minimum Output Network, US Patent US20100315162, NXP