A NOVEL BROADBAND IQ MODULATOR / DEMODULATOR MMIC

John Birkbeck, Julian Trinder
Roke Manor Research Limited, Old Salisbury Lane,
Romsey, Hampshire, SO51 0ZN. UK
john.birkbeck@roke.co.uk

ABSTRACT
Commercially available broadband microwave IQ Modulator / Demodulator modules typically cover an instantaneous bandwidth of up to 2-octaves, for example 1GHz to 4GHz. Such modules are usually based on passive printed structures with diodes for the mixing function. Bandwidth is generally limited by the ability to maintain accurate 90° phasing in the local oscillator feed, due to practicalities of the means generated, for example in a multi-stage branch line coupler. A prototype MMIC based IQ Modulator / Demodulator will be described which uses a novel but conceptually simple technique to maintain 90° phasing over a broader bandwidth. Whilst this first implementation of the technique targets a bandwidth of 1-6GHz, the underlying method is inherently broadband in nature, and could be applied to Silicon RFICs as well as GaAs MMICs.

MOTIVATION
It was identified that a broadband IQ Modulator / Demodulator module realised using European technology, would be an attractive component for future system designs for Space Applications. Lower and upper operating frequencies of 1.2GHz and 5.4GHz respectively were cited for a particular satellite based SAR (Synthetic Aperture Radar) application [1], which drove the target bandwidth for this first prototype to be 1GHz to 6GHz. Realising this bandwidth using conventional distributed techniques would be difficult, and would certainly not be suitable for any subsequent extended bandwidths. It was therefore considered most appropriate to prototype this new patent pending technique as the best forward-looking method available. This approach was also well aligned with the research interests of the sponsor.

PERFORMANCE TARGETS
Fig. 1 below shows a block level view of a typical IQ Modulator / Demodulator module. Three key components can be identified – the 90° LO (local oscillator) splitter, the mixer core, and the 0° combiner.

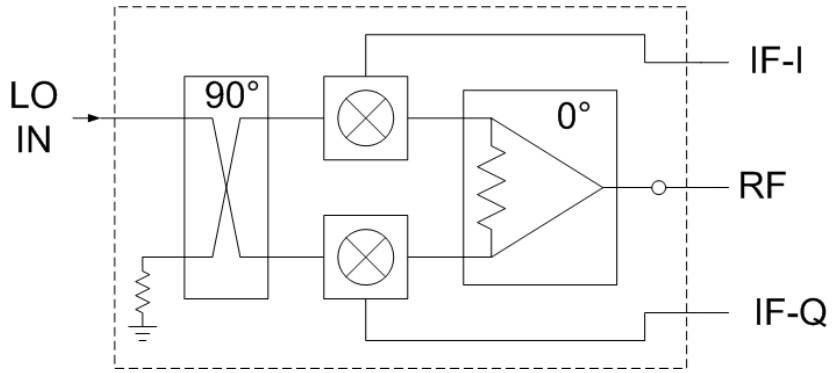

Fig. 1: IQ Modulator - Generic Diagram

The target performance for the Modulator case is shown in Table 1 below. The overall operating bandwidth has already been discussed. The I/Q bandwidth target is an extension of the 10MHz to 320MHz expected operating range. It can be seen that the LO drive levels are typical of that which would be required to drive diode based mixers. For an active MMIC approach a much lesser LO drive level is required, at the expense of DC current. It is the intention in the long term that the need to supply DC power to the device is acceptable in system design, given the benefits of larger operating bandwidth, and reduced LO drive requirements. The port return loss and conversion loss figures are typical nominal requirements. Carrier suppression and sideband suppression are key requirements however, and system performance is strongly linked to these key figures of merit.

Table 1: Target Performance - Modulator

Parameter	**Target**
LO & RF frequency	1.0 to 6.0 GHz
I/Q bandwidth	LF to 500MHz
I/Q drive levels	+0dBm (at 1dB compression)
LO drive level	+10 to +16dBm
Port return loss	10dB
Conversion loss	7-10dB
DC Power Requirements	to be minimised
Carrier suppression	-30dBc (min)
Sideband suppression	-30dBc (typ), -27dBc (min)

The Demodulator requirements of Table 2 are essentially the same as those of the Modulator, although the key figures of merit here are written as quadrature phase and amplitude accuracy.

Table 2: Target Performance – Demodulator

Parameter	**Target**
LO & RF frequency	1.0 to 6.0 GHz
I/Q bandwidth	LF to 500MHz
I/Q drive levels	+0dBm (at 1dB compression)
LO drive level	+10 to +16dBm
Port return loss	10dB
Conversion loss	7-10dB
DC Power Requirements	to be minimised
Carrier suppression	-30dBc (min)
Quadrature Phase Accuracy	±5° (max)
Quadrature Amplitude Accuracy	±0.5dB

THE 90° PHASING METHOD

The theoretical core of the method used to generate accurate 90° LO feed over a broad bandwidth is based on a signal summation using the following well known trigonometric identities:

$$\sin(A)+\sin(B)=2.\cos(½(A-B)).\sin(½(A+B)) \quad (1)$$

$$\sin(A)-\sin(B)=2.\sin(½(A-B)).\cos(½(A+B)) \quad (2)$$

Explaining the method in the simplest form, we begin by defining the LO input reference signal to the system as:

$$\sin(\omega t) \quad (3)$$

from this an inverse signal is generated:

$$-\sin(\omega t) \quad (4)$$

together with a variable phase signal:

$$\sin(\omega t+2\theta). \quad (5)$$

These three signals are then summed in two paths as follows:

$$\sin(\omega t+2\theta)+\sin(\omega t)=2.\cos(\theta).\sin(\omega t+\theta) \quad (6)$$

$$\sin(\omega t+2\theta)-\sin(\omega t)=2.\sin(\theta).\cos(\omega t+\theta) \quad (7)$$

The right hand side of the last two equations (6) & (7) can be considered as an amplitude term, multiplied by a carrier term. If the amplitude terms are detected, they can be compared, and an error signal derived to vary θ in a closed loop manner until they are identical. For the case where the amplitudes are identical we can write:

$$2.\cos(\theta)=2.\sin(\theta) \quad (8)$$

We see that this is only true when θ is 45°, 225° etc (or $\pi/4$ radians, $5\pi/4$ radians, etc). Applying these two repeating values to the right hand side of the full equations (6) & (7) always yields:

$$\sqrt{2}.\sin\left(\omega t+\frac{\pi}{4}\right) \quad \& \quad \sqrt{2}.\cos\left(\omega t+\frac{\pi}{4}\right) \quad (9), (10)$$

It can be seen that equations (9) & (10) represent two signals which are in perfect amplitude balance and perfect quadrature, by virtue of their sine/cosine relationship. In summary, the method produces combined 'gain and phase' error signals, without actually 'measuring' either explicitly, and uses these to simultaneously correct for quadrature imperfection. In practice, a 'differential signal' implementation is preferred, but the underlying method is the same.

Further details on this method are currently in press [3].

SYSTEM ARCHITECTURE

Top Level RF System Architecture

Fig. 2 below shows the key elements of the overall MMIC based system architecture. A single MMIC is used to implement the 90° phasing for the LO. This MMIC also contains the mixer cores, which uses balanced signals on the LO and IF ports, and a single ended signal on the RF port. Off-chip at PCB level, a balun and low pass filter (LPF) is used on the low frequency IF ports to provide the single ended to differential conversion from/to the mixer, and to block RF signals. On the RF ports, a high pass filter (HPF) is used to block IF signals, and a 0° combiner is used to combine/split the RF signal. The RF port is balanced with respect to the LO port, to ensure inherently good rejection of LO signals.

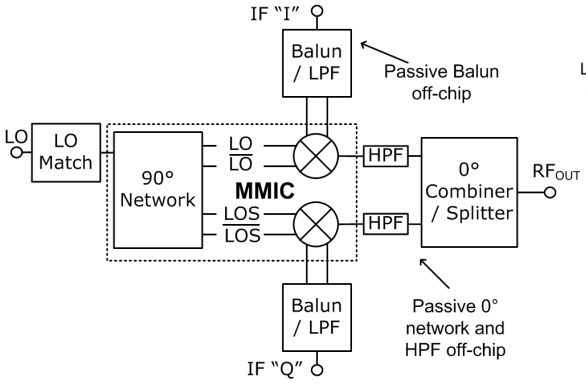

Fig. 2: System Block Diagram

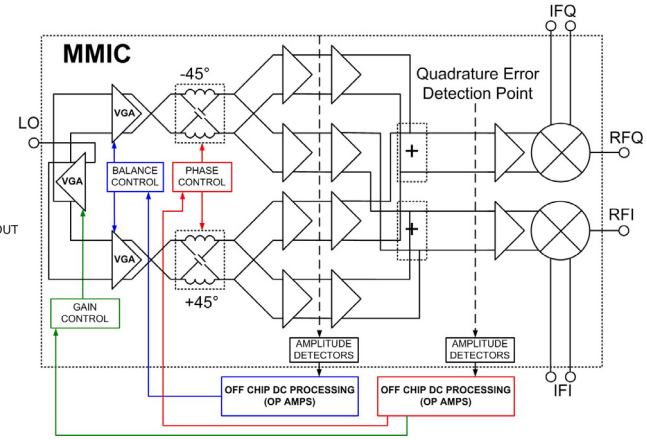

Fig. 3: MMIC Architecture

MMIC Architecture

The MMIC architecture is shown in Fig. 3 above. The practical implementation of the method is a "differential signal" based extension of the simple mathematical analysis presented above, but with the same underlying novel control concept. To provide phase shift and phase control a pair of differential lattice filters [2] are used on-chip, which are designed for -45° and +45° nominal phase shift, but are also voltage tuneable. At the outputs of the filters, a pair of differential signals will result with a controllable phase difference centred on 90°. In addition to the phase control requirement from the mathematical analysis presented earlier, additional amplitude control is required to remove the effects of circuit imperfections, and maximise dynamic range of the circuit. Hence there are three control loops in total, the first two allow for automated control of absolute amplitude level, and amplitude balance in the two paths. When these quantities have settled, the main control loop for quadrature accuracy (as per mathematical analysis) will complete the process. Signal level detectors placed on the signal planes as shown can be used to generate the error signals required for control feedback. Those at the point labelled "quadrature error detection point" are used to control the lattice filters. These represent the relative levels of the combined signals, and when they are equal the necessary conditions of equation (8) will be fulfilled, and 90° quadrature LO drive signals will be achieved. Overall, the 90° LO generation architecture as implemented can be considered as a passive 90° network, but with a novel control loop method wrapped around to provide consistent performance over the greatest bandwidth, plus additional minor loops to compensate for circuit imperfection.

PRACTICAL IMPLEMENTATION

Due to the relative complexity of the MMIC proposed, all functional elements were verified in a preliminary foundry run of "test cells". The final MMIC contained all elements of Fig. 3. DC processing of error signals was performed off-chip. The "test cell" run actually contained cells for on-chip processing of DC error signal, but these could not be used in the final design due to space constraints on the fixed multi-project die size. From an operating frequency perspective too, the very dense layout is undesirable, since it limits achievable performance to some degree. Shown to the left in Fig. 4 is a photograph of the MMIC which measures 3mm * 2mm and was realised on the ED02AH pHEMT process from OMMIC. The centre photograph shows the MMIC bonded into a custom LCP package from Labtech Microwave. The right hand photograph shows the evaluation PCB. It is mentioned here that the apparently considerable off-chip circuitry is mostly required for analysis purposes, and that an application board just to 'use' the device is considerably smaller and simpler (Fig. 9).

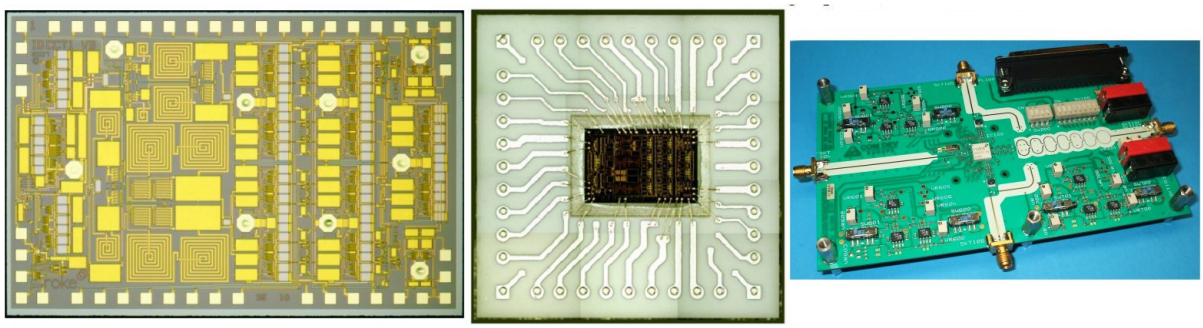

Fig. 4: MMIC, Package & Test PCB

RESULTS

Modulator performance is shown in Fig. 5 below for a 0dBm CW excitation of the IF port. Upper or Lower sideband is selected by varying the relative phase of the IFQ port with respect to the IFI port. Conversion loss is around 10dB, carrier rejection (centre of plots) is around -40dBc and unwanted sideband rejection is around -30dBc.

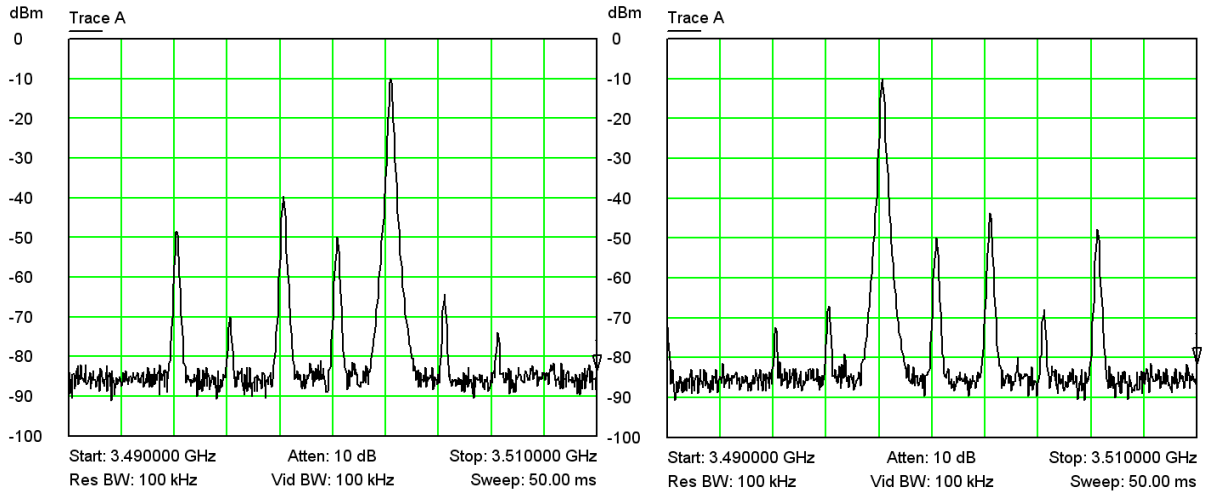

Fig. 5: Mid-band IQ Modulator Performance "closed loop" (USB & LSB operation)

The broadband plots of Fig. 6 show good performance to 4.5GHz in both unwanted sideband and carrier rejection, and the response shape is effectively independent of chosen sideband.

Good rejection of the unwanted sideband over the 1GHz to 4.5GHz region is limited to 30-40dB, due to part of the circuit being realised "off-chip" where electrical symmetry is less well controlled. Degrading performance above 4.5GHz is due to a combination of reducing LO drive levels, and a high pass filter resonance on the RF port. Reduced LO drive levels also explain the reduced rejection of the unwanted sideband at high frequencies, since detected DC input signals to the control circuits are lower, and DC offsets in these circuits become more significant, and limit achievable performance. The glitch in parameters which occurs around 5.5GHz is due to a sharp resonance in the IF feed network which compromises its ability to act as a broadband RF block. This resonance could not be moved out of band with standard component changes.

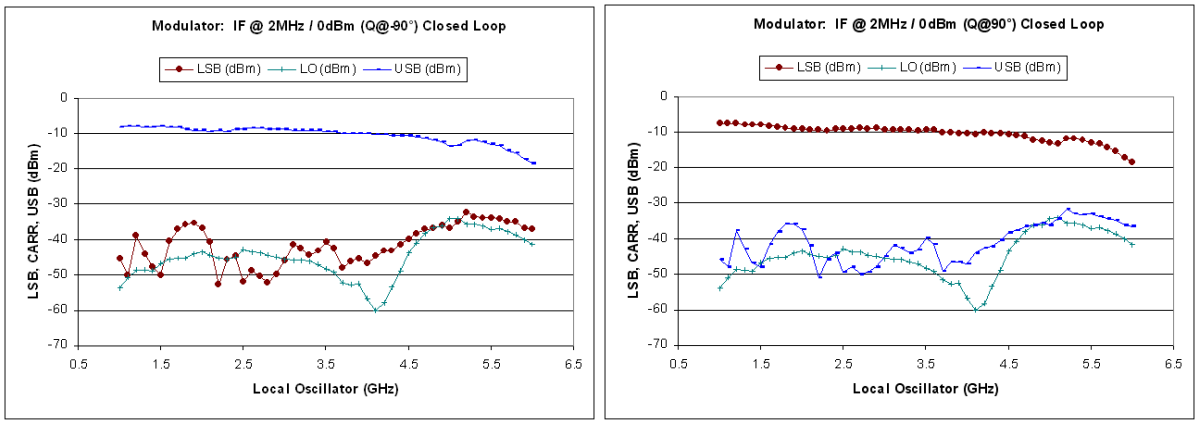

Fig. 6: Broadband IQ Modulator Performance "closed loop"

Whilst this first prototype does not include any temperature compensation, Fig. 7 below demonstrates good natural performance over temperature.

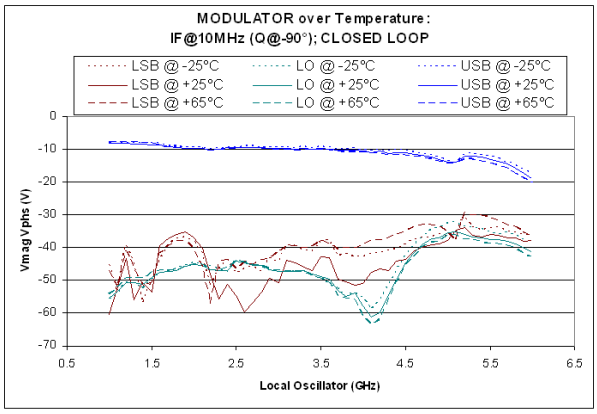

Fig. 7: Broadband IQ Modulator Performance "closed loop"
– over temperature

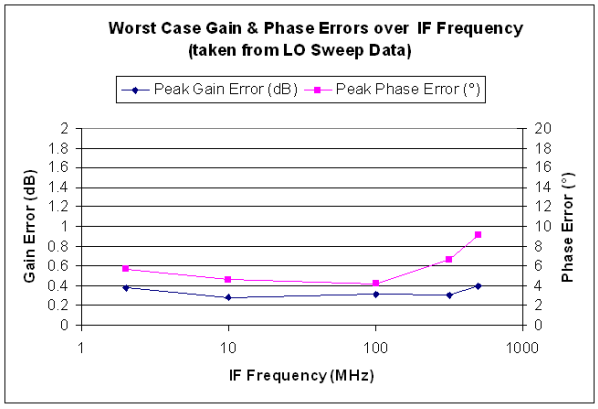

Fig. 8: Broadband IQ De- Modulator Performance "closed loop"

Fig. 8 above shows the "worst case" errors when the device is used as a demodulator. Over a wide IF range performance is good, and mostly limited by off-chip component bandwidth.

FUTURE EXPLOITATION TO PRODUCT

This first demonstrator in its current form satisfied the programme requirements very well, and indeed could be used 'as is' for some applications. An 'artists impression' of an application board to 'use' the current MMIC is shown in Fig. 9 below. Here, all the diagnostic circuitry present in Fig. 4 has been stripped out, and all that remains is the MMIC, the three control circuits, and the LO/IF/RF feed networks.

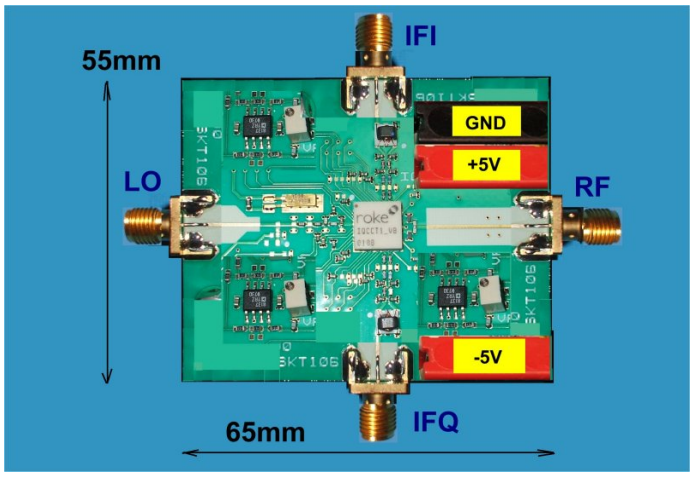

Fig. 9: Artists Impression: Application PCB for current design

However, use of the current prototype as a product would only be likely if "European Technology" or "Technology suitable for Space" was specified, or if ITAR issues were foreseen. This is due to the recent availability of new commercial SiGe products from US suppliers which cover the band of interest for most typical applications albeit generally as just a modulator or demodulator rather than being bi-directional.

To fulfil a 'product' role, further development is required to tailor performance for specific application. Examples include:

- A second manufacture run of the current design
  - Performance shortfalls corrected
  - DC control circuits integrated on-chip
- A product with extended operating bandwidth (eg 500MHz to 20GHz)
- A product operating at higher frequencies eg >>20GHz.

Of course, many specifications in-between can be considered, and constraining the functionality to just a modulator or demodulator opens up further opportunities in terms of size & performance potential.

As a demonstration of bandwidth potential, Fig. 10 below shows measurements over an extended range. The nominal 1GHz - 6GHz chosen band limit is evident, but what is useful to note is the underlying broadband behaviour. At higher frequencies, conversion loss degradation is caused by reduced mixer drive, but nevertheless well behaved suppression of the unwanted sideband is clear to 15GHz or so. This demonstrates the broadband potential of the 'on-chip' LO generation scheme. The reduced amount of suppression is caused by DC offsets in the control circuits dominating loop performance in low signal level conditions.

With band-limiting features removed, and mixer drive power increased, a 500MHz - 20GHz component (for example) would be feasible.

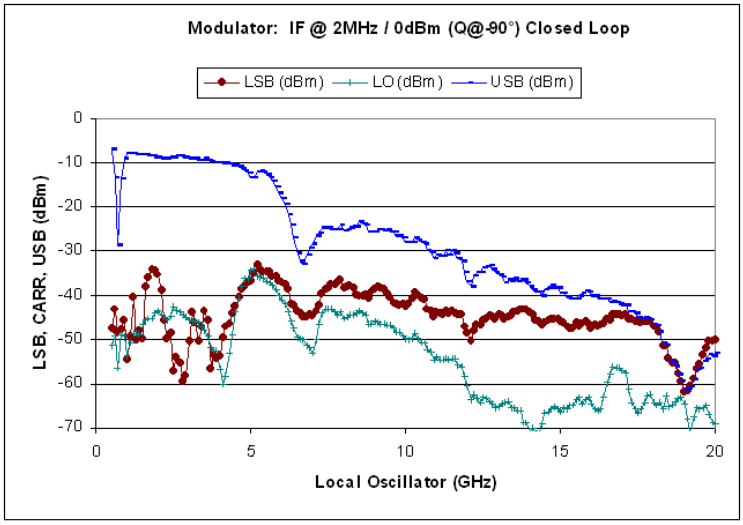

Fig. 10: Extended Bandwidth "USB" IQ Modulator Performance "closed loop"
- showing sensible behaviour to high frequencies, albeit at reduced performance.

CONCLUSIONS

An IQ Modulator / Demodulator MMIC has been presented, which uses a novel patent pending method to maintain performance over a broad bandwidth. Measured results are very good for a 'first pass' design, and show solid performance over temperature. Shortfalls identified can be mitigated in future designs where the die size constraint is removed, and additional circuitry can be included on-chip. The technique looks attractive for future use in much extended bandwidths eg 500MHz to 20GHz, or higher operating frequencies. This technique can find application on Silicon RFIC as well as GaAs MMIC technology, where high levels of integration with A/D converters etc may be attractive.

REFERENCES

[1] Tom McConnell, "Spaceborne Multi-band Synthetic Aperture RADAR", ARMMS Conference, April 2007.

[2] S.D.Bedrosian, "Normalised Design of 90° Phase-Difference Networks," IRE Transactions on Circuit Theory, June 1960.

[3] J. D. Birkbeck, J. R. Trinder, "Multi-octave Microwave Quadrature Signal Generation without Frequency Dividers", EuMW Conference 2008, in press.

ACKNOWLEDGEMENT

Roke Manor Research Ltd. wishes to acknowledge and thank COMDEV Europe Ltd for selecting us as their IC development partner for the IQ Modulator / Demodulator component in their research programme.

Roke Manor Research Ltd. further wishes to acknowledge the European Space Agency for research funding support of this programme.