On wafer and package test with an industrial solution for MMIC components

Jean-Francois Provost, Vincent Pierson, Abdelaziz Tadermet

United Monolithic Semiconductors-Backend

Abstract

Test approaches have changed over the last years led by the high volume market, the complexity and the diversity of the functions (bare dies and packages) to be tested in a production environment.

Both Software and Hardware developments have been required.

Among these works, three examples are illustrated in this paper:

- Development of pulsed power test bench: combination of new equipment generation and powerful test software. Our approach is based on parallelization of multi parameter measurements, capture simultaneously power sweep and pulsed current (very fast test time). These test benches are used for high power circuits designed on GaAs and GaN technologies
- Development of E-band test benches for on wafer test (LNA, Multiplier, PA, IQ up and down converters)
- Development of software tools for data analysis and decision making (setup validation, monitoring in real time...)

The advance test solution integrates different measurement types: DC, noise, [S] parameters up to 110GHz, power measurements and conversion gain up to 86GHz.

The benefits are a higher flexibility, an easy and fast data access, test time reduction and wide test offers at high frequency.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

1. Introduction

Backend production has developed an expertise on wafer test for 30 years and test package.

- 17 Automatic on-wafer microwave test benches (up to 110 GHz)
  - 100 % Functional test strategy ([S], Power, Noise …) - Wafer mapping
  - >17 Millions chips tested per year
- 4 full automatic handlers for high volume package and 3 semi automatic handlers for medium volume package
  - >22 Millions QFN tested per year

2. Pulsed power test bench 50Ghz

2.1. Standard pulsed power test bench

The characterizations of input/output response and 1dB compression on high power amplifier require a pulsed power test bench.

For years, a classic test bench has been used. It is built around a microwave source, amplifier and peak power meter. At these high powers, biasing is pulsed and RF can be pulsed too. Input signal is sweeping across a frequency (or input power) ramp. This ramp is repeated at different input power (or frequency) values.

Oscilloscopes are used to measure consumptions at each of these frequency/power points. Then calculations of Gain, Dissipated power, PAE, … are deducted.

All these measurements and calculations are controlled by test software and are completely automatic. At the end of this 2D characterization (response from both frequency and input power sweeps), data are automatically transferred to a database and can be analyzed with Tools developed at UMS

However, this kind of test bench has limitations, particularly in regard of test times. Indeed, a set of measurement (output power and consumptions) at one frequency/input power point needs 1.5 sec to be performed. More and more demands request for high characterization data, for instance 100 frequency points at 10 different input powers (1000 points to measure) leading to about 1500 seconds to test a die. As example, the test time for 4 inch wafer with 200 HPA, takes 83 hours.

2.2. High speed pulsed power test bench 50Ghz

2.2.1. Take the advantage of the sweeping speed of VNA

A Vector Network Analyzer (VNA) is traditionally used to perform S-Parameter measurements. VNA is able to sweep across a frequency (or power) table, to synthesize very quickly signals and to make fast measurements. 101 measured points can be performed in a few ms!

VNA is a flexible system. Whether on the input or output chain: different elements can be added such as Power amplifiers, isolators, attenuators,…

Our objective is to measure simultaneously power parameters (Pin, Pout) and DC parameters (Voltage and current to calculate consumption and PAE) within very short time. These parameters are needed at each frequency/input power point. In fact, normal and fast

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

behavior of VNA consists in performing RF measurements without interruption (communication with external test benches like oscilloscope etc). For our products, we need to perform DC measurements exactly at the moment when the input signal is stabilized, before the VNA set the next point.

The first idea would be to trigger the frequency/power sweep. At each point, the VNA performs RF measurements and waits for the next trigger before moving to the next point. Then, test software communicates with oscilloscope to perform DC measurements. After this operation, the next trigger is sent by the software. In this mode the VNA sweep is interrupted by an external triggering. This communication mode is very time consuming. Therefore, the benefit of using VNA is low and comparable to classical test bench.

VNA and DC measurement systems have to communicate without VNA interruption.

2.2.2. Parallelize a VNA with a DC measurement system

DC measurements (Voltage & current) have to be performed at each frequency/power point generated by the VNA.

Unfortunately, oscilloscopes don't have enough memory depth to capture signals with high accuracy over a long period of time (covering all the frequency/power points). The idea is to know exactly when this DC measurement can be performed with an established signal (frequency/power).

The VNA is running on its own and will not wait between two points. The solution is to get a 'busy' signal from the VNA to indicate exactly when the VNA performs the measurement. During this short time, the input signal is necessarily stabilized.

This 'busy' signal will be used as a trigger for the oscilloscope dedicated to DC measurements. At each input trigger, the oscilloscope will start acquisition over time only covering the pulse duration for the current point. Then the scope has to rearm itself before the next frequency/power point.

At the end of the VNA sweep, test software has just to get all the segmented data by remote connection (GPIB, USB, LAN ,….)

Figure 1 shows pulse synchronization for simultaneous DC and RF measurements.

Figure 2 shows the description of segmented memory on oscilloscope

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

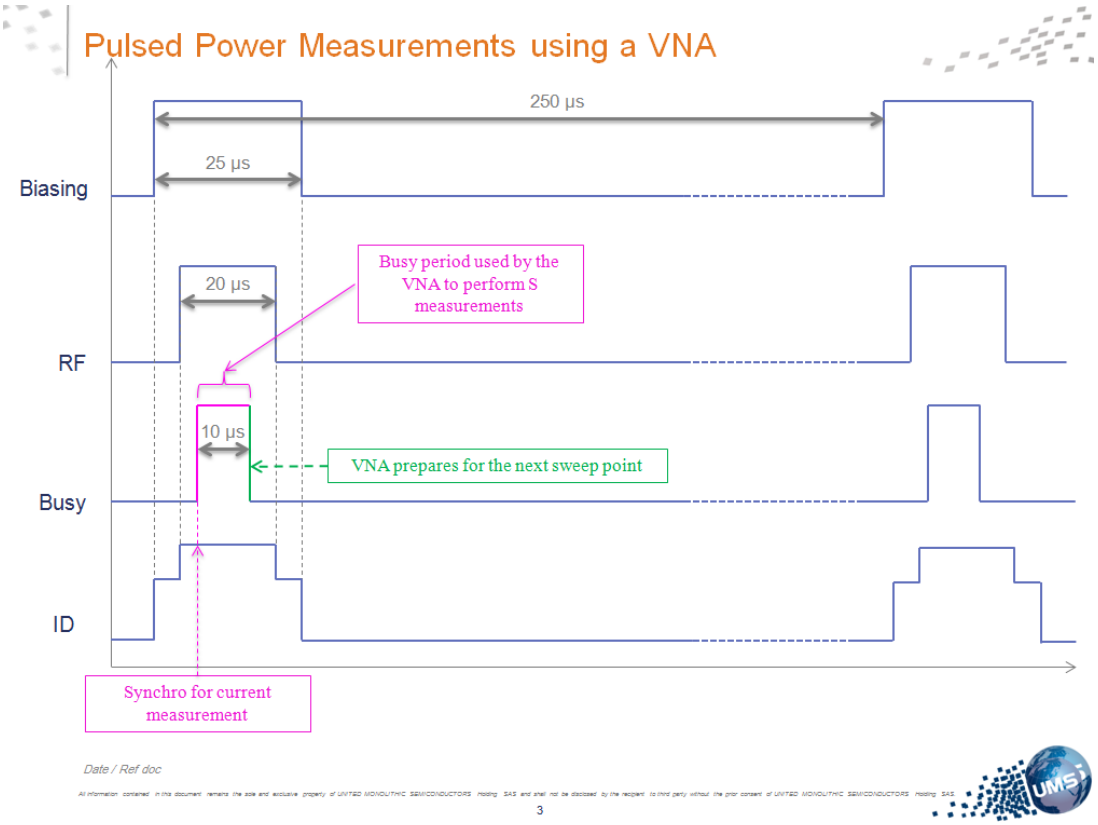


Figure 1 : Description of pulse synchronization (RF and DC measurements)

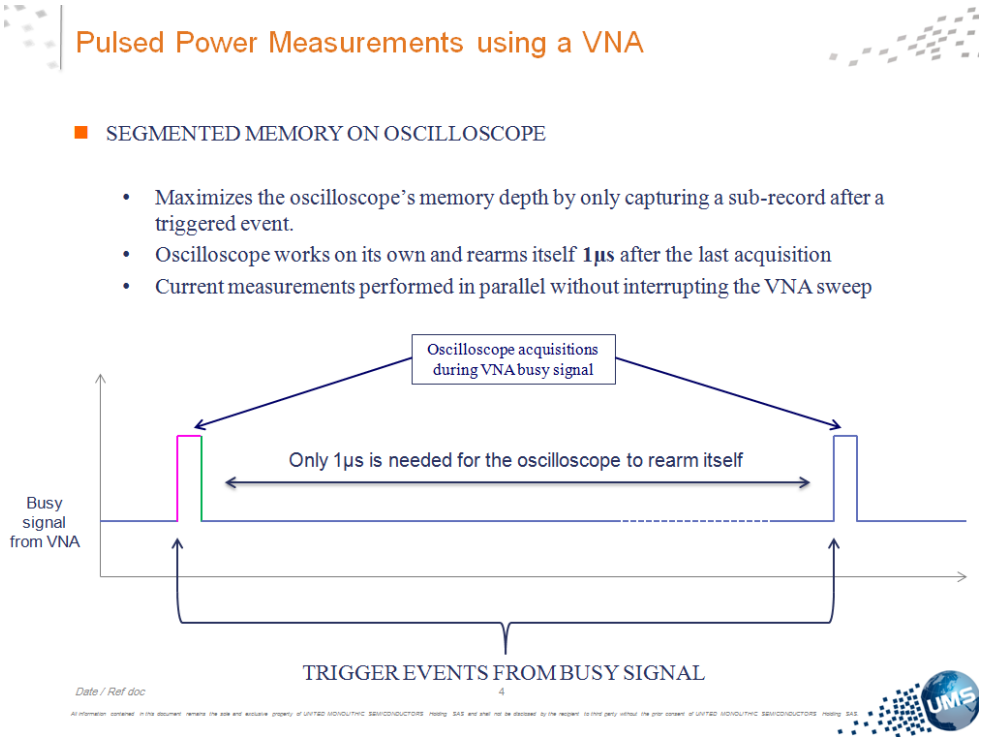


Figure 2 : Segmented memory-Oscilloscope

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

With high speed test bench, test time is divided by more than 100 with 1000 measured points. Considering previous 4 inch wafer, test time of 83 hours using classical test bench is now less than 50 minutes using new test bench.

2.2.3. High speed test bench need a high speed software

With test time reduction, we are facing another problem. Indeed, each second becomes important and any lost time in the test software can affect the throughput.

Test software has a lot of information to display in real time: progression in test sequence, status of the executed tests, measurements (data & graphics), statistical data, yield…

The display and the data refreshing are the main causes of waste of time in test software. Thanks to powerful multi-core computers, parallel operations are allowed.

Maximizing computing resources provided by multi-core processors requires some adjustments of the software application: Use of multiple threads within applications becomes mandatory. Multiple threads are not easy to develop, manage and debug. Robust IDE (integrated development environment) is required for providing powerful tools.

To achieve the last challenge, we improve the test software in order to separate (in different threads) the remote control of the test bench from the data display.

3. E-Band test benches for on wafer test

The aim of this chapter is to describe some standard E-band configuration for on wafer production test bench used at UMS in a production environment. To illustrate each configuration, a product has been selected

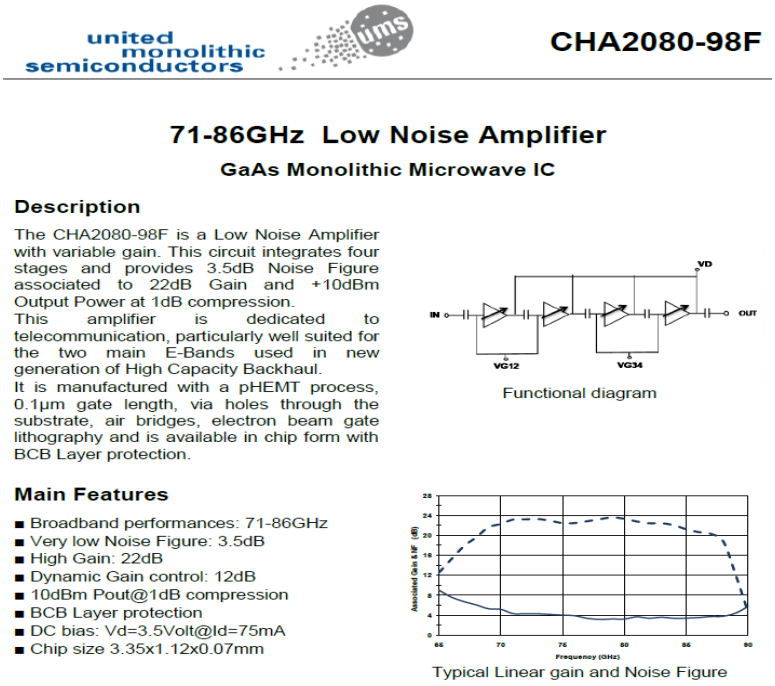
All test benches with the associated probe stations are driven by test software developed by UMS in LabWindows/CVI.

In the following figures (Figure 3 to Figure 10), product features and test benches dedicated to S parameter and conversion gain tests are presented.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

3.1. S parameter measurements : Low noise amplifier



united monolithic semiconductors

CHA2080-98F

71-86GHz Low Noise Amplifier

GaAs Monolithic Microwave IC

Description

The CHA2080-98F is a Low Noise Amplifier with variable gain. This circuit integrates four stages and provides 3.5dB Noise Figure associated to 22dB Gain and +10dBm Output Power at 1dB compression.
This amplifier is dedicated to telecommunication, particularly well suited for the two main E-Bands used in new generation of High Capacity Backhaul.
It is manufactured with a pHEMT process, 0.1µm gate length, via holes through the substrate, air bridges, electron beam gate lithography and is available in chip form with BCB Layer protection.

Functional diagram

Main Features

- Broadband performances: 71-86GHz
- Very low Noise Figure: 3.5dB
- High Gain: 22dB
- Dynamic Gain control: 12dB
- 10dBm Pout@1dB compression
- BCB Layer protection
- DC bias: Vd=3.5Volt@Id=75mA
- Chip size 3.35x1.12x0.07mm

Typical Linear gain and Noise Figure

Figure 3 : Main Features of CHA2080-98F (E band LNA)

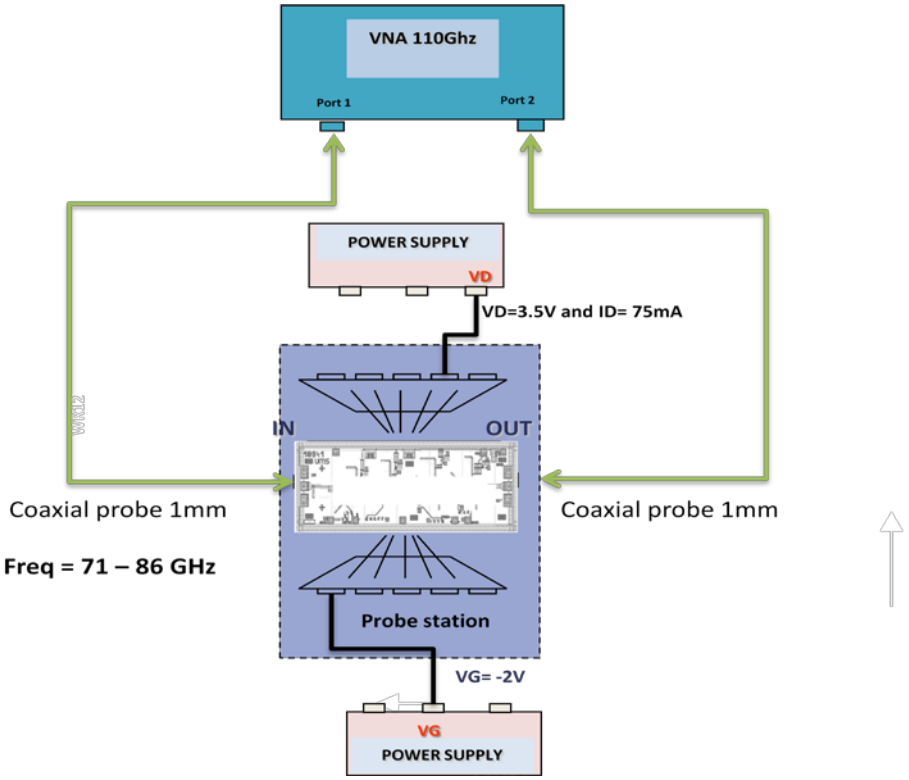


Figure 4: Setup description dedicated to E band S parameter measurements

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

3.2. Conversion Gain measurements: Down Converter

United Monolithic Semiconductors

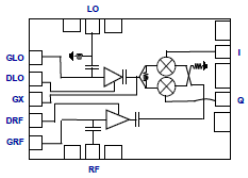
CHR1080a98F

71-86GHz Down-converter

GaAs Monolithic Microwave IC

Description

The CHR1080a98F is a multifunction monolithic receiver, which integrates a balanced sub-harmonic cold FET mixer, a LO buffer, and a RF low noise amplifier.
It is designed for the E-band telecommunication application, particularly well suited for the new generation of high capacity backhaul.
The circuit is manufactured with a pHEMT process, 0.10µm gate length.
It is available in chip form.



Main Features

- Broadband RF performances: 71-86GHz
- 8dB Conversion Gain
- 5dB Noise Figure
- -10dBm Input Power at 1dB compression
- DC bias: Vd=3.5V @Id=175mA
- Chip size 3.43x2.24x0.07mm

Figure 5 : Main Features of CHR1080a98F (E band Down-converter)

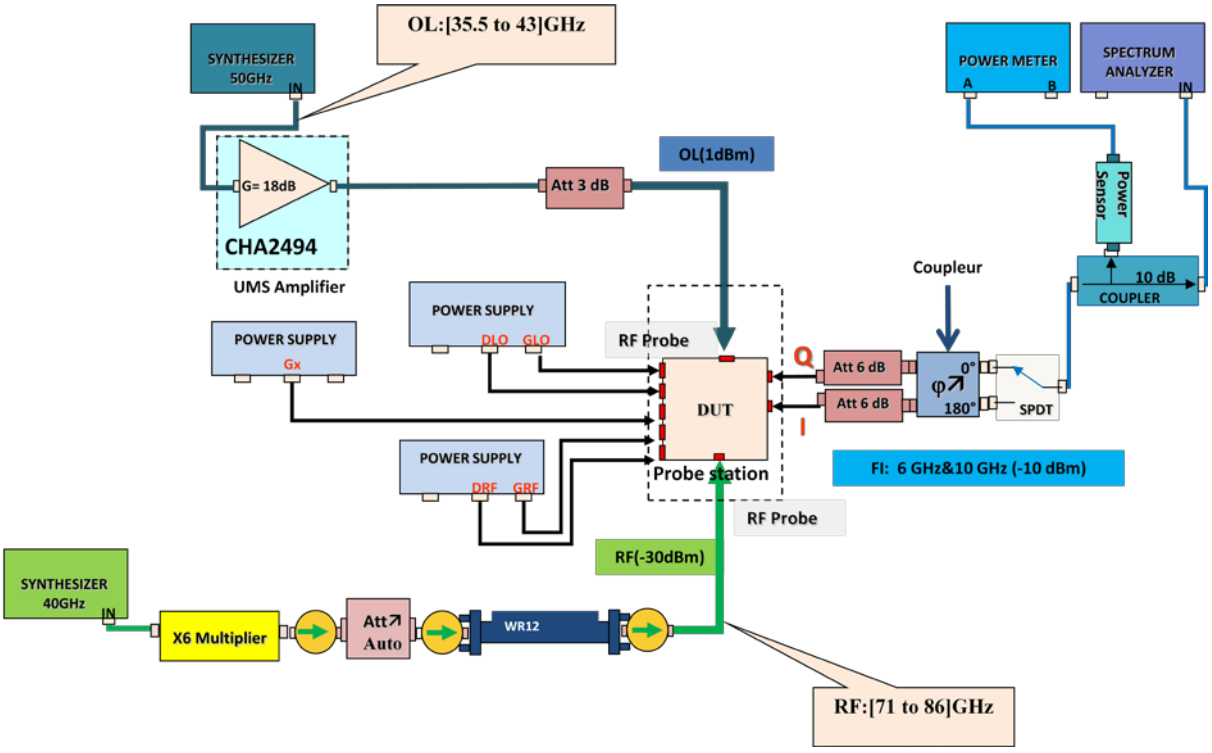


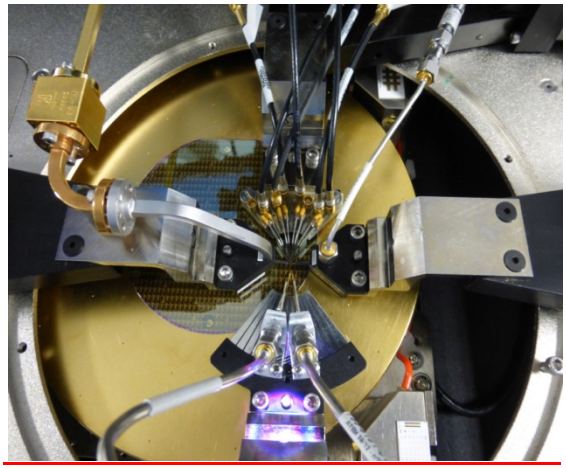
Figure 6 : Setup description dedicated to E band conversion gain measurements

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

DC

RF



LO

FI

Figure 7 : Picture of probe station –Mixer configuration

3.3. Multiplier X2: FBL_XD1901 (Filtronic design)

- Freq IN [35.5Ghz-38Ghz]
- Freq Out [71Ghz-76Ghz]

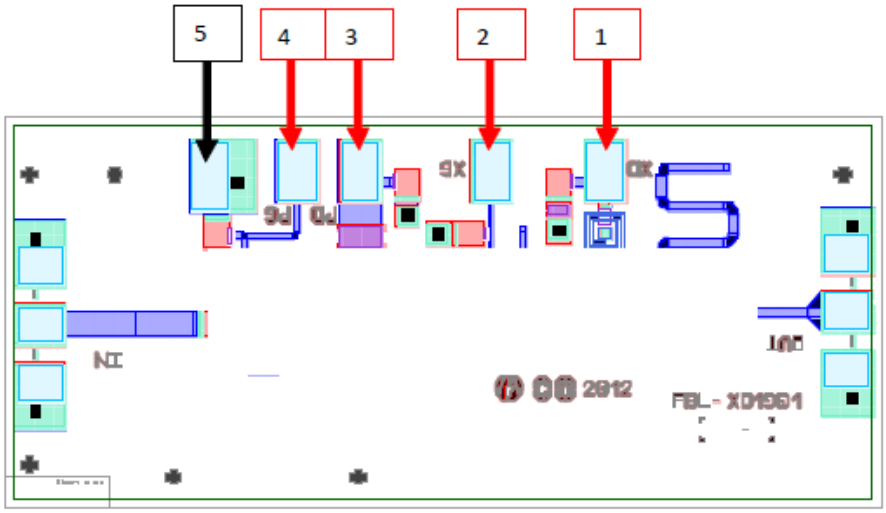
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

Frequency doublers

FBL_XD1901 (on maskset ULP003)

		min	max	100% on-wafer test, 25°C condition
Input frequency (LO/2)	GHz	35.5	38	35.5GHz, 36.75GHz, 38GHz
Output frequency (LO)	GHz	71	76	71, 73.5, 76GHGz
Output power at LO frequency	dBm	-4		Pin=0dBm Vg (pre-amp) = +0.1V, Vd (pre-amp) = +2.5V
Positive supply current	mA		60	Vg (x2) = -0.5V, Vd (x2) = +2.0V



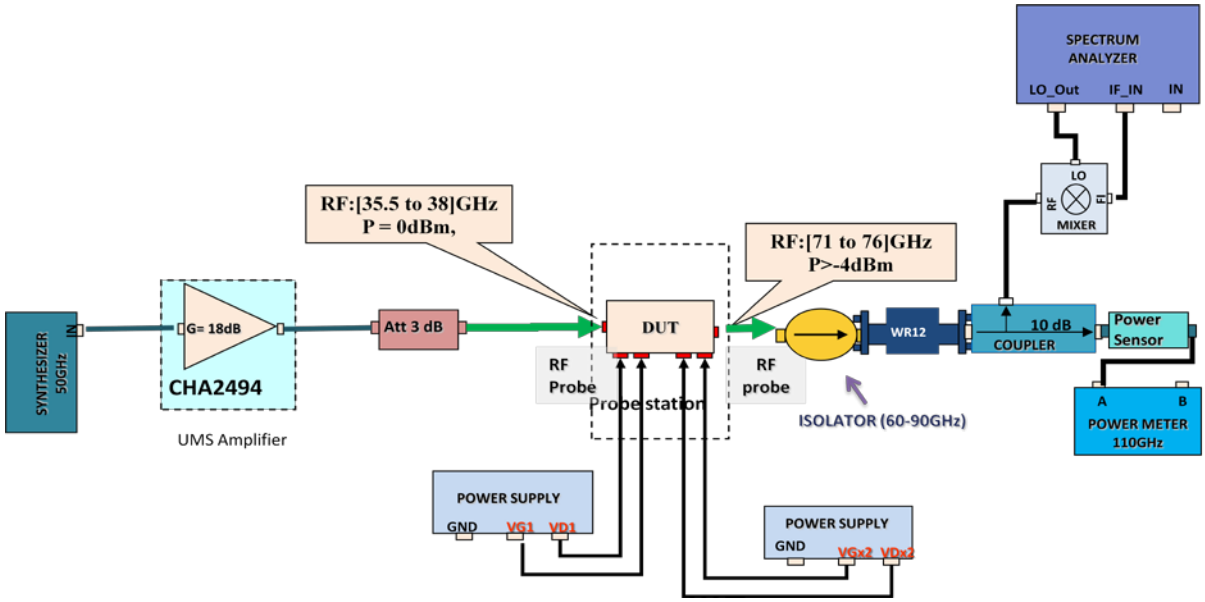


Figure 8 : Setup description dedicated to E band multiplier measurements.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

4. Software Development for production test

4.1. Software for Setup validation for on wafer test

The validation of a setup can require a lot of effort depending of the number of tested parameters. In a production environment addressing automotive, telecom, space, defense market with a high number of references and functions to be tested, the effectiveness is a part of the continuous improvement. On this observation the development of an automated tool to validate a setup was considered. The on wafer setup validation is taken

Automated setup validation description

The first phase is to define a golden wafer or golden dies of the selected product. The first measurement of the wafer will be the reference. These data are stored in an oracle data base with a die to number traceability.

The second phase is to define a product recipe with the relevant tested parameters for acceptance of the setup. A specific software interface has been developed to create the recipe, the parameters to be controlled are automatically proposed in a list coming from the test sequence by itself.

The control limits (LCL & UCL) are defined for each tested parameters based on repeatability and reproducibility approach.

Figure 9 describes an example of recipe showing the list of tested parameters.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

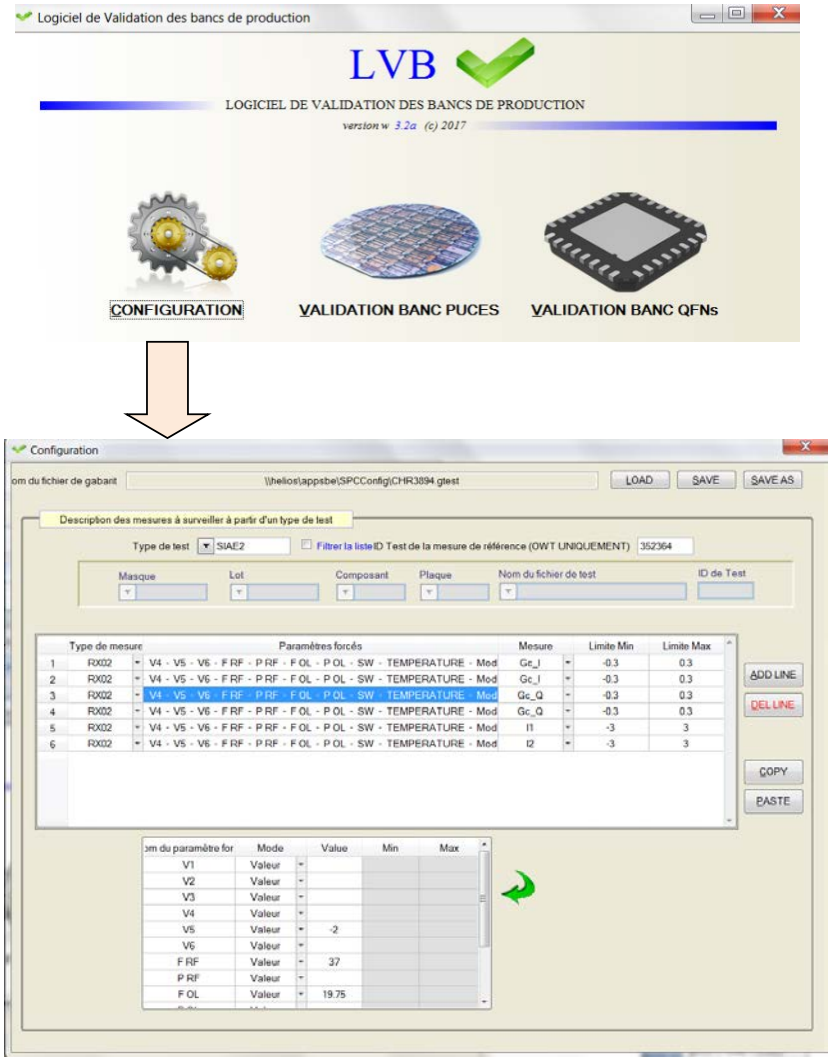


Figure 9 : Example of recipe with the list of tested parameters.

As shown in Figure 10, the final phase is to define a sampling mapping on the golden wafer including good and bad parts. Those chips will be tested and compared to the reference measurement before launching the production lot. This comparison is made for each die and each electrical parameter (parameter variation). The software provides a status of the setup; all parameters in the recipe have to be in the control limits. If a parameter failed, an indication will be display with a red cross and the setup will be not validated. Different statistical functions are available for data analysis.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

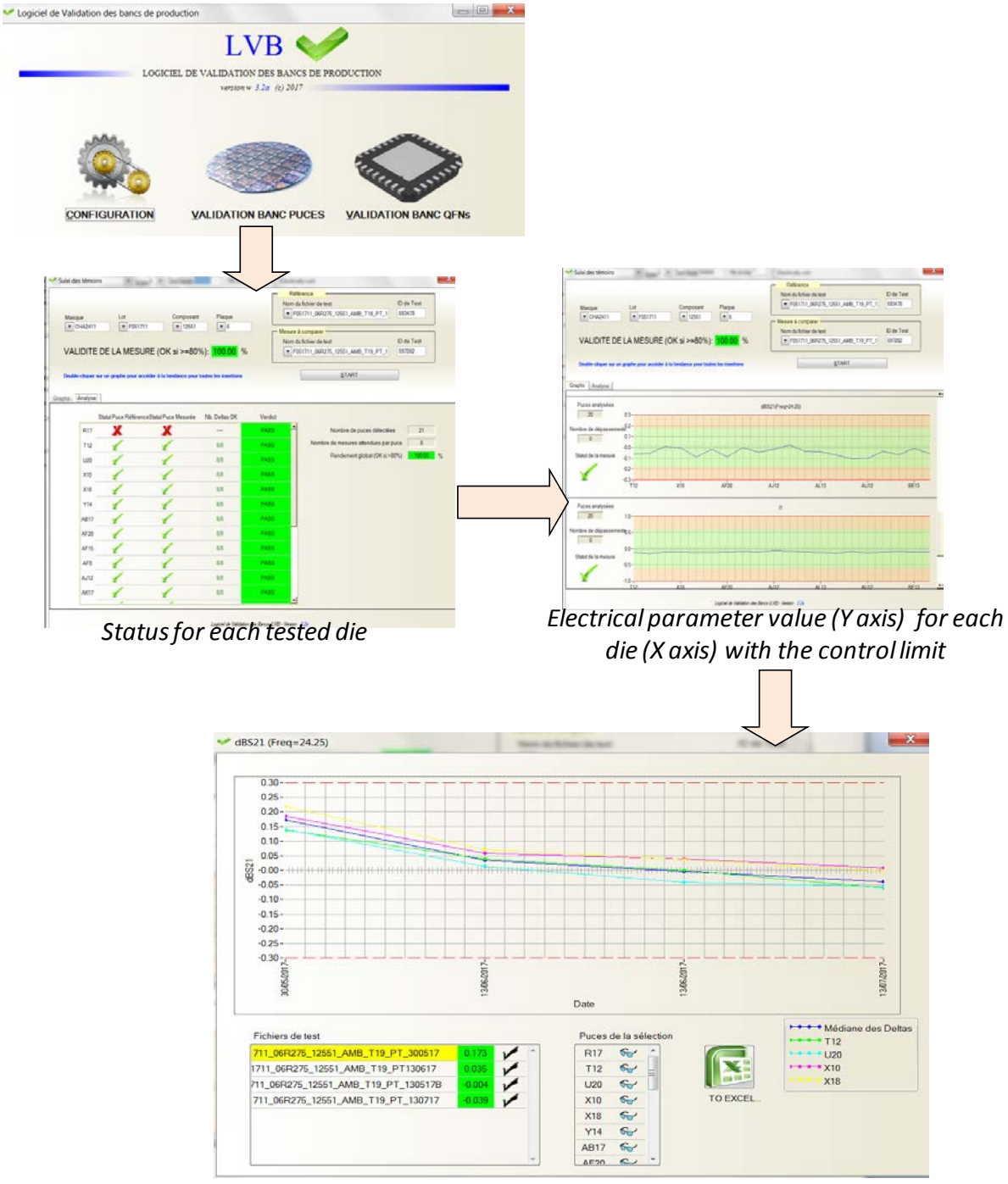


Figure 10 : Trend per die and per electrical parameter (Y axis) over the different setups(X axis)

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

This automated setup validation led to improve our agility. A similar application has been developed to validate a setup at the final package test in QFN based on the median value of the golden population

4.2. Test floor monitoring in real time

The access in real time of the test equipment is required for a close follow-up of the activity (throughput, yield, down time, wafer mapping,…). On this basis three main applications have been developed to support these needs.

- Software to display the electrical mapping in the open space of the test engineers on large screen (Figure 11)

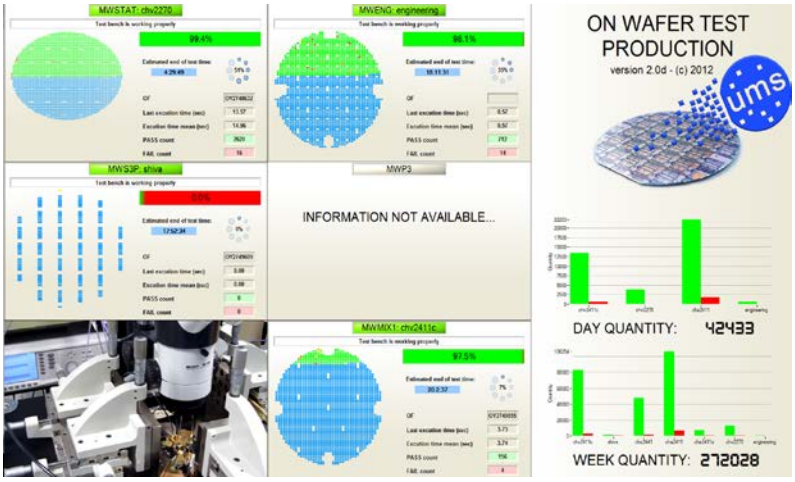
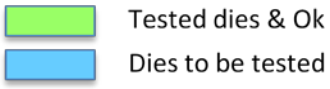


Figure 11 : Software description for electrical mapping display



Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

- Software to provide in real time an overview of the test benches
    - Information available: product under test, yield, test time, starting hours of the lot, tested quantity, good and bad quantities (Figure 12)

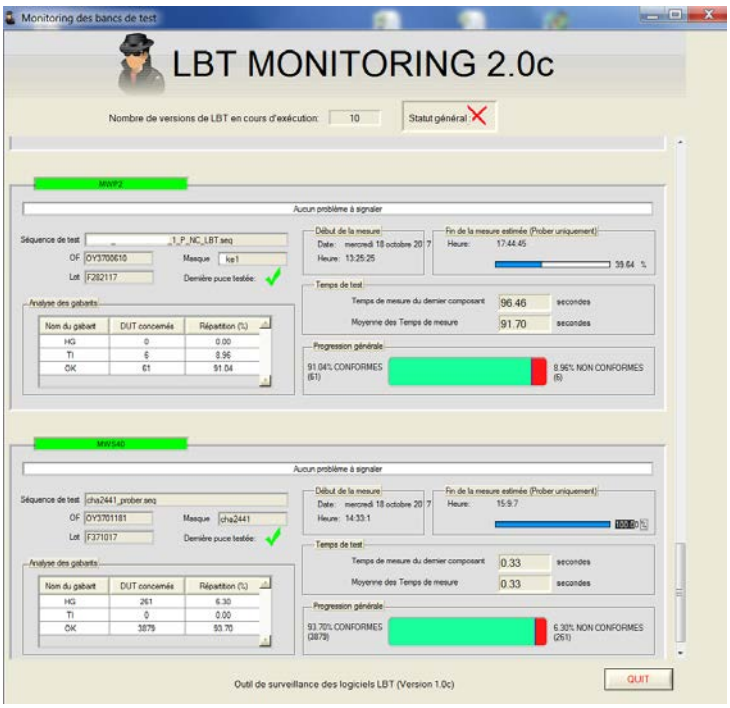


Figure 12 : Software description for real time test bench overview

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

- Software to analyze the overall day of production (Backend Production week :5 days/ 24hours with night shift)
    - Information available: production time and downtime over the days (Figure 13).

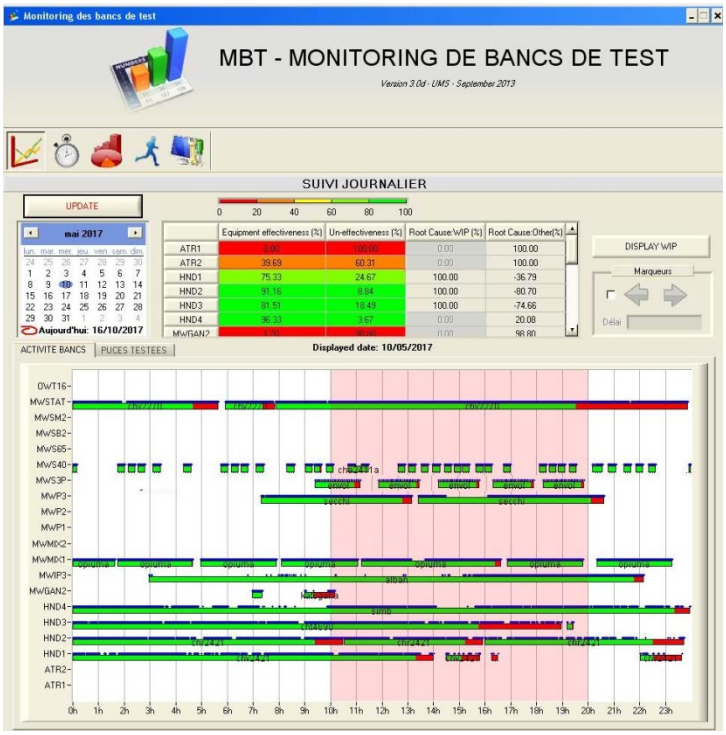


Figure 13 : Software to analyze the overall day of production

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

4.3. Data analyzing

As shown in Figure 14, a software has been developed for yield and detractor analysis (wafers and packages) based on production data (electrical and optical which are stored in oracle data base

- Easy access to electrical/optical mapping by selecting the product, lot number and the wafer
- Each electrical tested parameter can be selected for a detailed analysis (statistical distribution, outliers, detractor location on the wafer mapping …)

Figure 14 : Tested wafer mapping with tested parameter distribution

- Yield analysis on wafer lot with the associated detractors (Figure 15)

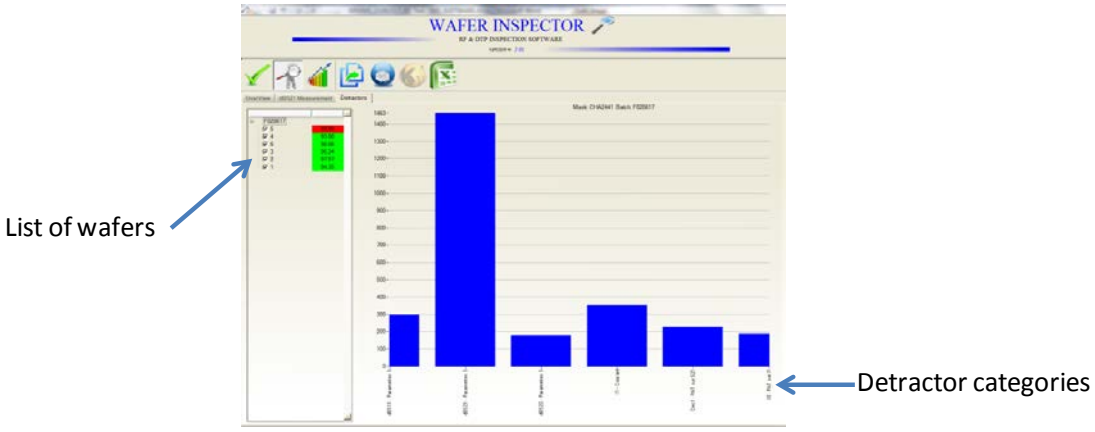


Figure 15 : On wafer yield analysis including associated detractors

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

Yield analysis per product over the time by selecting the window time (Figure 16).

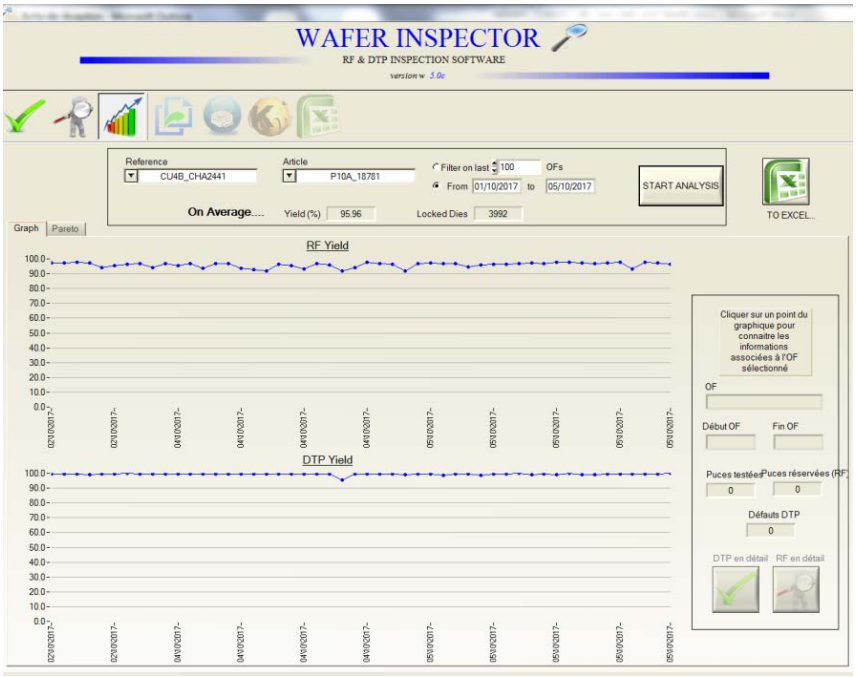


Figure 16 : Electrical yield trend

5. Conclusion

In a more and more complex environment with a high number of references/functions to be tested, hardware and software developments are the keys to provide agility to satisfy the demand. For all power applications in GaAs and GaN, both DC and RF measurements are required (output power, DC consumption and PAE). Test time is important in production environment especially in case of high number of dies or packages to be tested. Using VNA flexibility associated to external oscilloscope for DC measurements and new software, we have developed a powerful test bench enabling communication between RF and DC equipments without any interruption of VNA. Therefore, test time can be divided up to 100 (depending on number of tested points) keeping very accurate measurements.
Capability of software development led to develop automation in the monitoring of the activity, to develop powerful tools for data analysis (setup validation, production yields, wafer mapping, statistical analysis,…)
E band test bench are required industrialization phase offering a capability for E-band test with the benefit of all production tools.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

6. ACRONYMES / ABREVIATIONS

VNA	Vector Network Analyzer
DC	Direct Current
RF	Radio Frequency
Pin	Input Power
Pout	Output Power
PAE	Power Added Efficiency
LCL	Lower control limit
UCL	Upper control limit

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France

Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34