An 18 to 40GHz Double Balanced Mixer MMIC

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Abstract

This article describes a broadband, bi-directional mixer IC. The RF frequency range is 18 to 40GHz, the LO 20 to 42GHz and the IF 0.1 to 17 GHz. A double balanced passive topology is used to provide inherent isolation between all ports and good supression of spurious outputs. On-chip RF and LO baluns are included to provide an interface between the single-ended ports of the MMIC and the differential signals required by the double balanced mixer. The IC was fabricated on the PP15-20, 0.15µm gate length PHEMT process of WIN Semiconductor. With an LO drive of +10dBm the mixer has a measured conversion loss of between 7dB and 10dB, depending on frequency. LO to IF rejection is > 30dB.

1. Introduction

The design requirement for the mixer was an RF range of 18 to 40GHz, an IF range of 0.1 to 17GHz and an LO input range of 20 to 42GHz. A passive design was required, as the mixer needed to operate as both an upconverter and a downconverter. A double-balanced design was selected to benefit from the inherent isolation it would offer between the RF, LO and IF ports and the improved supression of spurious products (all even order products of the LO and/or the RF are inherently suppressed [1]).

2. Design and Simulation

The first consideration in the design process was the choice of mixer topology. A quad-ring resistive (or switching) mixer was chosen as it offers small size, good linearity [2] and high LO rejection. This topology has a balanced (differential) interface at RF, LO and IF ports, as depicted in Figure 1.

The transistors (depletion mode PHEMTs) in the mixer are biased at 0V Vds and therefore behave as switches [3]. The gate is DC biased at a point between 0V (switching transistor in its low loss state) and pinch-off (switching transistor in its low loss state). An LO drive signal is then superimposed on the gate bias switching the transistors between their high and low loss states at the LO frequency. The selected MMIC process needed to have transistors that provided good switching performance to mm-wave frequencies and a short gate length PHEMT process satisfied this criteria.

Initial simulations were undertaken assuming ideal baluns at all ports. This allowed the optimum device size and gate bias voltage to be selected for the mixer transistors (drain-source bias is 0V as stated above). Choice of device size is a trade-off between low on-state loss (large gate width devices) and high off-state isolation (small gate width devices). The optimum gate bias voltage was determined to be –1.4V. However, this was based on the nominal device models provided by the foundry and the optimum voltage would vary with process spread and with temperature. A direct gate bias scheme was therefore not appropriate and an on-chip active bias network was designed to set the gate bias voltage and provide a degree of compensation with process spread and temperature. The active bias network operates from a –5V supply at a current of less than 2mA.

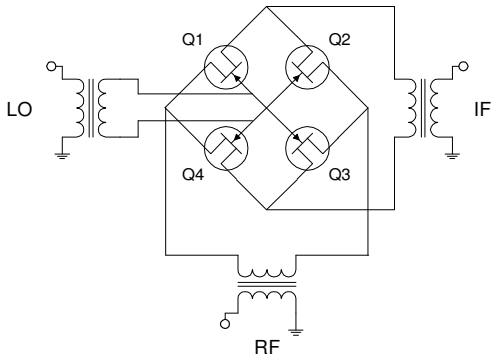

Figure 1: Quad-ring switching mixer

At low frequencies the gate-source/gate-drain capacitance of the PHEMTs in the mixer is small and the reactance is high. It is therefore straightforward to use a resistor to define the terminating load for the differential LO drive. As frequency increases the capacitive reactance at the gates reduces and the terminating resistance must be reduced if it is to remain the dominant load. At mm-wave frequencies this approach is no longer effective as the required resistance would be too low. A low impedance at the LO port of the mixer would reduce the effective LO voltage swing and degrade both the conversion loss and compression performance of the mixer. In order to address the problem of reducing gate reactance with increasing frequency, an impedance matching network was included at the LO port of the mixer between the LO port balun and the gates. A 200Ω terminating resistor across the gate terminals of the mixer was used to provide a resistive load and a passive LC matching network was designed to maximise LO voltage swing across the resistive load (and so across the gates of the mixer). The input capacitance at the gates of the PHEMTs was absorbed in to this matching network, which also serves to provide a reasonable return loss at the LO port.

On-chip baluns were required at the RF and LO ports, and the next stage of the design process was to consider the most appropriate balun structure. One well-proven structure, capable of achieving broadband operation with low insertion loss, is the "Marchand Balun" [4]. This was originally a co-axial balun, but printed versions have since been developed. The multiple coupled line version, depicted in Figure 2, has been shown to be suitable for MMIC implementation with octave band operation [5]. Both the RF and LO balun were realised using this type of structure.

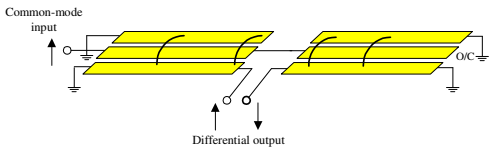

Figure 2: Multiple coupled line Marchand balun

The approach taken with the balun design was to initially use the multiple coupled line models in a conventional RF simulator to predict performance and balun dimensions. A full EM simulation was then undertaken to improve the accuracy of the simulation and allow the final optimisation of the balun dimensions. EM simulated amplitude imbalance across the 18 to 40GHz RF band was < ±0.12dB. The phase imbalance predicted by the EM simulation showed a gradual increases with frequency across the band but was still only 7° away from ideal at 40GHz. Simulated excess insertion loss was less than 0.85dB across the 18 to 40GHz operating band and the input match was better than 14dB. Measured performance of stand alone balun test structures are not available but a plot showing the EM simulated performance of the RF balun analysed as two port structures, with the outputs differentially combined in an ideal transformer, is shown in Figure 3. The simulated insertion loss is below 0.8dB across the entire RF band, with a good guard band at the high frequency end.

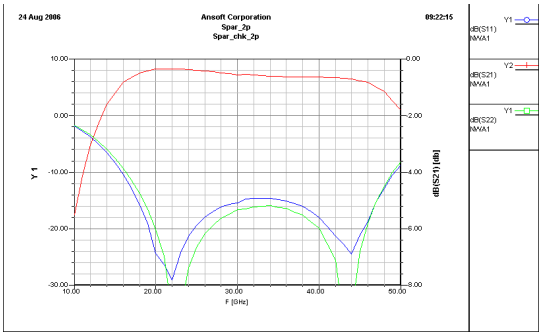

Figure 3: EM simulated, insertion loss and matches of RF balun, as a 2-port

Performance simulations of the entire mixer used EM simulator generated 3-port s-parameter files for the LO and RF baluns. Foundry supplied large signal transistor models were used for mixer transistors and the active bias network. Great care was taken with the layout to preserve symmetry as this would be critical in obtaining good LO rejection. All interconnect tracking, air-bridge cross-overs and discontinuities in the LO matching network were EM simulated. The resultant simulated conversion loss versus LO frequency of the whole mixer MMIC in downconvert mode is plotted in Figure 4. For this simulation the RF frequency was fixed at 19.6GHz and the LO swept from 20 to 36GHz (resulting in an IF output of between 0.4GHz and 16.4GHz). The red trace represents an LO power of +10dBm and the blue trace an LO power of +13dBm. For an LO drive of +10dBm the simulated conversion loss varies between 8.4dB and 9.7dB across the band.

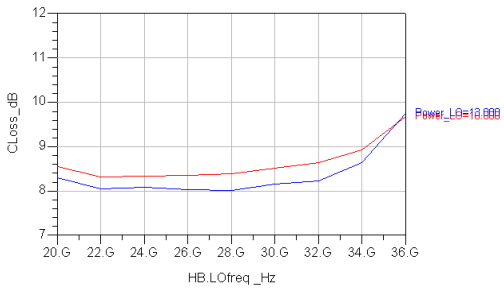

Figure 4: Simulated RF to IF downconversion loss versus LO, RF fixed at 19.6GHz

A simulation of the conversion loss in upconvert mode is plotted in Figure 5. In this case LO frequency is fixed at 23.5GHz with a swept IF. As with the downconvert simulation the red trace represents an LO drive level of +10dBm and the blue trace an LO drive level of +13dBm. For an LO drive of +10dBm the simulated conversion loss varies between 7.6dB and 8.5dB across the band.

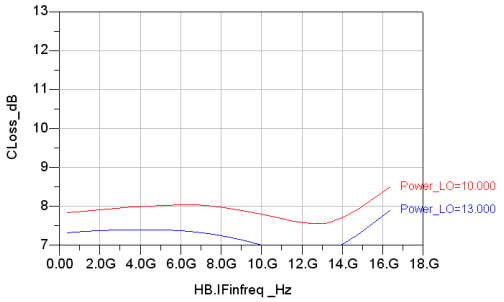

Figure 5: Simulated IF to RF upconversion loss versus IF, LO fixed at 23.5GHz

3. Realisation

The MMIC was fabricated on the PP15-20, 0.15µm gate length PHEMT process of WIN Semiconductor. A photograph of one of the mixer MMICs, whilst under RF On Wafer (RFOW) test, is shown in Figure 6.

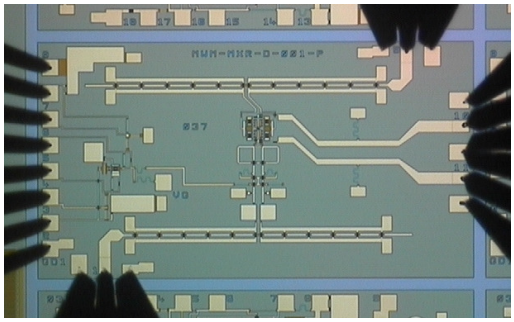

Figure 6: Photograph of the mixer MMIC

The single ended RF port is on the top side of the photograph and the single ended LO port is on the bottom side. These two ports can be seen interfacing to Ground-Signal-Ground (GSG) RFOW probes. The differential IF ports to the right interface to differential G-S-G-S-G RFOW probes for test. The DC probes to the left are for application of the –5V bias and monitoring of various voltages generated by the on-chip active bias network. The mixer itself requires only a –5V supply as the gate bias potential for the mixing transistors is generated by the on-chip active bias network.

4. Measured performance

The possible permutations of measurement that could be presented for a broadband frequency-converting component are extensive. A limited subset of the actual measurements made is necessarily presented here. The data selected attempts to provide adequate representation of most aspects of the mixer's performance. However, some features that may be of interest to certain readers may have been omitted. In this case interested parties are invited to contact the authors directly. All of the measurements presented below were made using RFOW probing. An off-chip connectorised balun was used to transform the differential IF signal to single-ended for ease of measurement.

Figure 7 shows the measured conversion loss of the mixer in downconvert mode with LO fixed at 28GHz and the RF swept between 18GHz and 27GHz (giving an IF output of between 10GHz and 1GHz). The results for three representative devices (the solid traces) are plotted showing good device to device repeatability with the conversion loss varying between 7.9dB and 9.9dB across the band. This compares favourably with the simulated performance, the dotted trace in Figure 7, which predicted an almost flat conversion loss of around 8.4dB.

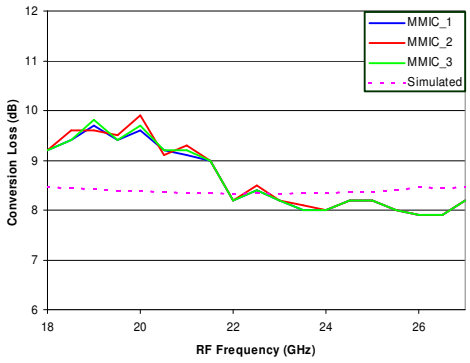

Figure 7: RF to IF downconversion loss versus RF, LO fixed at 28GHz

Figure 8 shows the conversion loss of the mixer in upconvert mode with the LO fixed at 36GHz and the IF swept between 0.5GHz and 17GHz. The resulting RF output is between 35.5GHz and 19GHz. Measured results for the same three representative devices are plotted (the solid traces) along with the original simulated performance (the dotted trace). The measured conversion loss varies between 6.9dB and 10.4dB across the band. This compares favourably with the simulated performance, which has a flatter response with conversion loss varying between 8.6dB and 9.3dB across the band.

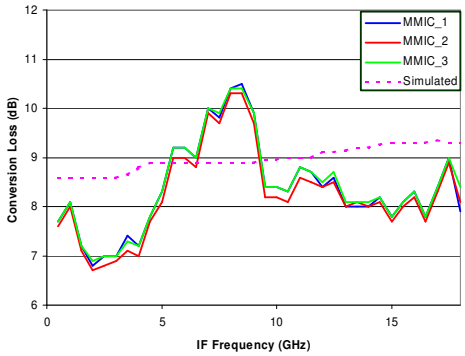

Figure 8: IF to RF upconversion loss versus IF frequency, LO fixed at 36GHz

The measured s11 at the LO port is plotted for the same three representative devices in Figure 9. This return loss is around 10dB across the band. Whilst not a perfect 50Ω, it is in good agreement with the simulated performance. During the design process this level of return loss was selected as representing a good-trade-off between input match and high LO voltage swing across the gates of the mixer.

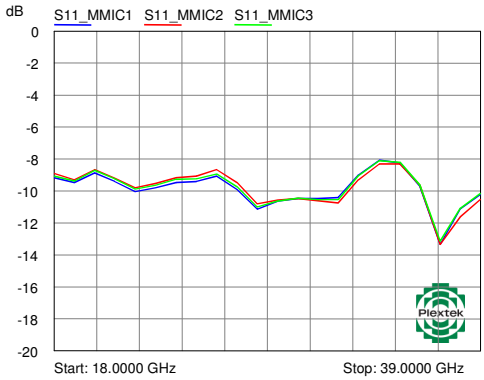

Figure 9: LO port s11 for 3 MMICs

The conversion loss performance versus LO drive level is plotted in Figure 10 for an LO of 28GHz and an RF input of 22GHz. Conversion loss is still reasonable even with an LO drive as low as +5dBm. As LO drive increases the conversion loss reduces gently. By the time the LO drive is +10dBm the conversion loss variation is levelling off. The simulated performance (dotted trace) is in good agreement with the measured.

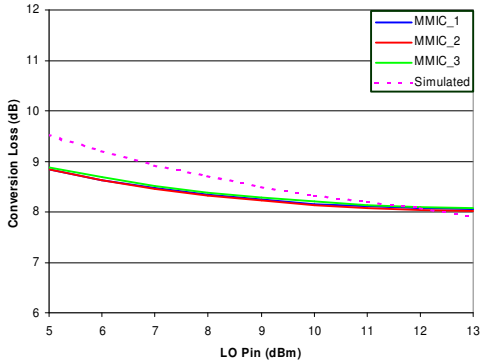

Figure 10: Downconvert conversion loss versus LO power level, LO=28GHz, RF=22GHz

Power transfer characteristics of the mixer were measured in both up and downconversion modes. Figure 11 shows the input power versus output power for the three representative devices at an RF of 40GHz and an LO of 42GHz (the top of both bands respectively). The input referred 1dB gain compression point (P-1dB) is around +3dBm. The measured P-1dB at lower LO frequencies increases to around +7dBm.

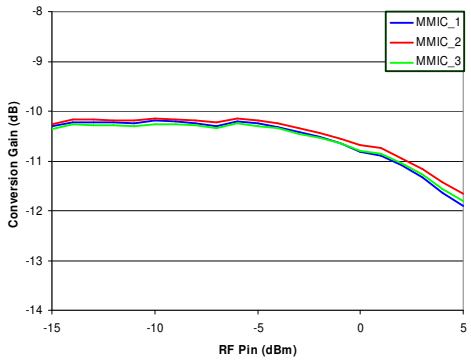

Figure 11: Downconversion compression characteristics, RF=40GHz, LO=42GHz

Similar power transfer characteristics in upconvert mode are plotted in Figure 12. The IF input is 9GHz and the LO is 36GHz, resulting in an RF output of 27GHz. The input referred P-1dB in this case is around +7dBm.

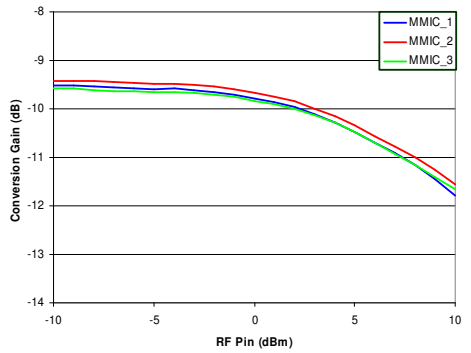

Figure 12: Upconversion compression characteristics, IF=9GHz, LO=36GHz

The measured LO to RF rejection is plotted against LO frequency in Figure 13 (strictly speaking the plot shows the LO to RF transmission rather than rejection). The level of rejection is determined by the performance of the on-chip baluns, the symmetry of the IC layout and the matching between devices on the IC. Leakage between the measurement probes can also affect the measurement and care must be taken to ensure that isolation between the probes is adequate. At low LO frequencies the LO to RF rejection is around 40dB. As may be expected this degrades gradually with frequency to around 27dB at the top of the LO band (42GHz). The LO to IF rejection was also measured and found to be greater than 30dB across the band.

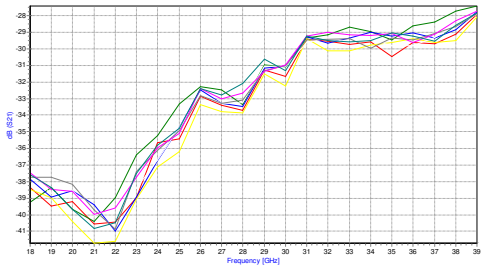

Figure 13: LO to RF transmission versus LO frequency

5. Summary and Conclusions

This paper has presented the design and measured performance of a broadband, passive (bi-directional) mixer MMIC realised on a commercially available PHEMT process. A summary of the measured performance is presented in Table 1.

Except where indicated, all measurements were made on-wafer with an LO drive level of +10dBm.

Parameter	Performance	Units
IF range	0.1 – 17	GHz
RF range	18 – 40	GHz
LO range	20 – 42	GHz
Conv. loss	7 to 10	dB
P-1dB (input)	3 to 7	dBm
LO to RF rej.	> 27	dB
LO to IF rej.	> 30	dB
LO port return loss	> 8	dB

Table 1: Measured performance summary

It should be noted that this MMIC design in the property of Elisra Electronic Systems Ltd.

6. References

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[4] Marchand, N. "Transmission-Line Conversion", Electronics December 1944, pp 142-145

[5] Devlin, L.M., Dearn, A.W., Pearson, G.A., Beasley, P.D.L and Morgan, G.D. "A Monolithic, 2 to 18GHz Upconverter", proceedings of the 2002 IEEE MTT-S