Thermal Analysis of GaN Devices

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Introduction

GaN devices, both in discrete FETs and MMIC form, are finding increasing use in microwave power amplifier and switch applications. When used in power amplifiers, up to four times the RF power is available from a given device size when compared to GaAs amplifiers, with comparable gain and efficiency. However the dissipated power per unit die area is also much higher, and great care needs to be taken with thermal management both from a performance point of view and more importantly to ensure adequate device reliability. Accurate thermal modeling is necessary to predict the channel temperature under a given set of conditions, since this parameter drives the reliability. At TriQuint, this has been performed over many years with a number of technologies, and this paper will describe recent work done on GaN on SiC HEMTs.

Thermal modeling method

Commercially available software is used at TriQuint to perform 3D thermal analysis using the finite element analysis method. The method has been validated by comparison to both infra-red measurements [1], and a combination of methods including Micro-Raman thermography [2].

The structure is broken down into a suitable number of nodes which together form a three dimensional grid or mesh. The mesh is programmed to contain the thermal conductivity properties of the various materials used. A number of assumptions are made to simplify the analysis, such as the heat source is uniformly distributed along the active GaN region, the width of the heat source is the same as the gate length and that the length of the heat source is the same as the gate width. It is also assumed that the total power dissipated is shared equally across all individual cells of the device. This assumption is considered valid for DC operation, but for RF operation will only apply in a multi-cell transistor when all cells are driven and loaded equally, which is not always the case in a practical amplifier realization.

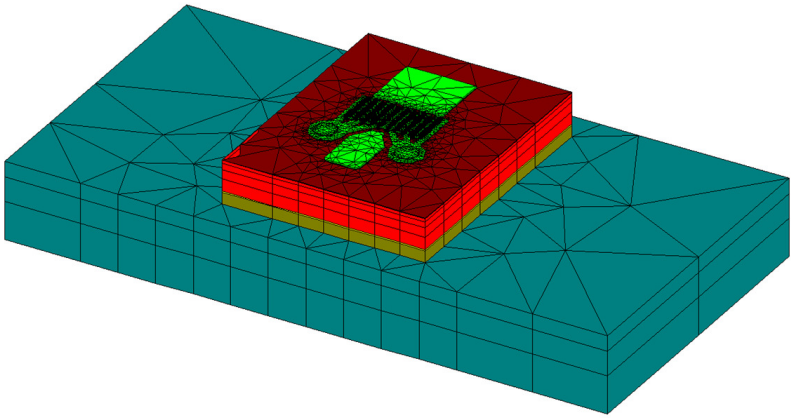

Fig 1 Device thermal analysis structure

The structure which was analysed is shown in Fig 1, represents as closely as possible an assembled device, such as that shown in Fig 2.

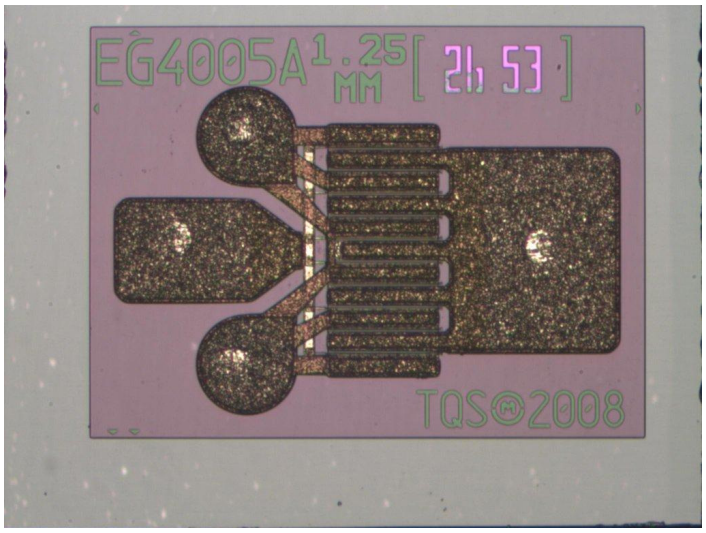

Fig 2 GaN HEMT (TGF2023-01)

It includes a metal carrier plate, a layer of AuSn solder of typical thickness, a layer of SiC representing the bulk of the device and finally a thin layer of GaN, where the heat sources are located. The backside of the carrier plate is generally set to be at a constant temperature (baseplate temperature). The structure allows for heat flow away from the active region via surface metallization as well as through the bulk substrate.

The analysis allows the temperature of all the nodes to be predicted from a given set of starting conditions. The temperature of the hottest node (usually under one of the central gates) is taken as the "channel temperature", and is then used to calculate the thermal resistance of the device.

The result of a typical thermal analysis stack is shown below in Fig 3. With a 0.5 x 0.68in carrier, the baseplate temperature was set at 70°C, and the dissipated power was 4.8W. The resulting temperature rises were as follows:

bottom of carrier to top of carrier 15.29°C
top of carrier (bottom of solder joint) to top of solder joint, 11.08°C
top of solder joint (bottom of device) to hottest channel 84.4°C

This leads to individual thermal resistances of 3.2 °C/W, 2.3°C/W, and 17.6°C/W respectively, and a total of 23.1°C/W.

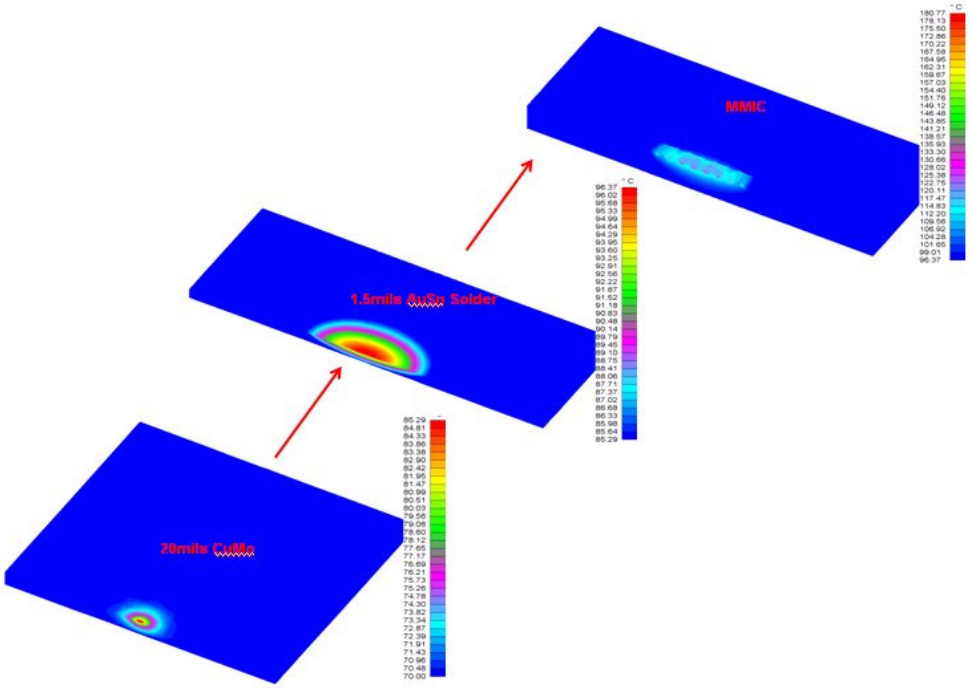

Fig 3 Individual layer thermal results

The definition that TriQuint uses for channel temperature may not be the same as other device manufacturers, and is certainly a higher figure than would be obtained experimentally from infra-red measurements, where the limited resolution of typical cameras means that a lower temperature is observed. However, the same definition is used to calculate the channel temperatures of the devices subjected to our accelerated life testing. This ensures that a calculation of channel temperature in a given application using the product of dissipated power and thermal resistance added to baseplate

temperature will be consistent with the median lifetime curve published in our data sheets. An example is given below in Fig 4.

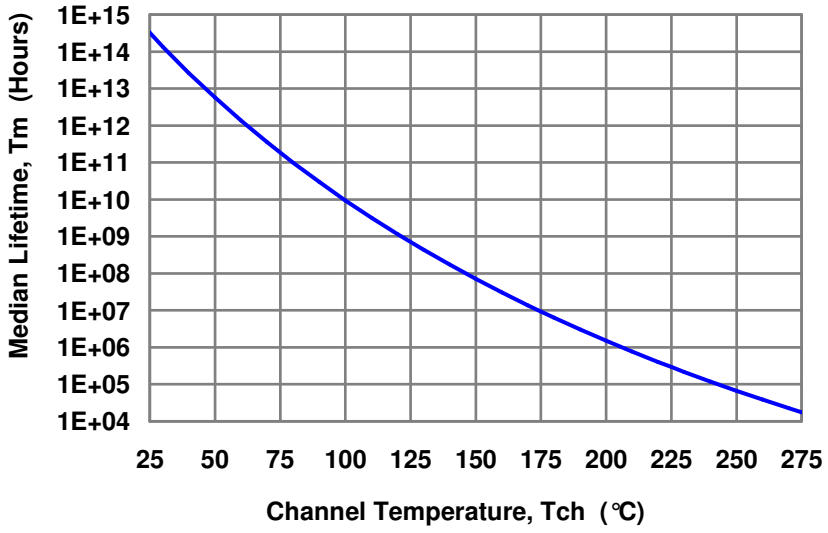

Fig 4 Median Life of GaN devices as a function of channel temperature

In order to obtain accurate results, it was necessary to incorporate the variation of thermal conductivity of the SiC substrate and GaN layer with temperature.. Fig 5 shows the variation in the thermal conductivity of SiC compared to GaAs over temperature, normalized to ~25°C. It can be seen that greater errors would result in using an average value of thermal conductivity for SiC compared to GaAs.

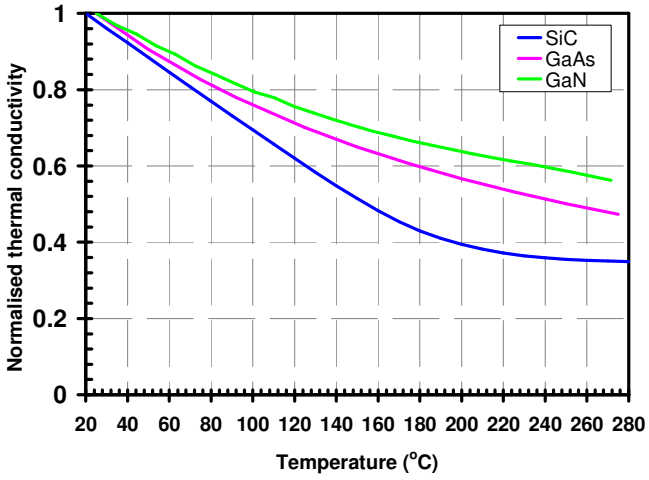

Fig 5 Variation of thermal conductivity of SiC, GaN, and GaAs versus temperature

Investigation of device layout and external parameters on thermal resistance

A matrix of devices were analyzed to look at the effects of varying the dissipated power, gate to gate spacing (pitch), gate finger length, number of gate fingers and baseplate temperature. The results are shown in Figs 6-9.

Figs 6 and 7 shows the predicted thermal resistance and channel temperature of an 8 x 100um finger device with 800um total gate periphery, as a function of baseplate temperature. It can be seen that the thermal resistance increases with baseplate temperature due to the variation in thermal conductivity of the SiC substrate and GaN layer with temperature. As a result, the channel temperature changes by approximately 30°C for a 20°C change in baseplate temperature.

Fig 8 shows the predicted thermal resistance for the same device as a function of gate to gate spacing. A larger gate to gate spacing reduces the effect of heating from one active area to another, and generally increases the die area giving a reduced thermal resistance. MMIC designers use this information when laying out devices to ensure the best compromise between thermal performance, electrical performance, and die size. The gate to gate spacing is of course fixed for commercially available devices.

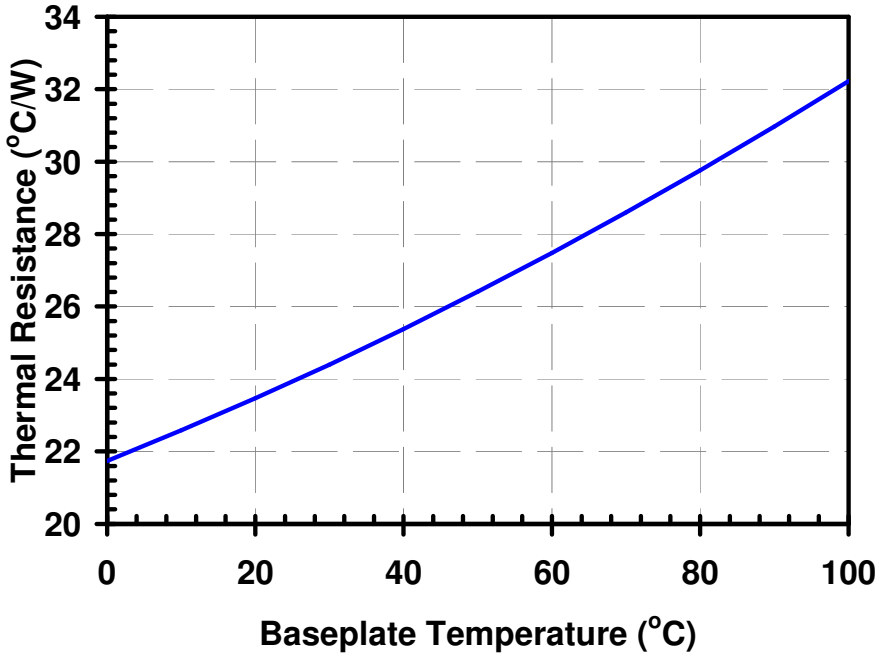

Fig 6 Variation of thermal resistance of 800um device with baseplate temperature

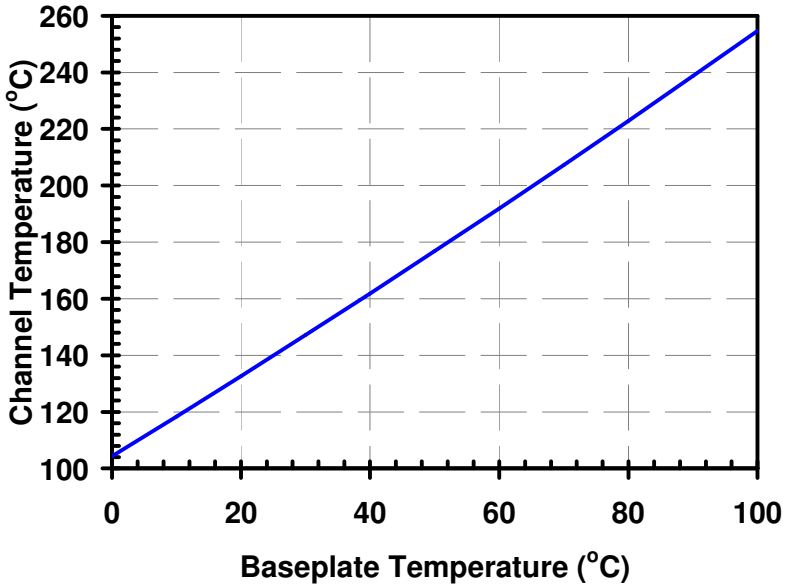

Fig 7 Variation of channel temperature of 800um device with baseplate temperature

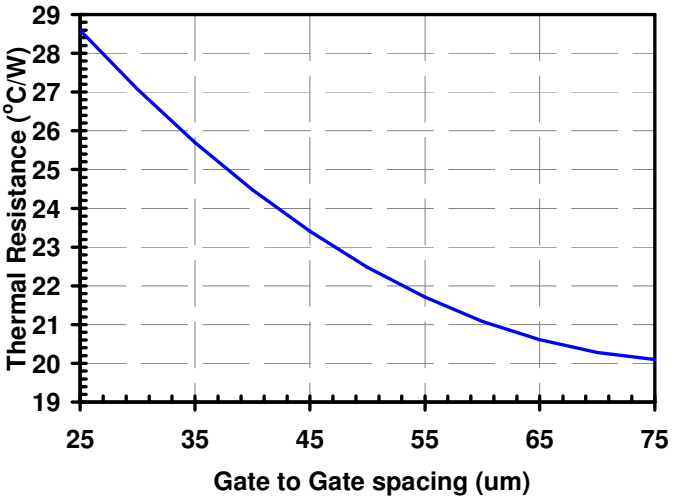

Fig 8 Variation of thermal resistance of 800um device with gate to gate spacing

The importance of analyzing individual device structures instead of simple scaling is illustrated in Fig 9. In this example, the device total gate periphery was changed by using different numbers of (100um) gate fingers and the thermal resistance calculated in each case. The power dissipation was scaled for the different resulting structures, to keep the dissipation per finger the same.

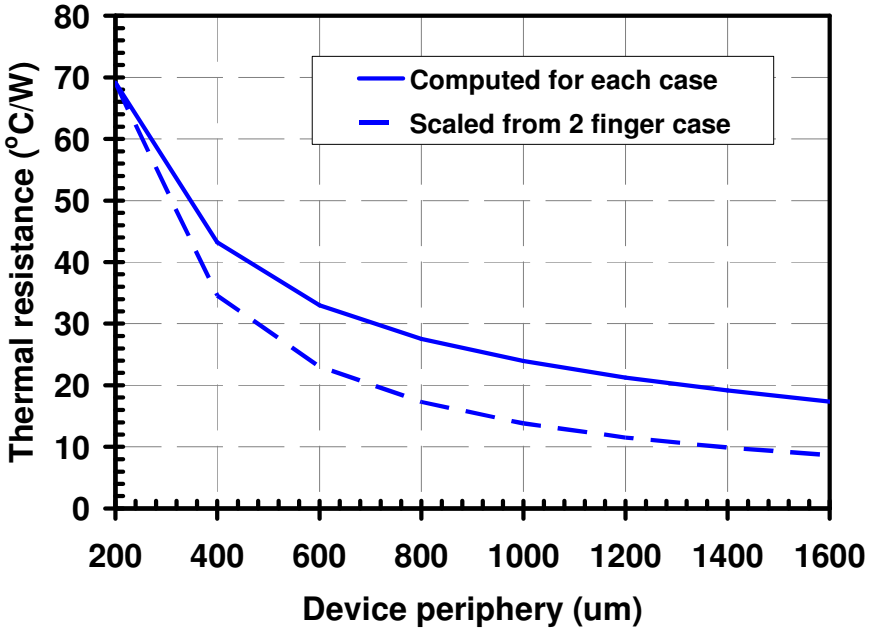

Fig 9 Variation of thermal resistance with device size

The graph shows the results of linearly scaling the thermal resistance of a 2-finger device. For larger periphery devices, scaling always predicts a lower thermal resistance than full analysis since the effect of mutual heating by adjacent active areas is not taken into account. Generally, devices need to be modeled on a case by case basis if accurate predictions of thermal resistance are to be made.

Thermal resistance of carrier plate to baseplate interface

The same method described above to model the thermal resistance of devices can be modified to include the heat transfer from the carrier to the mounting (chassis) plate, and down to the baseplate. The effect of varying the thermal conductivity and thickness of the attach material (epoxy/solder) was investigated as well as the thermal conductivity of the baseplate (which has the same dimensions as the carrier plate. The temperature of the lower side of the mounting plate was taken as the baseplate temperature in this case. The structure is shown in Fig 10.

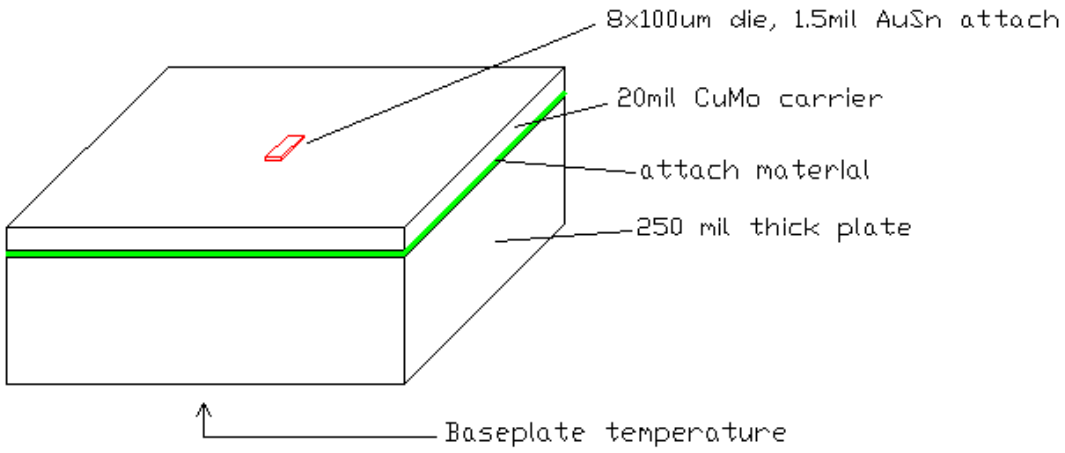

Fig 10 Thermal structure including carrier plate attach and mounting (chassis) plate

The increase in thermal resistance due to the attach material and metal plate as a function of the thermal resistance of the attach material (1 mil thick) is shown in Fig 11. The dissipated power was 4.8W and the baseplate temperature was 70C.

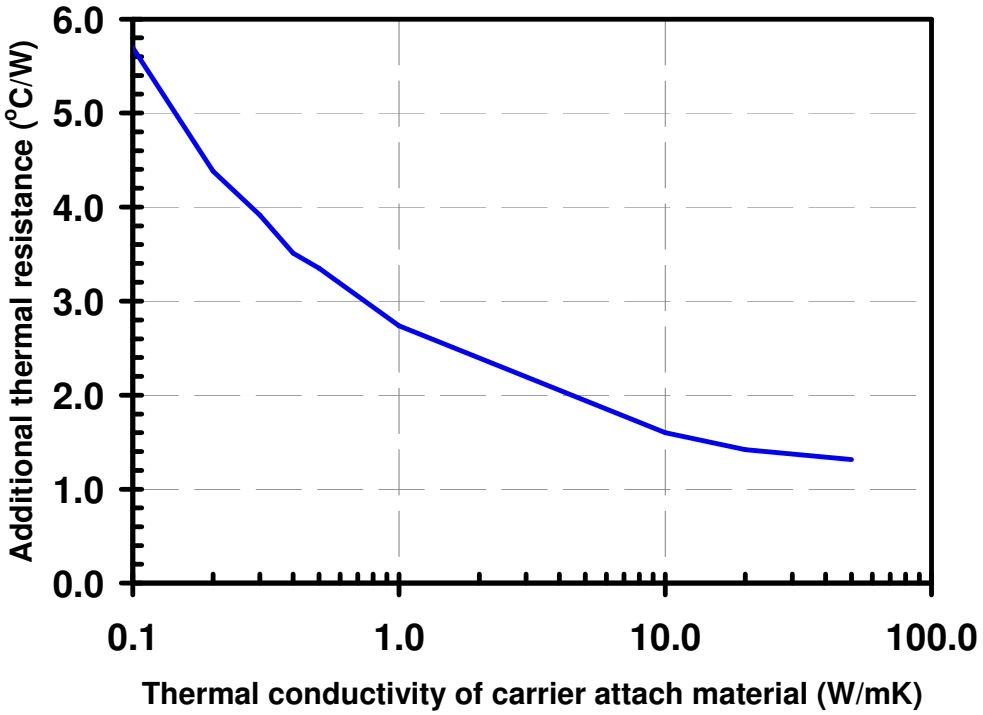

Fig 11 Additional thermal resistance of carrier attach material and chassis plate

For the majority of carrier attach materials with thermal conductivities >10W/mK, the model predicts that the additional thermal resistance is dominated by the thermal resistance of the metal chassis plate. The use of lower thermal conductivity materials in the 1-10W/mK region (such as some epoxies) can increase the additional thermal resistance considerably, especially if the thickness is greater – see Fig 12. This was computed for a material with a thermal conductivity of 1W/mK.

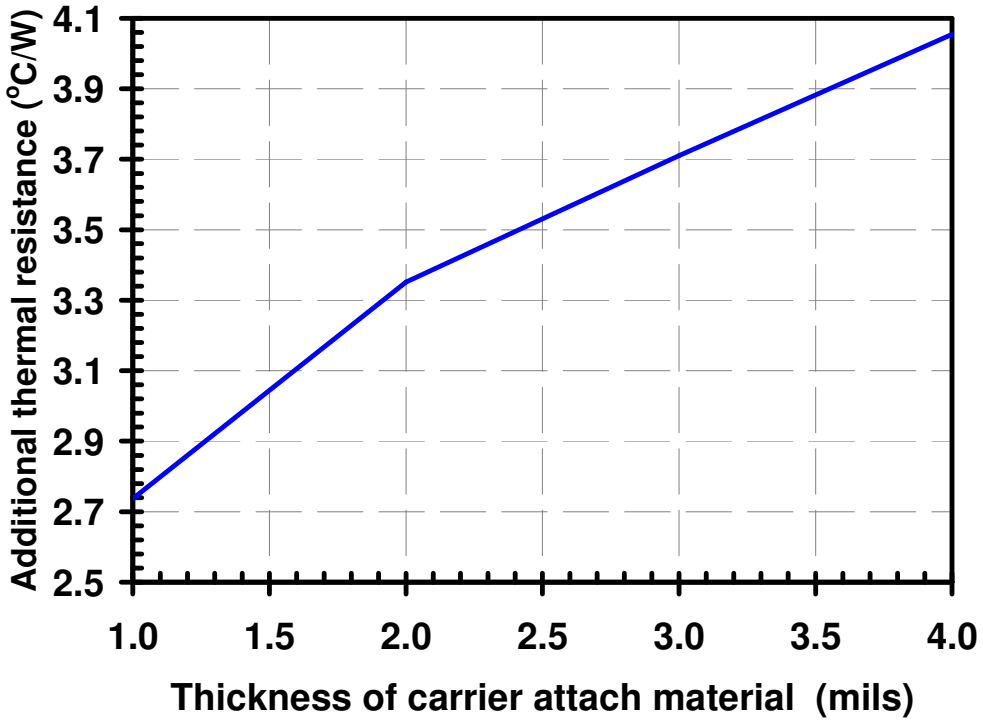

Fig 12 Effect of thickness of carrier attach material on additional thermal resistance

It should be noted that, while the thermal performance of an epoxy joint between a carrier plate and the chassis may be deemed adequate, the analysis does not take into account any adverse effects of high RF currents on the structure of the epoxy, such as may be encountered with discrete devices driven into saturation.

In some practical amplifier realizations, the carrier plate is not mounted to the chassis with any kind of attach material (solder or epoxy) and simply relies on screws or some other kind of mechanical mounting. Thermal modeling has been carried out to look in more detail at this case.

In one example a 5mm periphery device mounted on a carrier plate with dimensions of 8 x 9.5mm was analyzed, with the baseplate temperature set to 70C and a dissipated power of 14W. The total thermal resistance of the device, the solder attach, and the carrier plate was calculated to be 5.8 °C/W. The addition of a 1mil air gap between the carrier plate and the baseplate to simulate a possible worst case increased the thermal resistance to

22.6 ^{o}C/W. This led to a device channel temperature of 386^{o}C compared to 151 ^{o}C with no air gap. The maximum recommended channel temperature for this device is 200^{o}C.

Reducing the air gap to an area of 8 x 5.5mm (to simulate a bowed carrier with metal to metal contact only along the upper and lower edges) , resulted in a thermal resistance of 14.6^{o}C/W and a channel temperature of 274^{o}C. The thermal resistance and corresponding channel temperature were reduced to 7.2^{o}C/W and 171^{o}C by filling the partial air gap with thermal grease with a conductivity of 8W/mK.

This work underlines the importance of providing a very good thermal path from the device carrier to the baseplate, in order to avoid excessive channel temperatures.

Conclusions

GaN's higher power dissipation is causing users to reassess their thermal management requirements to ensure acceptable device reliability. To support this, finite element thermal analysis was used to investigate the dependencies of thermal resistance of GaN on SiC assemblies on a variety of variables. These variables included dissipated power, gate-to-gate spacing and overall periphery, baseplate temperature and even the attachment to the baseplate. Each variable dependence offered insight into the makeup of the overall thermal resistance and how the designer can manipulate each one to their benefit. This analysis has shown the importance of fully understanding the thermal stack up in order to accurately predict the expected junction temperature of the device and ultimately the corresponding reliability.

References

1. K. Decker, S. Ko and D Rosato, "Thermal Characterisation of Gallium Arsenide FETs", HDI Magazine, vol. 3 no. 12, December 2000

2. N. Killat, M. Kuball, T.-M Chou, U. Chowdhury, and J. Jimenez, "Temperature Assessment of AlGaN/GaN HEMTs: A Comparative study by Raman, Electrical and IR Thermography", IEEE IRPS Conference (2010)