# GaN Robust Receiver MMIC in X-Band – Process Optimisation and Circuit Results

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## Abstract

Excellent noise performance can be achieved using Gallium Nitride (GaN), circuit noise figures close to those achieved for GaAs devices have been reported. GaN offers additional benefits over GaAs: higher temperature operation, higher breakdown voltage and improved radiation hardness – making it an attractive technology for use in space-borne applications. Receiver components need to achieve minimum noise figure and high gain, but must also be protected against damage due to large signal inputs. This is ordinarily achieved by including a limiter device before the LNA circuit, typically diodes to clamp excessive voltage swings. GaN offers the potential to delete the limiter and therefore reduce component mass, cost and potentially improve overall system performance. This paper describes studies aimed at optimizing GaN processing technologies to simultaneously achieve low noise *and* robust devices for use in receiver circuit design. Initial small signal measurements are presented for an LNA design using a CPW GaN process. The LNA MMIC has been designed to withstand 10W CW input signal level.

## 1. Introduction

Excellent noise figure performance has been reported for wide bandgap semiconductor devices using a gallium nitride (GaN) material base. These devices are also well suited for operation at high temperature, high frequencies, high power and exhibit good radiation hardness. GaN devices are therefore very attractive for low noise space-borne receiver applications. The high voltage withstand capability of GaN can lead to considerably more robust components benefiting space systems by potentially eliminating the requirement for a limiter function before the low noise amplifier (LNA) device. In addition, simultaneous low noise and high voltage capability will allow integrated single function MMICs to be realised, leading to reduced size and lower cost transmit-receive (T/R) modules.

GaN technology has matured in the US and Asia and is rapidly becoming mature within Europe. Compared to GaAs, the three principal differences of GaN are (i) The 10x higher breakdown field of GaN and its alloys, (ii) the spontaneous and piezoelectric induced charges resulting in increased carrier concentration without doping, (iii) the state of the art GaN on SiC material has dislocation density up to four orders of magnitude higher than GaAs.

This paper describes studies performed using the QinetiQ GaN CPW MMIC process. The objective was to systematically vary key process parameters and assess it's impact on device robustness and microwave performance. The overall aim of this piece of work was to design, fabricate and test an X-band LNA MMIC with ~1dB

noise figure and capable of withstanding 10W cw overdrive at the input. Measured s-parameters and noise figure are shown for a preliminary LNA circuit design. In addition, a broad bandwidth feedback amplifier, designed at ESA, is also presented. Design considerations for MMIC operation under input signal overdrive are also discussed.

## 2. Process Optimisation Study

Robustness and noise optimization first needs a clear understanding and set of models for the primary failure mechanisms and noise processes. The input overdrive failure mechanism in LNAs has been little studied [1] but it is clear that there are two primary issues:

- Forward bias induced current flow across the gate Schottky diode leading to Joule-heating induced failure - forward current flow can be very effectively controlled by the use of a DC bias current limiting resistor [1]
- Reverse bias electric field induced degradation and failure at the Schottky gate corners - the reverse bias failure is the subject of intensive research but essentially protection amounts to limiting the electric field at the gate corners below some critical value [2, 3].

Process optimization simulations were performed using a physical device simulator (Silvaco ATLAS) to evaluate field distributions for various device geometries. The device simulations were used to generate s-parameters for each geometry. S-parameters were used to compile models for use in a microwave circuit simulator to assess device gain and noise performance based on the assumption that the fundamental noise processes were independent of geometry.

The following parameters were varied during the study:

- Gate position
- Gate geometry
- Gate length
- AlGaN layer thickness
- GaN cap thickness
- AlGaN composition

Optimization was based on a simultaneous minimization of the noise figure and the device electric fields.

## 2.1. ATLAS Physical Device Simulations

Studies performed using ATLAS were based on the parameterized device layout shown in Figure 1.

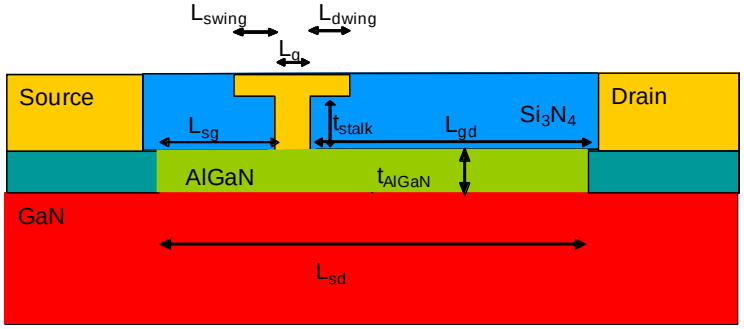


*Figure 1. Schematic diagram of the device structure used for ATLAS modeling – showing parameters varied during process optimisation.*

The ATLAS simulator requires several device and material parameters to be estimated. Key parameters include device thermal resistance (from a 3D thermal model of the device), AlGaN polarization charge, mobility, contact resistance and saturation velocity. Model calibration was undertaken using measured results for a nominal device.

Models developed using ATLAS allow the critical electric fields to be extracted for various sets of parameters. Figure 2 shows the E field distributions for 3 gate voltage conditions. In the figure Ex_chan is the field in the conducting channel in the direction of current flow, Ex_surf is the surface field also in the x-direction, Ey is the field lateral to the channel and at the peak field region at the gate edge. An infinite field strength (as expected for a sharp corner) far exceeding the breakdown field in bulk AlGaN of ~3MV/cm is calculated at the gate edge. However in practice this peak field will be reduced due to rounding of the gate corner, the use of GaN cap layers, and charge screening due to trapping in the passivating dielectric, all of which are difficult to quantify. Hence optimisation is based on the pragmatic solution of monitoring the field a few nm away from the gate corner. Most reported device simulations focus on the lateral field in the channel, Ex_chan. This is a key parameter for power amplifier operation, but is less important for the LNA application although gate leakage current can still potentially lead to bulk trap induced degradation.

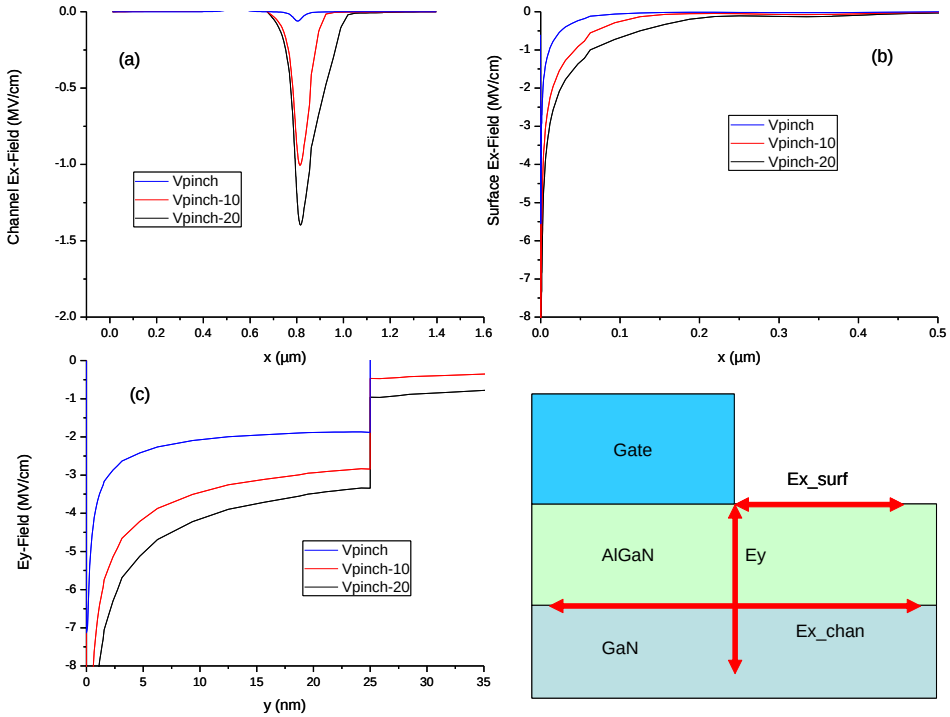


*Figure 2. Field distributions through devices at pinch-off and large reverse gate voltages. x=0, y=0 corresponds to the position of the gate edge*

ATLAS simulations can be used to provide a good qualitative comparison of the role each parameter plays in the variation of field levels in the devices as the parameters are varied.

Another key input failure is a gate current driven device degradation or thermal failure. These effects can be determined empirically and lead to a specification for a hard limit for forward gate current density for the process.

### 2.2 Device Microwave Models using Agilent's ADS

The next step was to generate scalable device models suitable to assess the device performance for robust LNA circuit applications. This was done using the following approach:

- Using ATLAS s-parameter data for a single device finger, construct multifinger device models. Scalable gate resistance and manifold parasitics were extracted and added.
- Add device geometry independent noise generators corresponding to a constant device noise temperature
- Vary the fitting parameters above to achieve a good fit for a standard device simulation and measurement

An example of measured and modeled s-parameters and minimum noise figure (NFmin) are plotted in Figure 3 and Figure 4 respectively. S-parameter measurements are included for an 8 finger device. Reasonable agreement is observed between measured and modeled data where models are built both using ATLAS derived single fingers and from small-signal models extracted for the fabricated device. In Figure 4 measured and modeled NFmin is shown for three gate bias conditions. The model yields a good match to measurement.

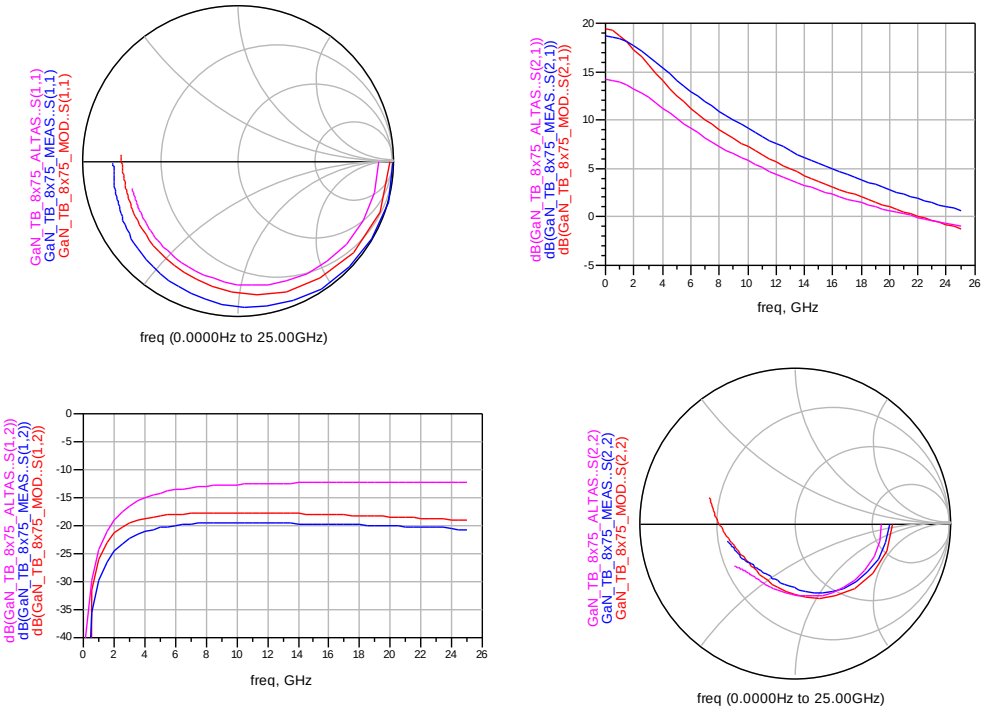


*Figure 3. Comparison of measured (BLUE) and modeled data for an 8x75 μm device. PINK data is for a multifinger device constructed using single finger cells modeled using ATLAS. RED data is a model extracted directly for the multi-finger device*

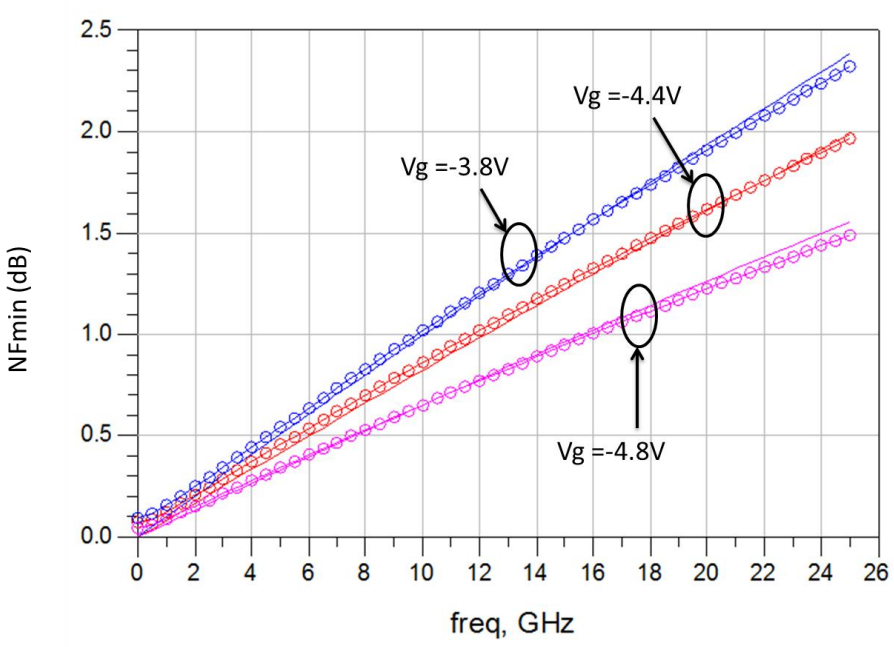


*Figure 4. Measured and modeled NFmin for -4.8, -4.4 and -3.8 V gate voltage. Model extracted for a 2x75μm device based on s-parameters derived from ATLAS single finger device models. Modeled data corresponds to the open circles.*

## 2.3 Impact of Variations on Device robustness and Noise Performance

A comprehensive series of simulations were performed for various device parameters and geometries. A comparative summary of the predicted change in the peak gate fields ($E_{max}$), used to assess robustness, and the simulated device noise performance are given in Table 1. The range over which the parameters have been varied are indicated. The impact on processing complexity and therefore process cost and yield is not the same for each of the parameters listed in Table 1.

| **Parameter** | **Nominal value and Range simulated** | **Change in $NF_{min}$ (dB)*** | **Change in $E_{max}$*** |
|---|---|---|---|
| AlGaN thickness | 10-50 nm<br>[25 nm] | -0.15 for 10 nm<br>+0.4 for 50 nm | Increased $E_{chan}$ with reduced AlGaN thickness |
| Gate position | $L_{sg}$ 0.75, 1.15, 1.55, 1.95 µm<br>[1.15 µm] | -0.1 (0.75 µm)<br>+0.3 (2.75 µm) | Weak effect |
| Gate length | 0.15, 0.25, 0.35µm<br>[0.25 µm] | -0.1 (0.15 µm)<br>+0.1 (0.35 µm) | No effect |
| Gate geometry | 0.1-0.3 µm stalk, 0-0.5 µm wing<br>[0.15 µm, 0.25 µm] | +0.1 (0.3 µm stalk, 0.5 µm wing) | Field plate effect for $t_{stalk}$< 0.2 µm |
| Gate Au plating thickness | 200 to 600 nm<br>[300 nm] | - 0.25dB (300 nm to 500 nm, with 0.3 µm stalk, 0.25 µm wing) | No effect |

*Table 1 Summary of transistor optimisation study findings showing impact on noise performance and peak field levels (*with respect to baseline device parameters shown in square brackets)*

A brief discussion of each summary conclusion is given below:

<u>AlGaN Thickness</u>
Varying the AlGaN layer thickness has a large effect on the device transconductance ($g_m$) and also the pinch-off voltage. Thinner AlGaN layers result in higher device gain and lower noise figure as indicated in Table 1. In addition it will increase the field in the channel, making devices with layers too thin more susceptible to hot electron damage. It is becoming common practice to include a thin GaN 'capping' layer on top of the AlGaN. The GaN cap reduces the field at the gate corner, but the cap thickness and Al concentration in the AlGaN needs to be adjusted to maintain sufficient carrier concentration for gain and noise performance.

<u>Gate Position</u>
The gate position in the source-drain gap determines the value for the source resistance, $R_S$ – which in turn impacts the gain and noise performance achievable as indicated in Table 1. Gate position has negligible effect on the peak fields simulated, although very narrow gaps will lead to reduced process yield and higher likelihood of surface field breakdown effects (not simulated in this study).

<u>Gate Length</u>
Processes using reduced device gate length are well known to yield higher cut-off frequencies, increased gain at 10 GHz and hence reduced noise. Electric field simulation showed no impact on the peak gate corner fields with gate length.

However, shorter gate length reduces the gate stalk area making it more vulnerable to forward current induced damage.

Gate Geometry

Changing the T gate geometry has a dramatic effect on the device robustness. The primary impact on device robustness arises due to the field-plating effect of the T-gate wings on the fields at the gate edge. Essentially, the wings of the gate insert transistors with low gain and large negative pinch-off voltage in series with the main gate. Once the gate reverse voltage exceeds the pinch-off voltage under the wings, a large degree of protection is afforded to the main gate. This effect is illustrated in Figure 5 where it can be seen that as the stalk height is reduced the E field strength at the gate wing edge increases, resulting in a sharing of the total voltage drop at the gate, therefore reducing the peak field near the gate edge. However, In general, measures such as this which increase the robustness lead to a degradation in the device rf performance - so a compromise needs to be established. For instance, the ATLAS derived $F_T$ drops by 9% and 32% respectively as the stalk height is reduced from 300 to 200 and then 100nm for the geometries in Figure 5.

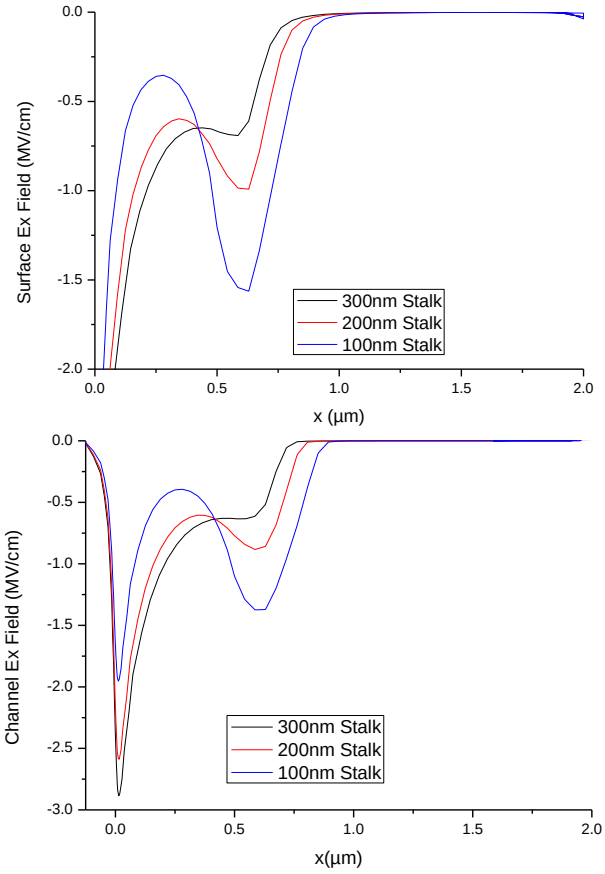


*Figure 5. Field distributions on the drain side of the gate (x=0 is the drain edge of the gate) for various gate stalk heights at -80V reverse voltage. The peak in electric field transfers from the gate corner to the T-gate edge as the gate stalk height is reduced. Gate overhang is 0.5µm.*

Gate Gold Plating Thickness

The device series gate resistance, $R_g$, has a large impact on the $NF_{min}$ that can be achieved. Using the ADS model for the baseline device extracted as described above, simulations of $NF_{min}$ were performed for $R_g$ ranging from 0 to 10 Ω. Over that range of $R_g$, $NF_{min}$ varies between 0.9 and 1.7 dB. For a given gate process,

multifinger device total gate resistance can be optimized using parallel, small unit gate width fingers, and by maximizing the gate metal thickness/surface area. For a simple T-gate section, with equal 0.25μm gate wings, increasing the plating thickness from 0.3 to 0.6 μm translates to a 30% reduction in $R_g$.

## 3. MMIC Circuit Designs

MMIC circuits were realized using the QinetiQ 0.25 μm gate length CPW GaN process which was the process which was used to demonstrate MMICs for the Korrigan project [4,5]. Design kits including active device and passive models, developed for the Korrigan project were used as a base-line for the robust LNA designs described here.

A second circuit design was completed by ESA as a means to potentially characterize the process. Layouts and measurements for the feedback circuit implemented are given in this section.

### 3.1 LNA Circuit Design and Measurement

A key consideration for circuit robustness is the total device gate periphery. Choosing the device configuration, especially for the LNA first stage, requires a device to be selected that can sustain the anticipated gate current, E field levels and also provide the optimum noise performance. Estimating the gate current and device terminal voltages requires a non-linear device model. Non-linear vector measurements can also be used to extract these parameters directly from measurements [6].

An overall circuit noise figure and gain of <1.5 dB and >18 dB respectively can be achieved using the two-stage circuit line-up illustrated in Table 2. This performance is typical of GaN technology. Comparing the required device noise and gain performance, and based on an estimate of device robustness, a 4x75 μm device was used for the first and second stages of the LNA MMIC.

| **Device** | Input Match | Stage 1 | Interstage | Stage 2 | Output match |
|---|---|---|---|---|---|
| **Gain (dB)** | -0.5 | 12 | -0.5 | 8 | -0.5 |
| **NF (dB)** | 0.5 | 0.8 | 0.5 | 0.8 | 0.5 |
| **Cum. Gain (dB)** | -0.5 | 11.5 | 11 | 19 | 18.5 |
| **Cum. NF (dB)** | 0.50 | 1.30 | 1.33 | 1.38 | 1.38 |

*Table 2. MMIC line-up estimates*

A photograph of the completed LNA MMIC is shown in Figure 6. The two stage circuit uses the same 4 x 75 μm devices in each stage, with source degeneration applied using spiral inductors to aid simultaneous optimum noise and gain matching. Thin film resistor, metal-insulator-metal capacitors, spiral inductors and parameterized CPW lines are all available using the process PDK. A small signal model for the 4 x 75 μm device geometry was not available at the time the MMIC was designed. Data and models for two 2 x 75 μm devices were combined using ADS.

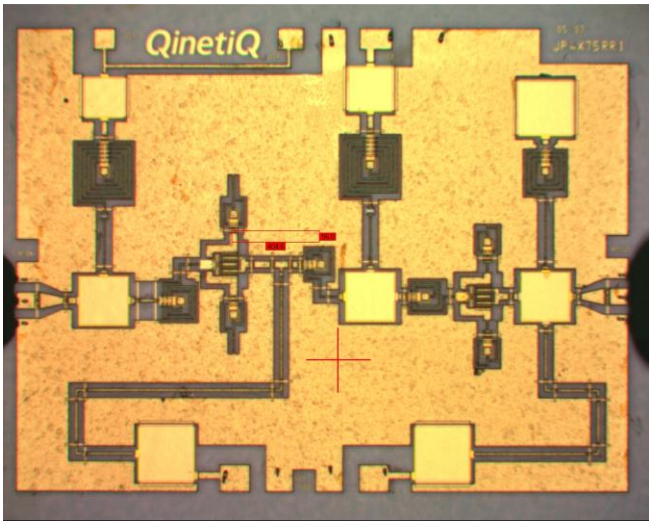


*Figure 6. Photograph of the GaN LNA MMIC*

### 3.1.1 LNA Circuit Small Signal Simulations and Measurement

Small signal S-parameters are shown in Figure 7 and Figure 8. Measured and modeled s-parameters are plotted – measurements are included for several gate bias conditions. Reasonable agreement is observed between measurement and modeling. Differences observed, in particular in S11, arise largely due to the active device model being approximated by two combined 2 x 75 μm devices. A further circuit iteration would be expected to yield the targeted gain over a bandwidth of 5 to 11 GHz.

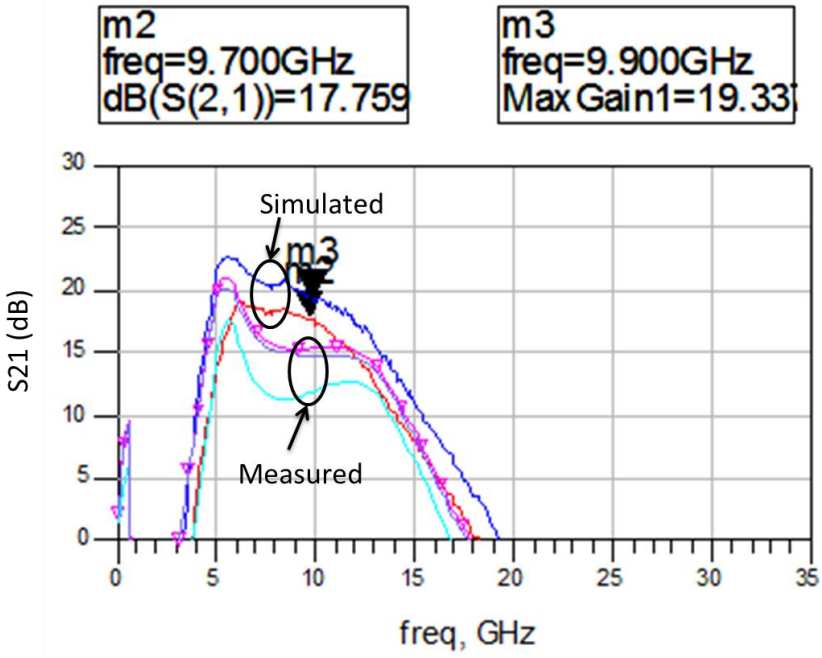


*Figure 7. Small Signal Measured (for various gate bias conditions) and Modeled Data for the GaN LNA MMIC – S21*

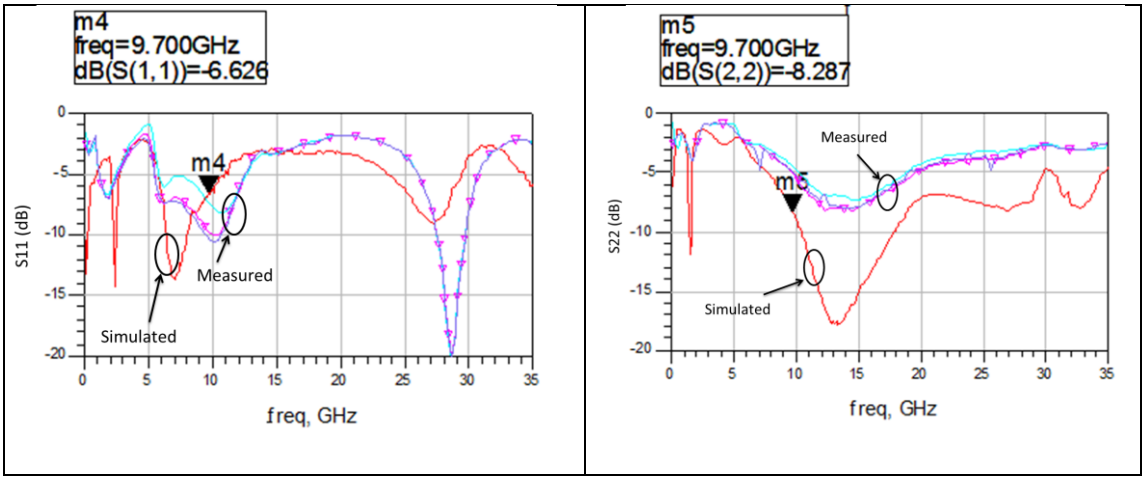


*Figure 8. Small Signal Measured (for various gate bias conditions) and Modeled Data for the GaN LNA MMIC – Port Matches*

Noise measurements are shown in Figure 9. A noise figure of around 2 dB is measured in the 5 to 10 GHz frequency range. A state of the art GaAs LNA would be expected to have noise figure better than 1 dB at 10 GHz. For this GaN MMIC, increased noise arises, in part, from the choice of a larger unit gate width device for robustness considerations – as discussed above. The GaN MMIC noise figure must be compared to the noise performance of the combined GaAs MMIC *and* limiting circuit.

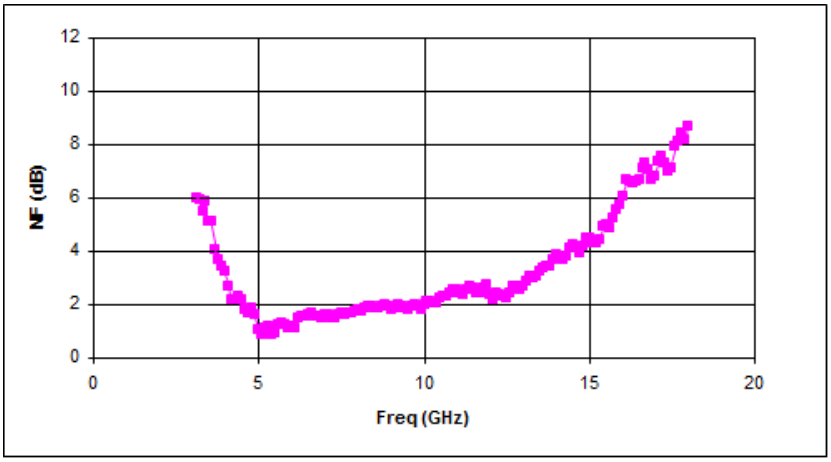


*Figure 9. Measured noise figure for the GaN LNA MMIC*

### 3.1.2 LNA Simulations of Device Overdrive

The MMICs have not been tested under large signal conditions at the time of writing this paper. For completeness, a non-linear simulation for a device is included in Figure 10. This figure illustrates a key tradeoff in use of a series gate resistor. Larger values of $R_g$ limit the gate current, but also increase the voltage at the gate.

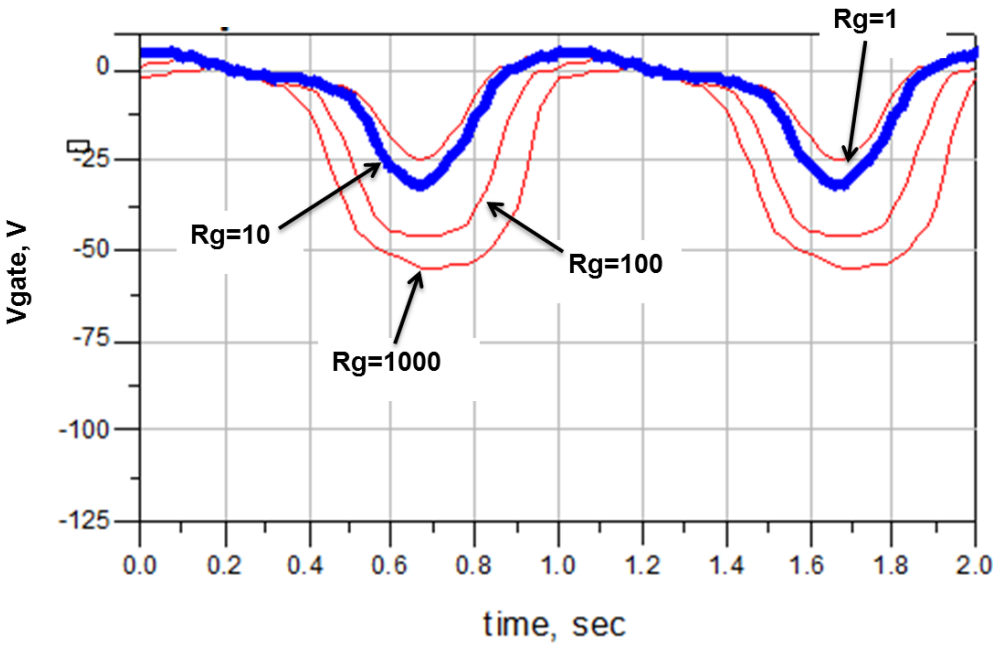


*Figure 10. Large Signal Simulations of Gate Overdrive as the value of a series gate resistor is varied bold line is for $R_g$ =10 ohm*

| Series Gate resistor ($R_g$) [ohms] | DC gate current ($I_g$) [mA] |
|---|---|
| 1 | 380 |
| 10 | 300 |
| 100 | 140 |
| 1000 | 40 |

*Table 3. Values of series gate resistor Rg and corresponding DC gate current derived from non-linear device simulations*

### 3.2 Feedback Amplifier Circuit Design and Measurement

The broadband (> octave) feedback amplifier, shown in Figure 11, was designed based on an 8x75um device. The MMIC has on-chip biasing structures. Several test structures were also included in the MMIC test cell by the ESA designer for process verification.

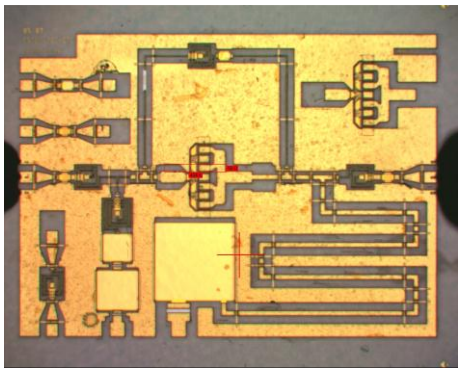

*Figure 11. Photograph of GaN feedback amplifier MMIC designed at ESA*

Measured s-parameters for the feedback amplifier MMIC are shown in Figure 12. Very good agreement is achieved between measurement and modeling. Greater than 7.5 dB gain is achieved over 2 octaves.

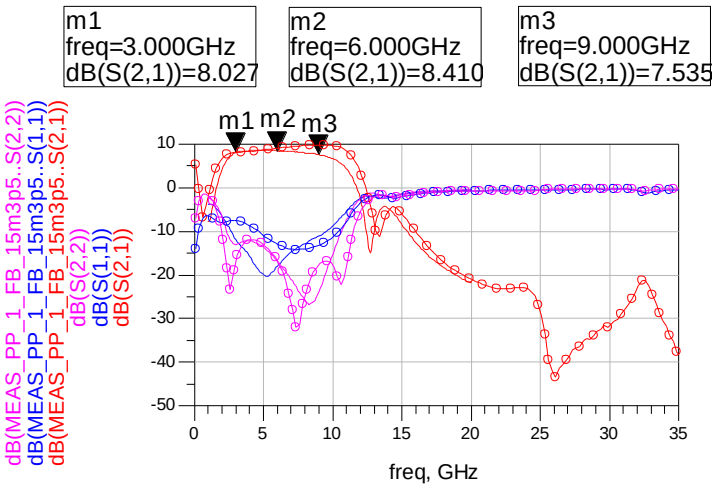


*Figure 12. Simulated (circles) and measured (no circles) s-parameters for the feedback amplifier*

## 4. Conclusions

The methodology for improving the robustness and at the same time retaining noise performance for GaN low noise amplifiers has been described. A test circuit implementing some of these approaches has been fabricated and demonstrated to have good noise performance. In addition, feedback amplifier has been demonstrated displaying wide bandwidth performance.

## 5. Acknowledgements

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