Power Amplifier devices for UMTS

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When developing power amplifiers for use in UMTS basestations it is vital to make the right choice for the final power device(s). This paper outlines the impact of the 3GPP specification for base stations on the power amplifier, determines tests and benchmarks to enable device comparison, and discusses how device characteristics can influence the rest of the system.

INTRODUCTION

The power amplifier stage of a typical cellular basestation represents a high proportion of the overall unit cost, this in part is due to the high cost of the power transistor used to generate the final output power, therefore a key decision for the designer is: 'how many transistors?' too few and the spectral requirements will not be met, too many and the efficiency will suffer and the cost will be excessive, this is true regardless of any linearity enhancement scheme surrounding the amplifier power stages. The other key question that must be answered is: 'What technology will achieve the required goals?' here the usual choice is between LDMOS and GaAsFET, and can only be answered by device testing against a common benchmark.

This paper attempts to:

- Detail the requirements of the power device based on the 3GPP specification.
- Derive a test suite for characterising devices to enable common comparison.
- Detail device demoboards and test boards.
- Present typical results.
- Discuss results and draw conclusions that impact the overall architecture.

REQUIREMENTS

The bottom line for the spectral requirements of a UMTS basestation is detailed in (1) from this the requirements for the power amplifier must be drawn, and then finally given knowledge of the performance of any linearity enhancement scheme employed, the requirements for the power stage. Within the 3GPP specification there are 4 power output classes defined ranging from > 43dBm total power output down to < 31dBm. These power classes modify the spectrum emission mask that the basestation must comply with.

So to make the first key decision one must determine how much power the power transistor(s) need to generate. First, the basestation power output must be decided. Second, knowledge of all losses following the final transistor(s) must be known, and third, how much improvement does the linearity enhancement scheme give. It is assumed here that all 3GPP compliant power amplifiers will employ a linearity enhancement scheme, because unfortunately transistors are not yet linear enough on their own, although there is hope with techniques like 'Derivative Super-position' (2)(3) and other potentially more linear structures like GaN. Typical linearity enhancement schemes used today include feedforward and digital pre-distortion.

Not all the above questions can be answered at the start of a project; therefore all devices short-listed must be tested over a range of output powers.

CHARACTERISATION

To make an informed decision as to the correct number and type of devices, one must gather data for all devices that might be suitable. The first port of call is the manufacturer datasheet; these vary a lot in quality and can really give the designer a hard time as quite often each manufacturer uses tests that do not cover your particular requirements. This has historically been very true of datasheets for UMTS transistors for several reasons; (a) the 3GPP standard has been around for a several years and has only recently been frozen, thus parameters change, (b) test equipment manufacturers have done their best to keep up with the standards but inevitably there has been a lag, thus different test equipment give different results, (c) the specification gives several options for the modulation, for example when measuring spurious emissions there is a choice of three formats depending on what the basestation will support, which can affect the measured performance.

So inevitably this means that the designer must determine a set of tests, which will provide all the information necessary to make the final decision.

Datasheet information usually includes the following information that is useful to the designer:

- Single carrier Adjacent Channel Leakage Ratio (ACLR) versus output power.

- Two carrier ACLR and 3rd Order Intermodulation Distortion (IMD) versus output power.
- Optimised source and load impedances (useful for the test circuit).

However quite often the modulation used for the measurements is not fully described in terms of statistics, or varies between manufacturers, or worse still, not even stated, necessitating re-measurement to a common standard. In some cases the designer may have a special modulation employing clipping algorithms, which would have to be used.
In addition to the above data, the designer would also want to characterise the following parameters using a test circuit or demoboard:

- S parameters over frequency.
- Gain and phase compression.
- 2 carrier CW IMD products, 3rd, 5th, and 7th at least.
- Sensitivity to variation in Idq.

To make these measurements repeatable and to remove the drudgery it is essential to automate the process as much as possible. At RMRL a suite of programs have been written using Agilent VEE, which has enabled a database of over 300MB to be generated for a broad spectrum of parts.
As well as spectral, (1) also contains other requirements that relate to the wanted signal modulation quality, namely Error Vector Magnitude (EVM), and Peak Code Domain Error (PCDE), both defined in section 6.7 of (1). These requirements are very important as they relate to the overall bit error rate for the base station transmitter. The power amplifier will contribute to the overall figures of EVM and PCDE, but measurements have shown that if the power amplifier meets the spectral requirements then the linearity is sufficiently good such that the contribution to signal modulation quality will be negligible. Therefore swept measurements of EVM and PCDE versus power output do not necessarily need to be included in the test suite.

W-CDMA TEST SIGNAL

Within the 3GPP specification, there are options as to the modulation format, these are referred to as *'test models'*. There are basically 4 different test models, each used for specific tests, in the case of ACLR and spurious emissions the relevant test model is Test Model 1, defined in (1) 6.1.1.1. However within this test model there are 3 options; 16, 32 and 64 DPCH (Dedicated Physical CHannel) or 'users', this results in a spread spectrum signal which exhibits a high peak to mean ratio dependant on the option chosen. Figure 1 plots the theoretical Complementary Cumulative Density Function (CCDF) for each option. It shows that there is about 1dB difference in absolute peak power between each option. This can affect the test results, therefore for repeatability reasons, one option should be standardised on. At RMRL the 64 DPCH has been decided on as this stresses the transistor to the maximum.
In most base stations a clipping algorithm is employed in DSP at the baseband stage to reduce the maximum peak of the signal in order to reduce the stress on the power amplifier, allowing it to provide more power and hence better efficiency. However when choosing devices it is better to consider testing using an unclipped waveform since this represents a worse case scenario. Results should only improve with clipping. It adds a safety margin for the designer, and provides protection from changes to the actual clipping algorithm.

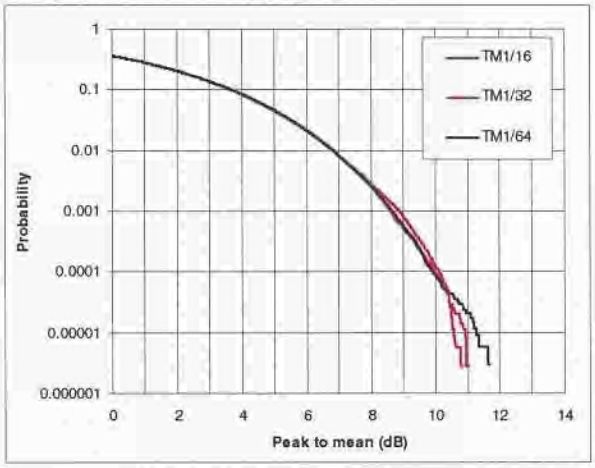

Figure 1: Test Model 1/64 CCDF curve

TEST BENCH

For testing high power devices a special test setup is required comprising:

- A high power dc supply.
- 2 x W-CDMA capable signal generators, e.g. Agilent ESG or Rohde and Schwarz SMIQ.
- 2 x High power class A driver amplifiers.
- Isolators.
- High power directional couplers.
- High power attenuators.
- 2 x power meters.
- High dynamic range spectrum analyser with rms detector and ACLR measuring capability e.g. Rohde and Schwarz FSIQ.

A typical test setup is given in Figure 2 below:
Note that the two tone signal is generated by combining at high power, and note the use of isolators, both measures ensure that source IMD is negligible. The whole test set-up must be carefully calibrated for loss with a network analyser to ensure accurate measurements since a loss of 0.2dB already represents 1W in 20W.
Note also that (1) 6.1.1.6.3 states that each modulated carrier shall have a different scrambling code, incremented from 0 starting with the lowest carrier frequency, there shall also be 1/5 time slot offset between their frame structures. This again will make a minor

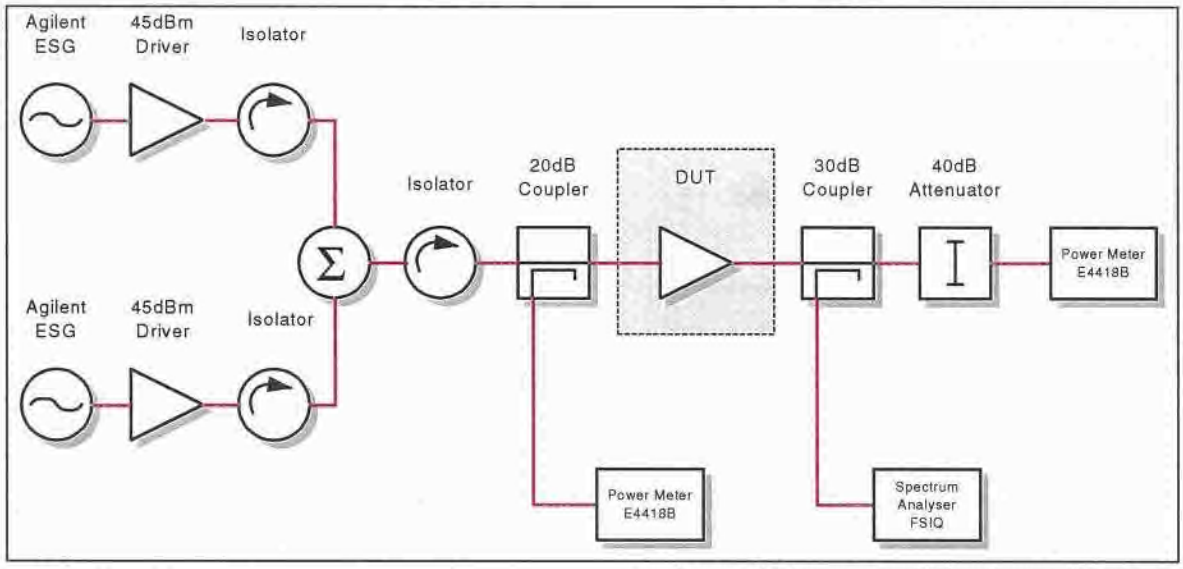

Figure 2: Typical IMD/ACLR test setup

difference to the composite peak to mean ratio and should be included as part of the test setup.

BENCHMARK TEST

If certain assumptions can be made about system performance it is possible to generate a 'benchmark' test that allows easy comparison of devices. The first step is to extract the most demanding requirement from (1), the situation changes depending on the number of carriers the amplifier is required to pass. With one carrier there are no discrete IMDs to worry about and the most stringent spectral requirement is the out of band emission found in (1) 6.5.2.1.2, this is illustrated in Figure 3, also shown are the less stringent requirements of ACLR. It can be seen that the requirement level in dBm is –28.2dBm/30kHz, given a 43dBm carrier this translates to –50.2dBc.

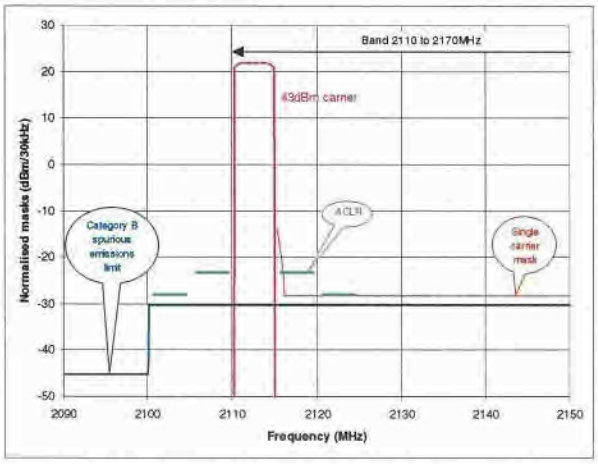

Figure 3: Single Carrier UMTS spectrum requirements

However, most amplifiers are designed to handle at least two carriers and in this case the most stringent requirement is the category B Spurious emission mask found in section 6.5.3.4.2. This requirement is considerably tougher than ACLR or out of band emission for one or more carriers. Figure 4 below shows a composite plot of the spectral requirements assuming a 2 carrier transmitter at the bottom of the frequency band 2110 to 2170MHz. The carrier spacing for the 2 carrier signal is 15MHz, this means that the lower third order IMD product will fall at 2097.5MHz and will be required to be below the –45dBm/30kHz category B mask limit.

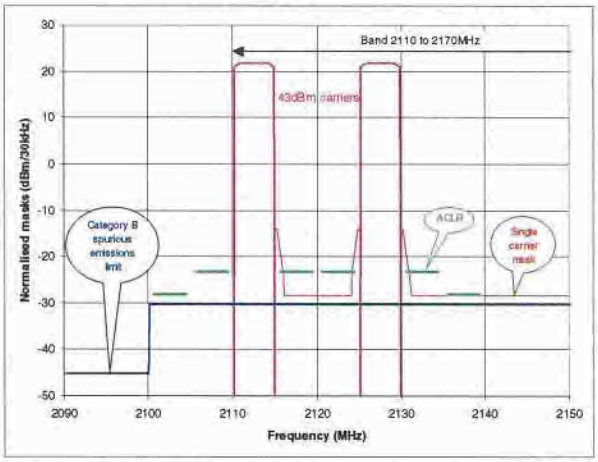

Figure 4: Two carrier UMTS spectrum requirements

Translated to dB relative to a 43dBm carrier results in a level of –67dBc. In order to generate a benchmark IMD level for the power stage, the losses at 2097.5MHz relative to the wanted band e.g. duplexer filter, plus the linearity scheme enhancement must be subtracted from the -67dBc figure. In practise a general figure of about –35dBc results.

TWO CARRIER BENCHMARK:	
Total 3GPP requirement =	-67dBc
Linearity improvement scheme =	20dB
Duplexer out of band loss*=	10dB
Margin =	2dB
Power stage IMD level =	**-35dBc**

* K&L WSD-00189 UMTS duplexer

The linearisation improvement figure of 20dB suggests that a feedforward system is required to produce a compliant multi-carrier amplifier.

DEMOBOARDS AND TEST BOARDS

The quickest route to characterising a device is to obtain an application demoboard from the transistor manufacturer. The demoboards are designed to be as flexible as possible and adjustable tuning elements are often included for optimisation. The user can therefore optimise the demoboard to some degree for their particular application. However it is necessary at some point to make your own board customised to your application and manufacturing philosophy.
Sometimes the delivery of a demoboard is either outside of your timescales or simply not available, in this case it is necessary to make your own board from the outset. Designing your own test board for a high power transistor is at first a rather slow process as there are significantly more steps involved compared to say a small signal device, in particular with regard to the mechanical and heatsinking arrangements. The typical tasks involved include the following:

- If gerber files for a test board can be obtained from the manufacturer, use them!
- No gerber files, then hopefully obtain the manufacturer declared optimum source and load impedances, decide what they mean and use them as a starting point for matching circuits.
- Design the test board including bias networks.
- Design the heatsink and / or baseplate.
- Have all parts manufactured.
- Build the pcbs and assemble the completed test board onto the heatsink.
- Test the test board, and tune up if necessary.
- Compare the results against the datasheet.

Figure 5 is an example of a test board for a Motorola MRF 21125 based on manufacturer supplied data, it is part of a family of test boards all designed around the same heat sinking and biasing arrangements in order to speed up development of a test board for a new device. It can be seen that the gate and drain circuitry can be rapidly removed and replaced in order to experiment with different matching circuits. The gate bias circuit is also on a separate board for the same reason, however this is only a temporary solution as the gate bias circuit should really be thermally connected to the power transistor in order for the transistor Idq to be correctly thermally compensated. Note also that the power transistor is not soldered, this is only acceptable for a test board, where devices are to be compared, soldering makes this hard work.

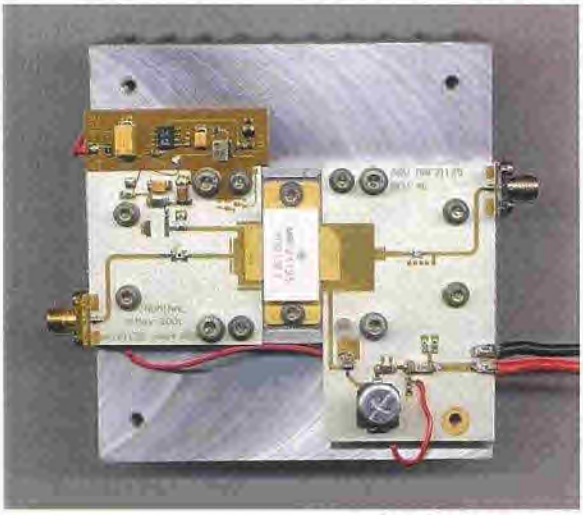

Figure 5: Typical power device testboard

TYPICAL CHARACTERISATION RESULTS

Figure 6 below shows small signal gain curves over a frequency sweep of 500MHz centered on 2140MHz. It compares a typical demoboard against another transistor of the same family optimised for flat gain. Flat gain is important for manufacture repeatability as a 'peaked' response is more sensitive to component tolerances.

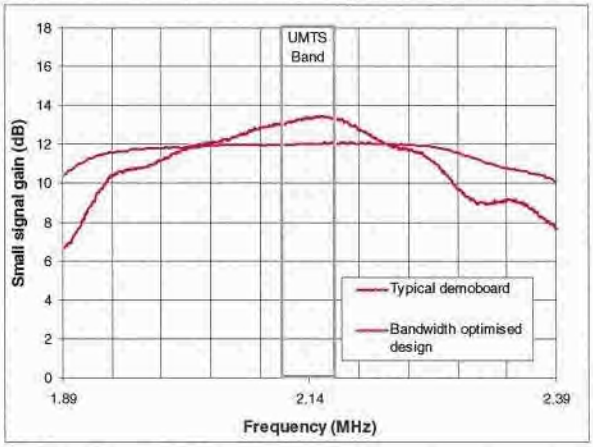

Figure 6: Small Signal Gain

Flat gain (and phase) over frequency is also a very important characteristic when linearisation is employed. In the case of a feedforward system the amplitude (and

phase) ripple limits the amount of improvement that can be obtained over a given bandwidth.
The amount of improvement or cancellation is given the equation below found in (4):

$$S := 10 \cdot \log\left[\left| 10^{\left(\frac{A}{10}\right)} + 1 - 2 \cdot \left[10^{\left(\frac{A}{20}\right)} \cdot \cos(\phi) \right] \right| \right]$$

Where A is the amplitude ripple in dB, and ϕ is the phase ripple, both over the bandwidth of interest. Taking the two devices above over a bandwidth of 15MHz, and 60MHz, and the following cancellation figures result assuming the phase ripple for both devices were equal to zero:

	Device	
Carrier spacing	**Standard demoboard**	**Optimised device**
15MHz	-33.70dB	-64.80dB
60MHz	-25.76dB	-38.48dB

Compared to the 2 carrier benchmark described earlier where 20dB is required from the linearisers, the standard demoboard would cause severe limitations as carrier spacing is increased as on its own would consume nearly all the budget just due to gain ripple. The figures will be worse if phase ripple were included. The output stage considered here will be only one part of the complete amplifier line-up and the way the S21 of all the devices interact would have to be carefully considered.

Figure 7 below shows a typical plot of power gain and phase versus input power level. The amplifier compression at the higher power levels can be clearly seen.

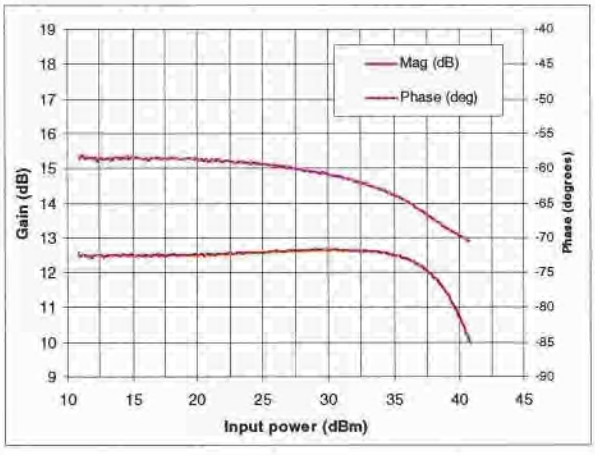

Figure 7: CW power sweep

The absolute gain and shape of the compression curve is related to the quiescent current (Idq) of the transistor which for a class AB stage will be in the region of 10% of Id max. It is important to set the optimum Idq for best efficiency and linearity. Linearity is strongly affected by Idq due to the gain peaks as the device approaches saturation, these cause so called IMD 'sweet spots', the gain peaks are a form of build-in pre-distortion giving a little gain expansion. The gain response can also interact with the phase curve to give the same result. If the transistor manufacturer had better control of the device transconductance curve then maybe we might see improved transistors and the goal of a class AB amplifier without an external lineariser might be achievable.
It is still useful to plot the gain and phase of a transistor versus power level, but is not ideal for optimising linearity, it is far better to adjust Idq whilst observing IMD directly.

As mentioned above Idq has a strong effect on the linearity of a device, this can be easily observed in Figure 8 which shows 3rd order IMD levels versus average power output from a typical LDMOS device as Idq is varied. For this particular device the optimum Idq under CW excitation is about 1.30A. Similar plots could be drawn for 5th and 7th order products, however generally 3rd order is dominant and so optimising Idq for this order is normally adequate. Note for this device the dip in IMD or 'sweet spot' at 40dBm output level at an Idq of 1.3A.

Characterisation using CW is very useful for carrying out an initial comparison of devices and optimisation, however the performance will change considerably under W-CDMA excitation due to the high peak to mean ratio and spread spectrum characteristics of the signal. Figure 9 shows ACLR versus output power for the same device as shown in Figure 8. By comparison the following points can be drawn:

- At high power ≈45dBm, the IMD/ACLR levels are similar and the amplifier is driven well into compression by the peaks of the signal.
- With W-CDMA the 'sweet spots' have disappeared.
- Significant 'memory effect' or ACLR imbalance is evidence with W-CDMA as power is backed off.
- At high Idq where the device is getting closer to class A bias, the back off curve with W-CDMA retains the shape seen with CW, albeit at an overall lower level.
- The optimum Idq setting for single carrier W-CDMA has increased to ≈1.6A.

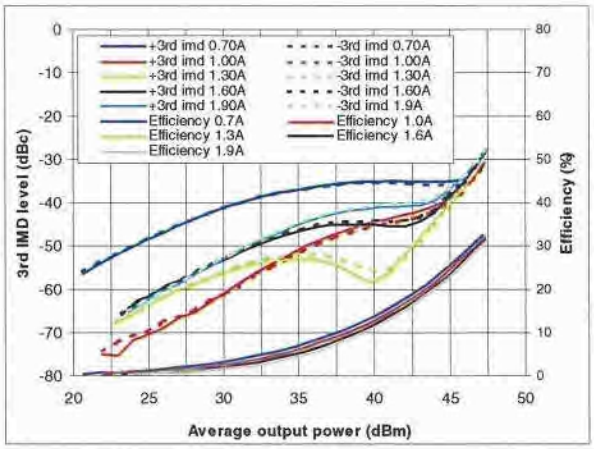

Figure 8: CW IMD versus Idq

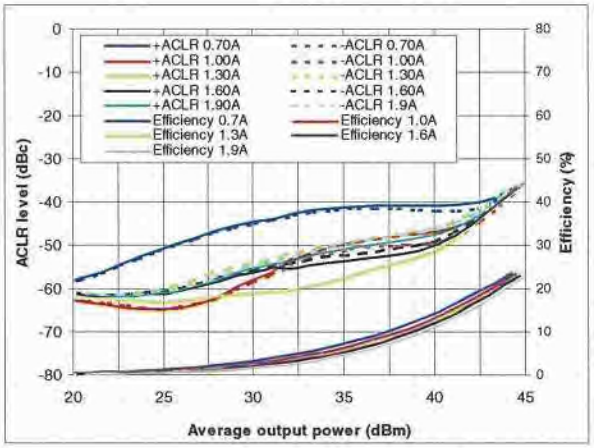

Figure 9: ACLR with 1 x W-CDMA source

ACLR with a spread signal is really a composite of 3rd, 5th, 7th etc orders of IMD products added together over the complete range of baseband frequencies, or like a closely spaced multi-tone CW signal, thus it is no surprise that the plots seen in Figure 8 and Figure 9 are so different.

Now consider the case of a two carrier W-CDMA signal applied to the same amplifier, see Figure 10 and Figure 11 below.
In Figure 10 the plot of 3rd order IMD it can be seen that the 'sweet spots' have reappeared, but there is significant 'memory effect' with more than 10dB IMD imbalance noted at some power levels. This points to poor design of this particular demoboard supplied as is from the manufacturer.

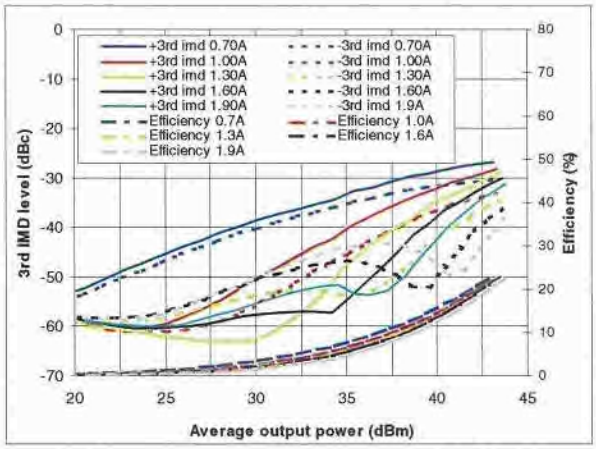

Figure 10: IMD with 2 x W-CDMA source

Here we see:

- 'Sweet spots' very sensitive to Idq.
- Large memory effect.
- Optimum Idq now ≈ 1.9A (at 2 carrier benchmark –35dBc).

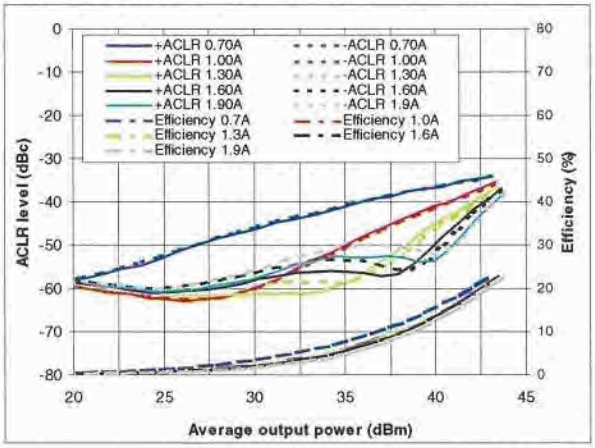

Figure 11: ACLR (lower carrier) with 2 x W-CDMA source

Figure 11 shows the ACLR plot for the same 2 carrier W-CDMA input signal, but just considering the lower of the two carriers, in practise the other carrier will exhibit essentially the same set of curves. The plots are significantly different to the single carrier case shown in Figure 9, however with two carriers the absolute peak to mean ratio will have been modified to perhaps 12dB so this is no surprise.
Here we conclude:

- ACLR with two carriers is significantly lower in level compared to 3rd order IMD (5dB or more at high power), therefore less important. Normally improving the 3rd order IMD to meet specification will automatically ensure ACLR is acceptable.
- Optimum Idq is again ≈ 1.9A.

IMPACT OF MEMORY EFFECT

As observed Figure 10, this particular demoboard exhibited quite different memory effects under 2 carrier CW conditions compared to 2 carrier W-CDMA conditions: in the CW case hardly any memory was observed and in the W-CDMA case up to a very poor 10dB was noticed.

If 10dB IMD imbalance exists at the benchmark level then the implications are that if the higher of the two IMDs is enhanced by the memory effect whilst the other is cancelled then the amplifier is not providing the power it could if there were no memory effect. This means that with a feedforward amplifier either the correction has to work harder or the amplifier has to be backed off more with the hit on efficiency. Neither case is desirable.

Memory effect can also cause big problems with digital pre-distorting linearisers as independent coefficients to control each IMD product is not available and thus one IMD could be improved at the expense of the other, or just a generally poorer performance results. More recently digital techniques at RMRL have been developed to overcome these limitations. Therefore it is important for multicarrier amplifiers that the memory effect be characterised.

Memory effect can be explained in different ways, one useful way described by Steve Cripps in (5) is "a time lag …between AM-AM and AM-PM responses", this can be introduced by poor gate and drain decoupling at low frequencies causing a distortion of the envelope currents which results in IMD asymmetry. This is really only applicable to reduced conduction angle amplifiers like class AB where drain current varies with output power, this is seen in the plots above and note that as Idq is raised towards class A bias, memory effects reduces.

The 2 carrier CW IMD plot does not show up the memory effect very well because the carrier spacing used was only 1MHz. Better evidence will be seen if the carrier spacing is varied between 1MHz and about 15MHz which represents more closely the range of envelope frequencies with a 2 carrier W-CDMA signal. Figure 12 below shows a typical family of curves measured with a carrier spacing varied between 1 and 15MHz, here large amounts of IMD imbalance are observed as the carrier spacing is varied.

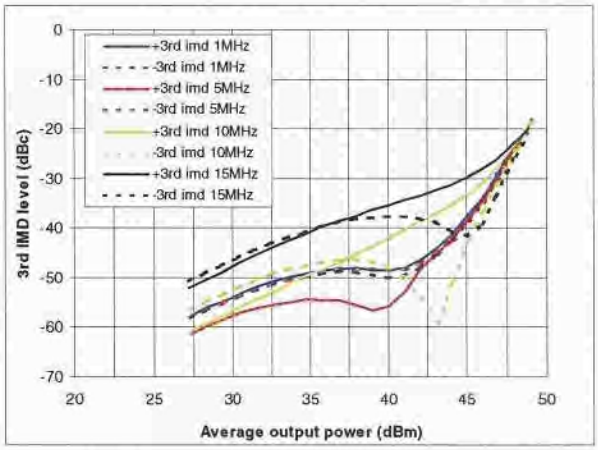

Figure 12: 3rd Order CW IMD versus output power with 1 to 15MHz carrier spacings

Fortunately techniques have been developed at RMRL to reduce the memory effect down to levels which have very little impact on system design, an example of which is shown in Figure 13 below. Similar improvements are seen for 5th and 7th order products.

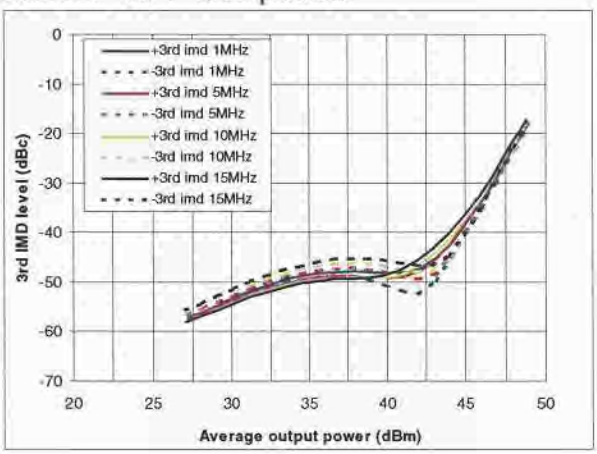

Figure 13: 3rd Order CW IMD versus output power with 1 to 15MHz carrier spacings with improved circuit

CONCLUSIONS

This paper has explained criteria for choosing power devices for use in W-CDMA power amplifiers intended for UMTS usage. A critical decision is the choice and number of power devices used in the output stage which set the linearity of the whole amplifier. The 3GPP specification has requirements that influence the choice of device, although consideration must be made to the complete system, if system performance has not been determined then a benchmark figure of merit can determined which help with device comparison. Datasheet information is not sufficient for device selection, to ensure a common baseline, devices must be tested on the bench, and demoboards must be obtainable from the manufacturer or designed and built in-house.

Careful considerations must be made to the test setup to ensure that the correct test signals are used with the correct test equipment and that the system is accurately calibrated.
It is important to build up an automated test suite to carry out the tests to ensure repeatability and gather more data than could be achieved manually.
Traditional characterisation using CW stimulus although useful is not sufficient for complete characterisation of a device, measurements must made using W-CDMA sources and swept over power.
Memory effects in class AB devices limit performance and reduce efficiency. There are very significant differences between the performance of devices within the same technology and between different technologies, this too must be carefully characterised. Techniques are available to minimise the impact of device memory.

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