Techniques for Right First Time MMIC Design

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Abstract

A MMIC design process is described which is robust and allows working circuits to be achieved in one design pass. QinetiQ has successfully used this process for the last decade. The design process is described first. Then a recently designed X-band Transmit / Receive MMIC is used as an example to show how the design process has been followed. This MMIC was fabricated using the Bookham Technology (formerly Caswell) H40p foundry process. The MMIC has a conversion gain of 10dB for receive mode and a conversion loss of 9dB for transmit mode. A low noise amplifier (LNA) used as a building block in the transceiver MMIC is used to demonstrate the design process described. Finally, the results of the LNA and the MMIC are shown. The measured results have very good agreement with simulation.

Introduction

The use of Monolithic Microwave Integrated Circuit component technology in modern microwave systems is becoming more and more important. The main reason for this is the ability to achieve small size and weight. It also has advantages in terms of reliability, repeatability of performance and reduction of parasitics. However, the foundry cost is very high and design duration can take three to six months. This makes the pre-manufacturing cost expensive. Moreover post-fabrication tuning is practically impossible. In addition, market requirements change rapidly, and competition for products is also high. To be successful, the cycle time for introducing new products into the market place has to shrink dramatically. Typically, it used to take eighteen to twenty-four months from design to market, now possibly four months is needed. Therefore, the need for designing a MMIC "right first time" becomes a necessity.

Here a general MMIC design technique is described. This technique has been adopted by QinetiQ (formerly DERA) for one decade and has allowed a high "right first time" success rate. Most of the failures are due to the nature of our business that pushes the foundry process to its limit. The design technique is first described then a case study of a transceiver MMIC design is used to demonstrate the technique. It begins by considering the top-level system design of how each component is orientated to optimise for space and connectivity. The LNA in the MMIC is then used to show the component level design. The measured result of the LNA is almost coincident with the design.

The MMIC Design Process

The ultimate objective of MMIC design is to produce a working circuit first time round. There are three basic points that should help in order to achieve this goal:

1. A reproducible / stable foundry process.
2. The foundry must provide accurate component models, both active and passive.
3. The use of appropriate design methods.

At the onset of a design project, one should look for a foundry that has attributes suitable for achieving the required circuit function. Factors that should be covered include the cost of foundry

processing, its reputation, device performance, process stability and the availability of both active devices and passive structure models. This is very obvious since any design will only be as good as the model accuracy. A statistical model is an additional benefit to the design since it can provide insight into performance variation due to process tolerances. Once the optimum foundry has been identified, the design can then commence.

During the design phase of the project, the following criteria should be followed. The circuit design should be compatible with the foundry process being used. It should occupy the smallest amount of GaAs area so as to achieve the highest yield and lowest per unit cost. All circuit specifications should be met and it should be tolerant of foundry processing variations since there is no tuning element in the circuit as is the case with a conventional hybrid microwave integrated circuit (MIC).

The design cycle can be summarised by the flow chart shown in Figure 1 below. Work starts with circuit block design based on MMIC specifications and proceeds through circuit design, optimisation and sensitivity and yield analysis to MMIC layout. The process is iterative, as shown. Circuit design typically uses a microwave design tool such as Libra/ADS and layout using a tool such as Wavemaker.

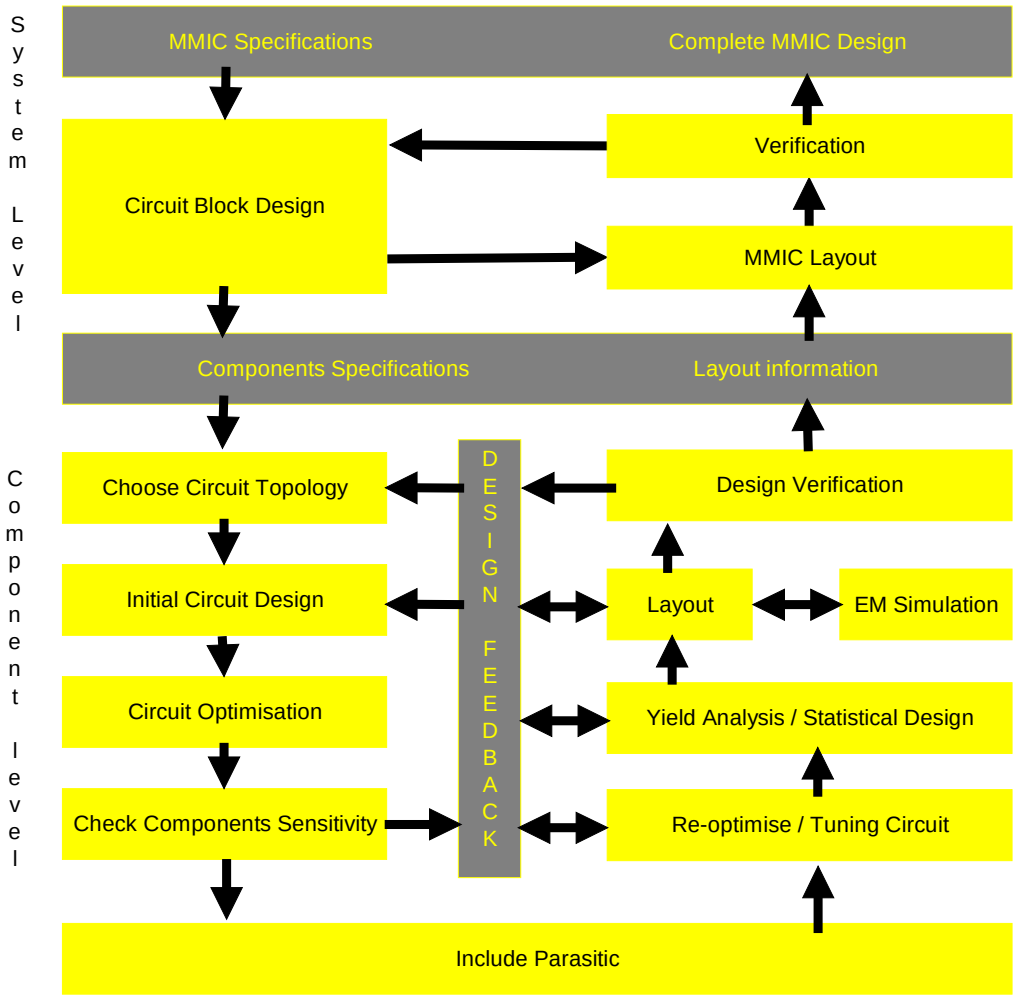

Figure 1 MMIC Design Flow Chart

Circuit Design

Once the appropriate circuit technique has been identified, circuit synthesis techniques can be used. For instance, in the amplifier design one can use a Smith chart or network synthesis tools. Electronic Design Aid (EDA) tools are preferable for MMIC designs as they allow unrealisable

topologies to be quickly identified and rejected. Some thoughts should be given as to how any synthesised ideal lumped element matching networks will be physically realised, using either lumped or distributed components. It should be noted that distributed elements are less sensitive to foundry variations but occupy the largest amount of chip area, particularly at low frequencies. If it is required to convert lumped element matching networks into their distributed equivalents then for example Richards Transform can be used. A starting approximation would be to use short and open circuited lengths of transmission line to realise inductors and capacitors respectively.

Circuit Optimisation

After the prime circuit topology has been obtained it will usually require some form of optimisation to achieve full band performance. Optimisation is essential for MMIC design, however it is not a substitute for good initial circuit design and should be used with care. The aim of optimisation is to produce circuit element values that result in the desired target performance. The optimiser targets should be chosen carefully, for example conflicting goals such as minimum S_{11} and minimum noise figure are best avoided. Also it is more efficient to only optimise parameters that are really required, for example S_{11} and S_{22} are not important in modules required for balanced amplifiers and similarly searching for maximum S_{21} together with minimum S_{11} and S_{22} is not necessary as they correspond to the same condition. Optimisation should begin with the simplest circuit, the smallest number of variables and use sensible component ranges for resistors, capacitors and inductors that are compatible with the foundry process. In some cases it is often beneficial to optimise in stages, e.g. input noise figure, output VSWR and inter-stage network gain flatness, followed by optimisation of the complete circuit using a composite error function. If a wide bandwidth response is required, one can choose a few frequency points to begin optimisation, such as the lower, the centre and the upper frequency points, to reduce the time needed for initial optimisation. Frequency points can be added gradually as the response approaches the criteria set by the circuit specification. If difficulties are found during optimisation then tuning components manually by hand may be beneficial as sometimes improved results can be obtained. This approach is particularly useful if an optimisation process is trapped in a local minimum such that a global optimum is not obtained. Scaling of the optimisation goals must be applied appropriately.

Sensitivity Analysis

One of the major differences between conventional hybrid and monolithic circuit design is that monolithic circuits are very difficult, if not impossible, to adjust after fabrication due to their level of integration and small size. In the design of MMICs, it is necessary to incorporate a certain degree of 'tolerance' to specified processing variations, so that batch to batch wafer differences still allow circuits to meet their design specification. At the start of a design, it is important to ensure that the circuit topology chosen is insensitive to the process variations and to eliminate such circuit components. For example, if a circuit uses very short open circuit stub, its impedance is sensitive to the length of the stub because the impedance is a cotangent function. On the other hand, if a shunt open circuit stub is longer than 2/3 of the wavelength, λ, its equivalent capacitance becomes very sensitive because the capacitance approaches the sensitive part of the tangent function. It may be necessary to perform a sensitivity analysis manually, using for example the 'TUNE' facility in ADS, by varying each element one at a time and monitor the response to check whether there is any sensitive circuit element. If such an element exists, effort should be made to replace the component, or if necessary, choose an alternative topology.

Adding parasitics and re-optimisation

If the circuit passes the sensitivity analysis the next stage in the design would be to add parasitics associated with the prime circuit elements. It is recommended that only circuit element models supplied by the foundry are used as such models are often process dependent. The physical dimensions of the required component are usually used to calculate the element parasitics from information supplied in the foundry's design guide. The Smart library supplied by the foundry usually contains parasitics related to the process parameters such as substrate thickness. Introducing parasitic elements usually degrades the circuit performance. Hence, the initial design needs to provide performance margins to allow for this. Furthermore, regarding the introduction of parasitics, re-optimisation should take place to optimise the performance according to the given

specifications. Here, the parasitic of the prime components should be adjusted accordingly. This process, however, is mostly automatic using the foundry supplied Smart Libraries.

In addition when designing a MMIC, allowances must be made for interface parasitics and discontinuities at the interfaces between the monolithic chip and external RF input/output lines. The effect of packaging is also required. Most foundries supply discontinuity models to take into account some of these effects. Appropriate discontinuity models should be included in the MMIC input and output networks at an early stage in the design. Also the effects of earth bond wire inductance should be included throughout the design, if via holes are not used.

Statistical Design

Some circuit topologies are less sensitive to component variations, e.g. by introducing feedback. These topologies can be deployed to minimise performance sensitivity. However, these may be at the expense of, say, gain reduction, degraded noise performance, etc. Very often, MMICs are pushed to the extremes and their performances are set at the limits of the technology. Therefore performance sensitivity is a natural and unavoidable consequence. Statistical design methods are useful in this area.

Circuit optimisation, where nominal circuit parameter values are searched for using optimisation routines is used to find a solution that provides the best performance. However, the purpose of a statistical design, on the other hand, is to find nominal parameter values that provide good yield during MMIC fabrication. The accuracy of the method depends on the reliability model, including statistical descriptions of the range of parameters that the design will encounter during fabrication. Meehan and Purviance [1] have described statistical design methods in more detail. Simulators such as Libra, ADS incorporate statistical design tools. [4]

Care should be taken when statistical optimisation techniques are used, since MMIC component values do not have independent behaviour, i.e. all elements of the same type tend to move in the same direction over specified tolerances. For example if the thickness of the metal film used in the fabrication of the resistor increased by a fraction of a micron then **all** resistor values change to a lower value. Moreover, if the dielectric film thickness used in the MIM capacitors changed then **all** capacitors will have a new value. This sensitivity analysis approach is perfectly acceptable for passive components, however with active circuit elements complex relationships may exist between some of the equivalent circuit parameters, e.g. Cgs, Rds, Cgd, gm etc. This information should be provided by the foundry and implemented using 'Smart Libraries'. This emphasises the importance of using a foundry having a well-characterised and repeatable process.

Layout

After the addition of parasitics, the circuit would undergo a second sensitivity analysis. Upon successful completion of this stage, a physical layout of the design would be implemented. When transforming the schematics into a physical layout it is suggested to use as many standard component cells provided by the foundry as possible since design rules will be automatically maintained. When positioning components, strict foundry layout rules have to be adhered to, such as minimum component to component spacing, minimum feature size etc. At present most foundry layout procedures use rules of thumb based on practical experience, however this approach becomes inadequate as circuit complexity and packing density increases. During the layout, extra lengths of transmission line and interconnects will often be needed to help realise a practical circuit. The addition of an extra component on the layout means that the circuit model will require further electrical analysis. The circuit layout process can be carried out by using a polygon drawing package. Automatic layout tools are used by some large design houses or foundries. However, this software is developed in house and is not available in the commercial market yet. [5]

Electromagnetic simulation is extremely useful nowadays due to a commensurate increase in the complexity of the MMIC and the advent of high speed workstations. Closely packed circuits should be simulated for accurate model and coupling effects. Most of the MMIC structure can be simulated on a 2½ D simulator such as Sonnet or Momentum. The simulated results can be fed into the circuit simulator and results can be compared. Minor adjustment can be made to the circuit components to achieve the desired response.

When laying out a circuit, one should always be aware of how the MMIC will be tested on wafer due to the cost involved in mounting in test jigs and how it will be packaged. Often complex circuits require multi-DC bias supplies and low frequency signal lines as well as RF inputs and outputs. Therefore, a test strategy must be planned well ahead.

Design Verification

After layout is completed, it is often necessary to have an independent check, i.e. reverse engineering. This will minimise human error of circuit layout. In low frequency analogue design, software tools are now available commercially to implement automatic layout. This significantly reduces design time. However, for RF and Microwave design such tools are only available for a limited range of foundries, where they have been developed internally.

One way to verify the design is to have an independent person who takes the layout and translates the content into a schematic. This in turn is simulated with a circuit simulator. The result is then compared with the designed one. If a discrepancy is found, effort will be spent to rectify it until a similar response is achieved. The exercise is to cut down the un-avoidable human error. Design rules are also checked at this point to ensure all foundry layout rules have been followed.

This reverse engineering process can now be carried out automatically using a software tool, e.g. Cadence. This process is called layout verses schematic (LVS). During LVS the software recognizes the layout patterns and translates them into schematics for circuit simulations. The schematics and simulations can then be compared manually.

Case Study: Transceiver MMIC

To demonstrate the design methodology, a transceiver MMIC has been considered. This MMIC is used in a phased array antenna module. The MMIC design is first considered at a system level in terms of component orientation, interconnect and chip interface. The LNA design is then shown to illustrate the component design process. Finally, the measured and simulated results of the LNA and the overall MMIC function are shown.

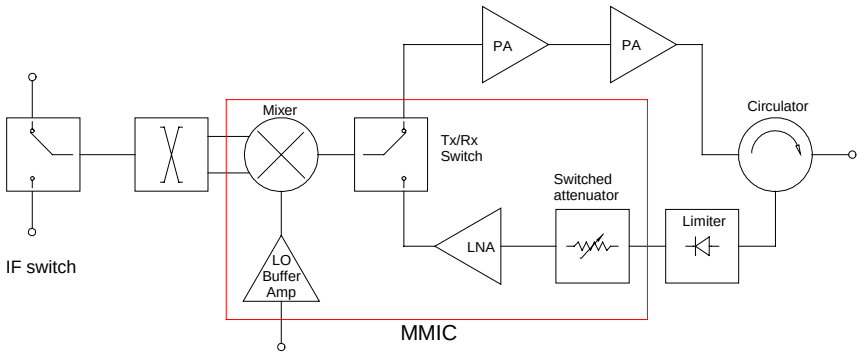

Figure 2 System block diagram

System Level Considerations

The system requirement is a T/R module for miniaturised phased array radar. A block diagram of the module is shown in Figure 2. This module has to fit into a cross section area of 15x15 mm^2. Effort is needed to integrate as much circuitry as possible into a single chip. The small signal handling components are chosen for integration into a compact multifunction MMIC. The power amplifier is best isolated to minimize the RF feedback during the transmit cycle. Moreover, the foundry process selected cannot deliver the transmit power required. This multifunction MMIC, therefore, includes an image reject mixer, a LO buffer amplifier, a RF switch, an LNA and a switched attenuator.

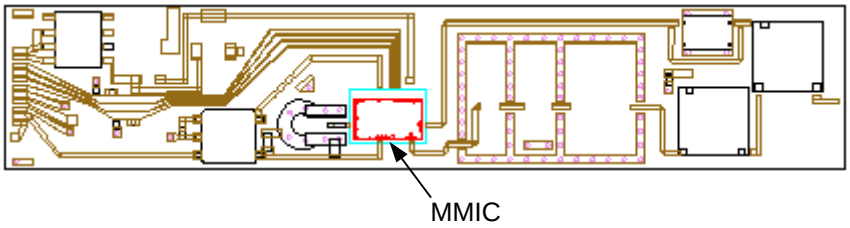

Figure 3 MMIC in a module

Various foundries have been studied, and the H40p process from Bookham technology (then Caswell) has been selected. The selection is based on the principles defined in the previous paragraphs. In summary, this is a mature process and QinetiQ has obtained accurate models from the foundry. Most importantly, the Marchand Balun used in the mixer can be realized using the two metal layers which is uniquely available from this foundry process. The two layers of metal are insulated using a thin layer of dielectric of which the thickness is very well controlled. The performance of the Marchand Balun depends on the tight coupling between adjacent transmission lines. Simulations showed that a gap of two to four micron is needed for the coupling to work effectively. Since the minimum gap width of metal on the same level is at least six microns, the two metal layers implementation topology is the preferred solution.

After an appropriate foundry has been identified, the next step is to identify interfacing with the chip. Figure 3 shows an artist impression of the module. The MMIC is placed in the middle and offset to the lower half of the module. It can be seen that the module is very tightly packed. The DC supply can only be accessed from one side (the top) leaving the other three sides of the MMIC for the LO, Receive and Transmit ports. The IF comes out from either side of the MMIC. The interface configuration also eases the RF on wafer test since only one DC probe card is needed and there is only one RF connection on each side of the MMIC.

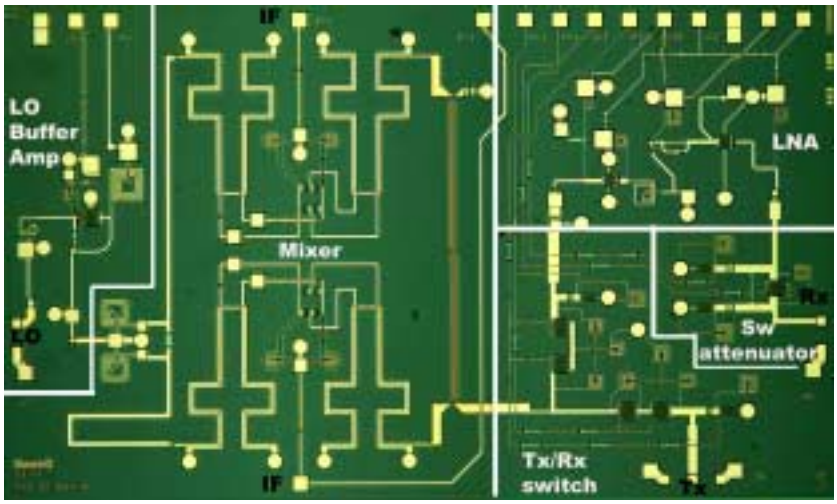

Figure 4 Photo of multifunction MMIC

Having the interfacing information in mind, the circuitry orientation and layout can then be considered. A few options have been suggested initially. The final layout depends on the actual circuitry size. A photograph of the MMIC is shown in Figure 4.

After the system aspect has been considered, the information is used in individual circuit design. When completed, the overall chip integration can be commenced. Some circuit components during the integration layout process require minor alteration in order to fit into the space allowed. When the layout is completed, the design verification is carried out manually to ensure the layout versus schematics is correct. The finished design is then sent off to a foundry for chip fabrication.

Component Level Consideration

To explain the process of component design, the design of the LNA used in this chip is described below. The information from the system design showed that the LNA frequency should be 10GHz ±0.5GHz, with a gain of >20dB and an associated noise figure ≤2dB. The power requirement is that the input 1dB compression point is ≥–10dBm. The input return loss is to be better than 7dB.

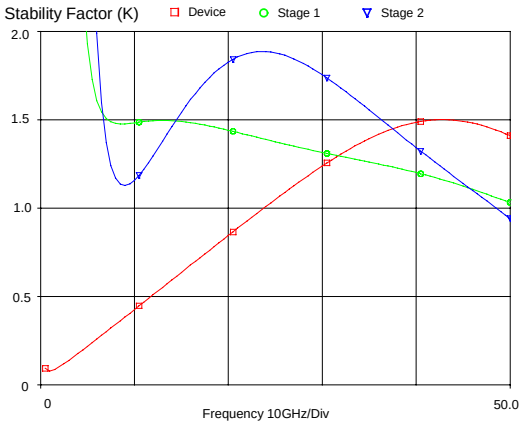

Figure 5 K stability factors

Choosing Topology & Initial Design

The topology choices for a LNA are limited. A reactively matched topology provides best noise performance. If good input return loss is required, a balanced design can be used, however, this is at a cost of both noise figure and DC power consumption.

In the LNA design, the number of amplifier stages is first identified using the maximum available gain data from the foundry. Two stages are sufficient to provide the gain required. Power handling is then considered. This is calculated from the power per unit gate width data provided by the foundry. A standard 240um gate width is chosen, operating at 50% of the saturated drain current. The drain voltage used for the second stage is 3V while the first stage is at 2V. A single drain supply is used with the 2 V supply derived via a voltage drop resistor.

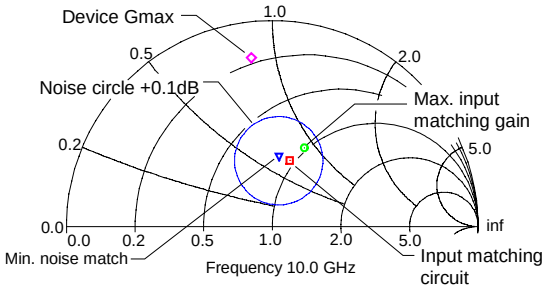

Figure 6 Matching impedance and device Gmax

Detail design

Given the experience of the designer and the simplicity of the circuit specification, some steps in the initial design may be omitted. The detailed design, with parasitics included, can be commenced immediately after the circuit topology is chosen.

Once the device and its bias conditions are decided, the device model is then used to consider the stability factor. When a device is unconditionally stable, it can be presented with any passive source or load impedance without risk of oscillation. The K stability factor is a technique for evaluating the stability of a device. Figure 5 shows the K stability factor for the device. When K is greater than unity, the device is said to be unconditionally stable. From Figure 6, this device is only stable at a frequency above 24GHz. Also shown in Figure 5 is the K stability factor for the two amplifier stages after they are stabilized. When stability circuits are included, the first stage becomes stable up to 50GHz while the second stage is stable to 48GHz. This is sufficient for the present design since the device unity current gain cut-off frequency (Ft) is about 40GHz.

After the device has been stabilised, the noise figure of the device is then examined. From the device model, it is found that the device has a minimum noise figure of 0.9dB at 10GHz. Therefore this will be the absolute minimum noise figure that the LNA will achieve. Figure 6 shows the input matching impedance for minimum noise figure and maximum gain. The circle around the minimum noise match point shows the matching impedance for 0.1dB noise degradation. A trade-off needs to be made between the minimum noise figure and maximum gain. It should be mentioned that the maximum gain point also corresponds to the best input return loss. Therefore, the input return loss specification governs the minimum noise figure that the LNA can achieve. However, introducing source inductance can reduce the gain of the device. This puts the maximum gain point closer to

the minimum noise figure point. The maximum amount of source inductance that can be introduced depends on the stability of the device, since large source inductance leads to an open circuit at high frequency, hence an unstable circuit. Stability conditions must be checked to ensure the device remains stable up to the device cut off frequency.

The matching circuits are next to be designed. In this LNA example, we have decided to use two stages. There are three matching sections to be designed. The input matching circuit needs to present the required impedance for minimum noise figure. The inter-stage is to match the output of the first stage to the input of the second stage and the output matching circuit must match the output of the second stage to the system impedance. It should be pointed out that the source inductance is also a series feed back mechanism, reducing the reverse isolation of the device. This introduces difficulty in achieving the simultaneous matching condition for both input and output of the device since the input matching condition affects the output and vice versa. The initial matching was carried out using a Smith Chart. A simulator (such as Libra) was used to monitor the impedance change during the matching circuit design. Once the matching circuit is realised, the optimisation routine can be used to adjust the circuit to achieve optimum performance.

Sensitivity and Yield Analysis

The sensitivity test was carried out manually by adjusting each component used in the LNA. Each element was checked against the designed response.

With the smart library, component tolerance is in built. A Monte Carlo simulation run with about 500 sample shows that the variation is within expectation. Statistical adjustment may improve the yield further. More information on this topic can be found in [1].

LNA Layout

The circuit layout is carried out manually using a 2-D drawing tool 'Wavemaker'. Effort is made to arrange all the matching circuit elements to make the LNA small without compromising performance. The input and output of the LNA are also positioned in such a way that the attenuator can connect to its input without additional line length added and the output can connect to the RF switch with a minimum length of line. To achieve the lowest noise figure, input matching network loss must be minimised. To help achieve this, care must be exercised to ensure minimum lengths of transmission line are used in the input matching circuit. If an inductor is to be used, choose the library standard inductor since this is well characterised. In this LNA example, there is only one inductor used in the inter-stage matching circuit. Other shunt inductors used in the circuit are mainly for bias and stability purpose. The bias requirement for the two stages of the LNA is different. To enable operation from a single drain supply voltage, there is an on chip resistor and a potential divider to provide the correct bias condition for both devices.

The Measured LNA Performance

The LNA was also fabricated as a separate test component. The measured and simulated responses of the LNA are shown in Figure 7. The gain and output return loss have very good agreement. The input return loss is about 8dB worse than simulated. Nevertheless it follows the same trend in frequency.

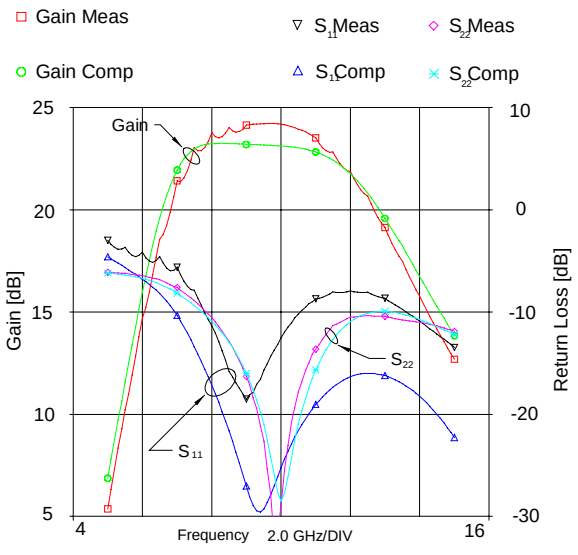

Figure 7 Compare measured and simulated results of the LNA

Integrated MMIC Layout

When all the component designs are completed, trial integration follows. Although detailed planning of the overall chip has reduced the iterative process between layout and design, further improvement is immediately realised once the integration process starts. There are two adjustments made after the first trial integration. Firstly, with the LO input of the Mixer at the centre, there is no space for the LO buffer amplifier. This short fall has been rectified by shifting the LO port of the mixer to one side and re-routing the input and output connections of the LO buffer amplifier so that it can be placed along side with the mixer LO port. The other problem is that the Transmit / Receive switch was symmetrically laid out, however, when bending it in an 'L' shape, the switched attenuator fits into the empty space available.

The other consideration for the layout is that the chip must be tested using the RF on wafer test facility. This imposes two hurdles to be overcome. The number of DC connections required is ten. On each side of the chip, there can only be either RF probe pads or DC connections. The frequency translating nature of the chip has almost made this impossible to be tested on wafer. However, with the IF ports being tested using the DC probes, this becomes possible. One of the two IF ports is routed to the opposite side of the chip that has all the DC connections, so that they are both in line and can be tested using a single DC probe card for RF on wafer test. This is possible because the IF is at a very low frequency. A twisted-pair connection is sufficient. The number of pads needed exceeds the number that DC probe card can handle, therefore, the control lines for the switch and attenuator are linked using a line in the saw channel so that the chip can be tested on wafer. The advantage of using the saw channel for the connection is that the link will be broken when the chip is diced.

Throughout the design, standard library components are used. Component spacing was also followed tightly within the foundry design rules. The Marchand balun is the only exception. This structure was designed and simulated using an electromagnetic simulator (Sonnet EM). The result was then fed back to the circuit simulator (namely Libra) for circuit level design.

Integrated MMIC: Comparison of Measured Results and Simulation

The integrated chip was simulated using Libra by linking the individual circuits together in a hierarchical structure manner. The transmit results are shown in Figure 8 and the receive results are shown in Figure 9. In both cases, the measured results show good agreement with the simulations.

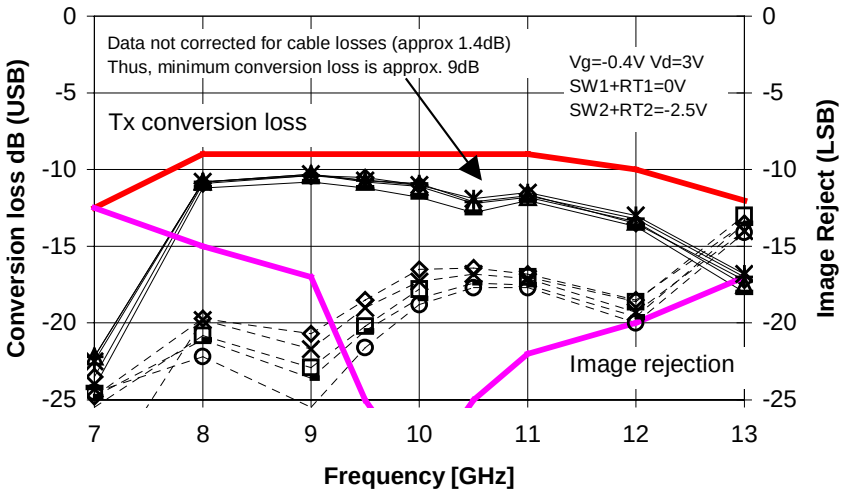

Figure 8 Transmit path results compared

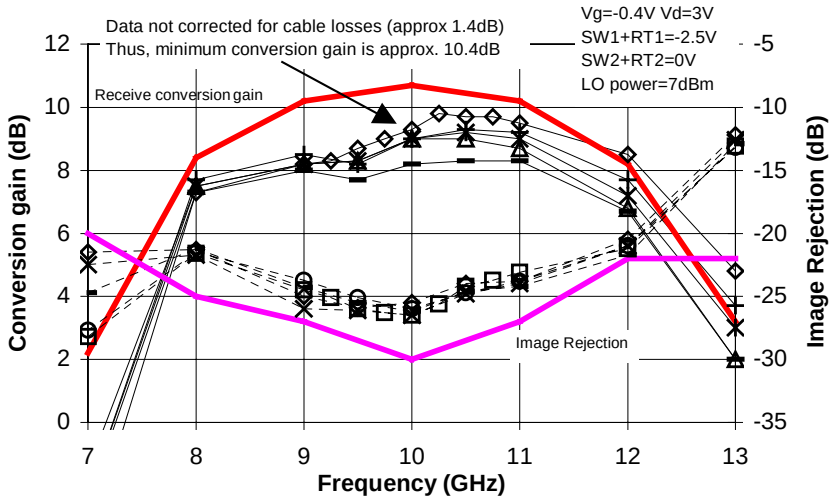

Figure 9 Receive path results compared

Conclusions

A MMIC design method is described which is robust and allows working circuits in one design pass. This approach is widely used by the MMIC team in QinetiQ and has allowed a very high success rate to be achieved over the last decade. An X-band transceiver MMIC, used in a phased array radar, has been used to illustrate the design method. In particular the LNA design has been discussed to demonstrate this method at the component level. The measured results show good agreement with the simulations.

Acknowledgement

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