USING A VECTOR NETWORK ANALYSER IN OSCILLATOR DESIGN

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Introduction

In this paper I am going to describe a technique for using a vector automatic network analyser to solve some of the problems that occur in oscillator design and development. This is not a complete analysis of oscillator theory or design; it is a simple and practical technique that can be used in the lab at the debugging stage. It is particularly useful for oscillators with added stabilising elements such as crystals, surface acoustic wave (SAW) devices, ceramic resonators, etc.

Some of the problems encountered that can be solved with this technique are:

- Oscillators that will run but not start.
- Overtone crystal oscillators running on the wrong overtone, or even the fundamental.
- Oscillating on more than one overtone simultaneously
- Spurious oscillation at well above the design frequency
- Breaking free of the stabilising element and wandering off in frequency.
- VCOs that change behaviour as they are tuned.

Readers who have not experienced at least one of these problems will have led very sheltered lives indeed. The problem with most approaches to fixing these problems, and also quite often with simulations, is that once the problem is absent, one does not know how well it has been fixed – is the problem going to recur as soon as one's back is turned, or when the design in put into production. What I am going to show here is a method of detecting these problems while they are still incipient, and thereby enabling a margin of safety to be designed in.

This technique is something I developed and have been using since the late 1980's. I would, however, be very surprised if it has not been independently developed many times by others.

Oscillator Theory

One classical view of an oscillator is as an amplifier and a frequency determining network. Figure 1. At the desired frequency and amplitude the gain around the loop is unity and the phase shift is zero, or 360, 720, etc degrees. One can easily envisage how the loop can be broken open and a network analyser used to measure S_{21} in order to characterise the circuit. This is rarely practical, however, not least because of the physical difficulties. Above a few 10's of MHz it is difficult to get valid measurements on a real circuit (as opposed to a specially prepared test circuit). And in any case, the resulting Bode plots usually require significant mental effort to interpret.

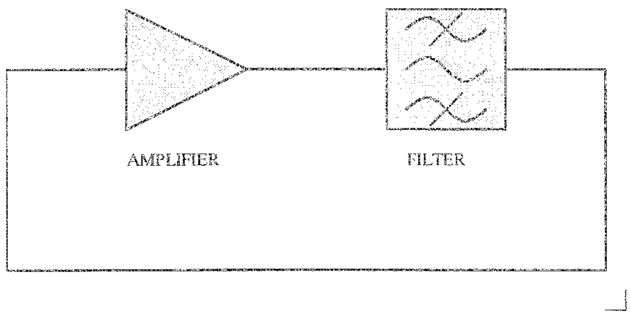

Figure 1: Oscillator viewed as a loop

An alternative view is to treat the oscillator as a shunt combination of impedances, one of which is a negative resistance that is contributed by the active element. It is then possible to choose a node in the network that one can connect to and make an S_{11} measurement. By displaying the S11 plot on a Smith Chart it is very easy to see what is going on. More importantly, one can also see what might be going when one is not looking.

Figure 2 shows an idealised oscillator drawn this way and the resulting S_{11} measurement. If the loop goes outside the open circuit point on the Smith Chart, the circuit is an oscillator. Or, more accurately, will be as soon as we stop measuring it.

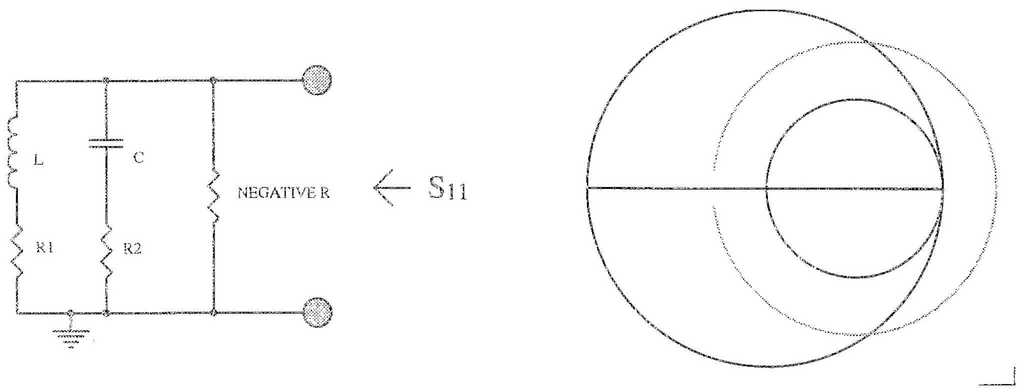

Figure 2: Idealised Oscillator Impedance

In a real circuit there may be a bewildering choice of nodes to connect to. For an S_{11} measurement, the best place is a high impedance point. A good rule of thumb is to connect to the highest impedance node of the active element, as shown in Figure 3. Note that while the measurement can be made with little physical invasion to the circuit, electrically it is very invasive. The presence of a 50 Ohm load on a high impedance point stops any oscillation. The circuit is being measured for small signal responses at its resting bias condition. We are therefore measuring the start up conditions, rather than the running conditions of the oscillator.

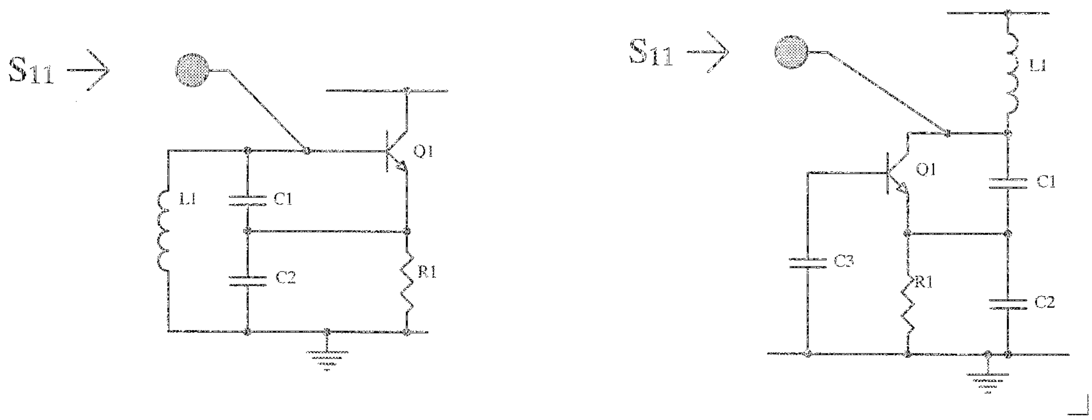

Figure 3: Circuit connection points

A Smith Chart display of these starting conditions will reveal most of the standard oscillator problems. Some are shown in Figure 4.

a) Plenty of gain in the active element but the feedback is arriving with a phase lag. This circuit will be reluctant to start and always looking for an excuse to do something else.
b) A spurious resonance at high frequency. The oscillator may jump to the spurious frequency, or even generate both frequencies. Even if the oscillator runs correctly, this plot reveals an incipient problem that needs to be fixed.
c) A spurious resonance at low frequency, possibly caused by a decoupling problem or a choke in one of the supply or bias lines. Again, even if the oscillator appears to run correctly, it is an incipient problem.
d) Coupled resonators. This is the effect seen if the wanted signal is taken out of the oscillator by a tuned stage without sufficient isolation.

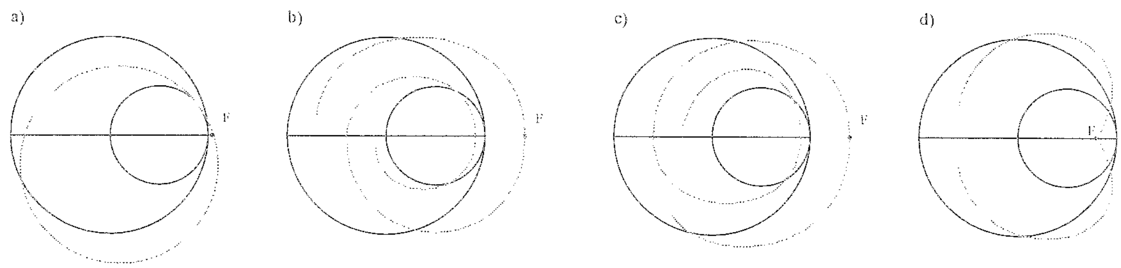

Figure 4: Problem oscillator plots

Stabilised Oscillators

It can be seen therefore that for a well behaved oscillator, there should be one resonant loop going well outside the open circuit end of the Smith Chart and any other loops well inside. The same principle can be extended to stabilised oscillators.

Figure 5 is the circuit of a 3rd overtone crystal oscillator, with an S_{11} measurement being made on the base of the transistor. Why this node in the circuit is chosen and not the top of the tuned circuit will be apparent when the roles of Rb and Cb are considered.

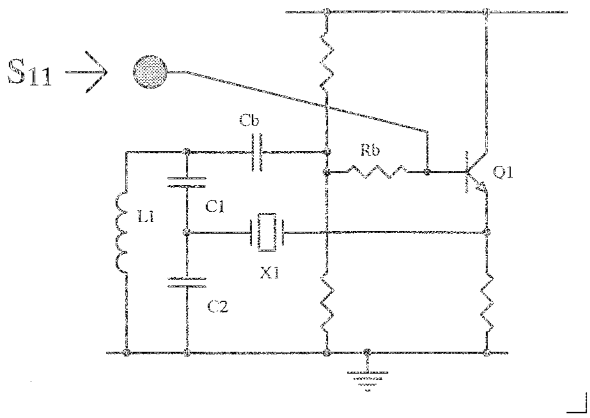

Figure 5: 3rd Overtone Crystal Oscillator

The S_{11} plot expected is shown in Figure 6 and the essential feature is immediately apparent. The main resonance C of the tuned circuit is inside the chart, but it is positioned so that a subsidiary resonant loop D which is due to the feedback on the crystal overtone goes around the open circuit point. This, in a nutshell, is how to make a well behaved stabilised oscillator. The main loop must be inside the chart or it can break free of the stabilising element. The subsidiary loop must go around the open circuit point, or it will not start.

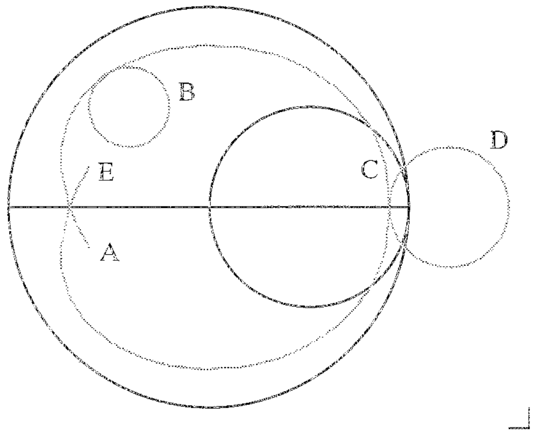

Figure 6: Impedance plot of overtone oscillator

Other features to note in this ideal plot are the lack of troublesome resonances at A and E, and the smaller loop at B. This is due to the crystal fundamental resonance of the crystal. In this example it is not a problem, but with unfortunate choices of L, C1 and C2 it could be. The usefulness of Rb and Cb can now be seen. Changing their values has little effect on the normal operation of the oscillator but they can be very powerful in controlling the position of loop B.

The plot shown in Figure 6 cannot be generated directly but must be built up from several measurements. The reason is that very fine frequency steps are needed to measure the loops at B and D. The way in which this can be done is illustrated in another example.

Figure 7 is the circuit of a simple SAW stabilised UHF oscillator. This is typical of low cost transmitters in the licence exempt band at 433 MHz. Such oscillators are

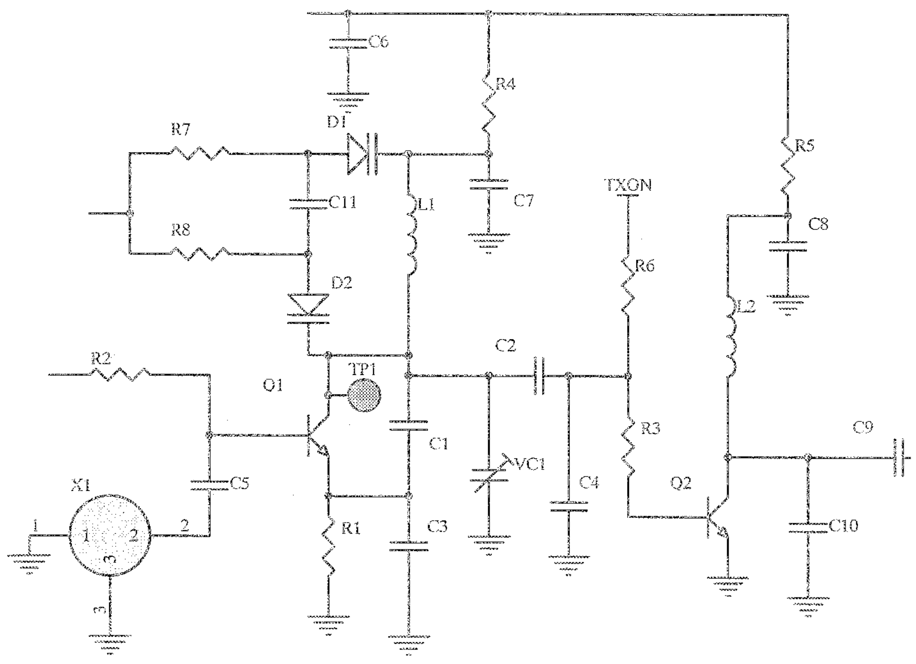

Figure 7: SAW stabilised UHF Transmitter

used in short range alarm and remote control systems and have probably caused more collective misery to the design and development community than any other type.

Figure 8 is a screen shot of an S_{11} measurement at the collector. The main LC resonance is near to 433 MHz and is just inside the Smith Chart. The spurious resonances at high and low frequencies are under control. Some slight rippling of the trace can be seen around 433 MHz. This is the effect of the following stage; there is a little coupling to its output circuits but not enough to compromise the oscillator.

Examining over a reduced range at very fine frequency steps (801 points in 1 MHz) gives the screen shot in Figure 9. This clearly shows the large excursion around the open circuit point due to the SAW device. Taking these two measurements together it can be seen that this is a well behaved oscillator that is always going to start on the right frequency and cannot be tuned or pulled away from the SAW frequency.

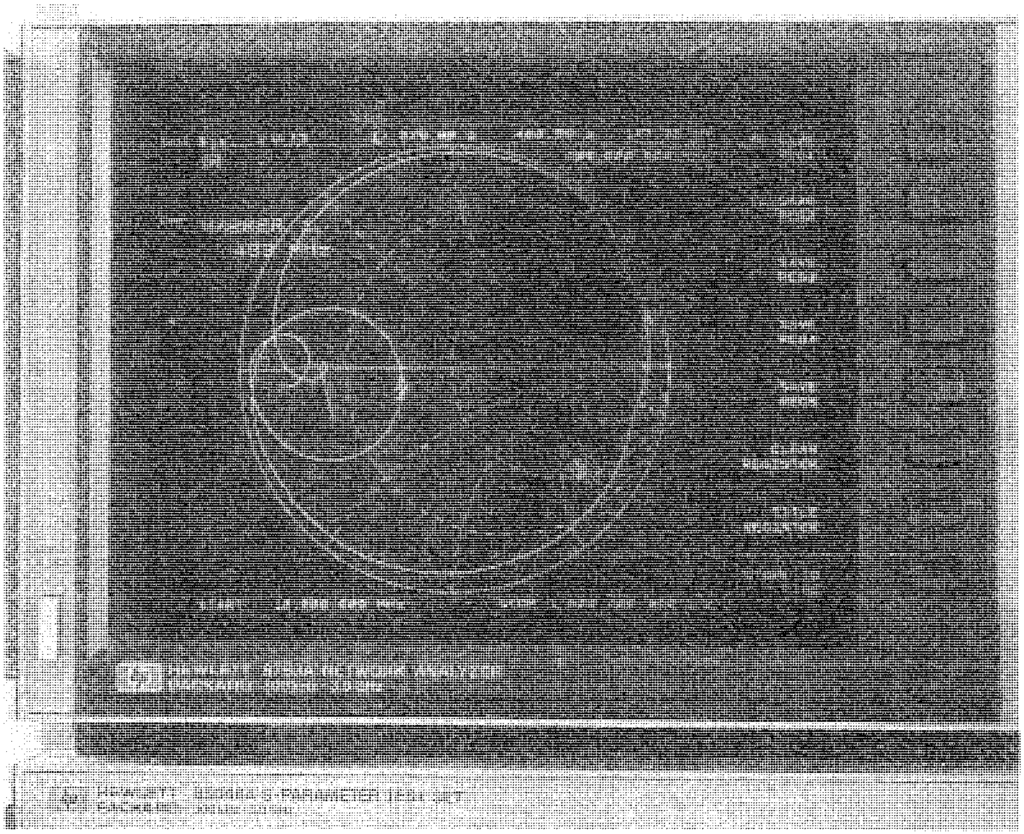

Figure 8: Wideband plot

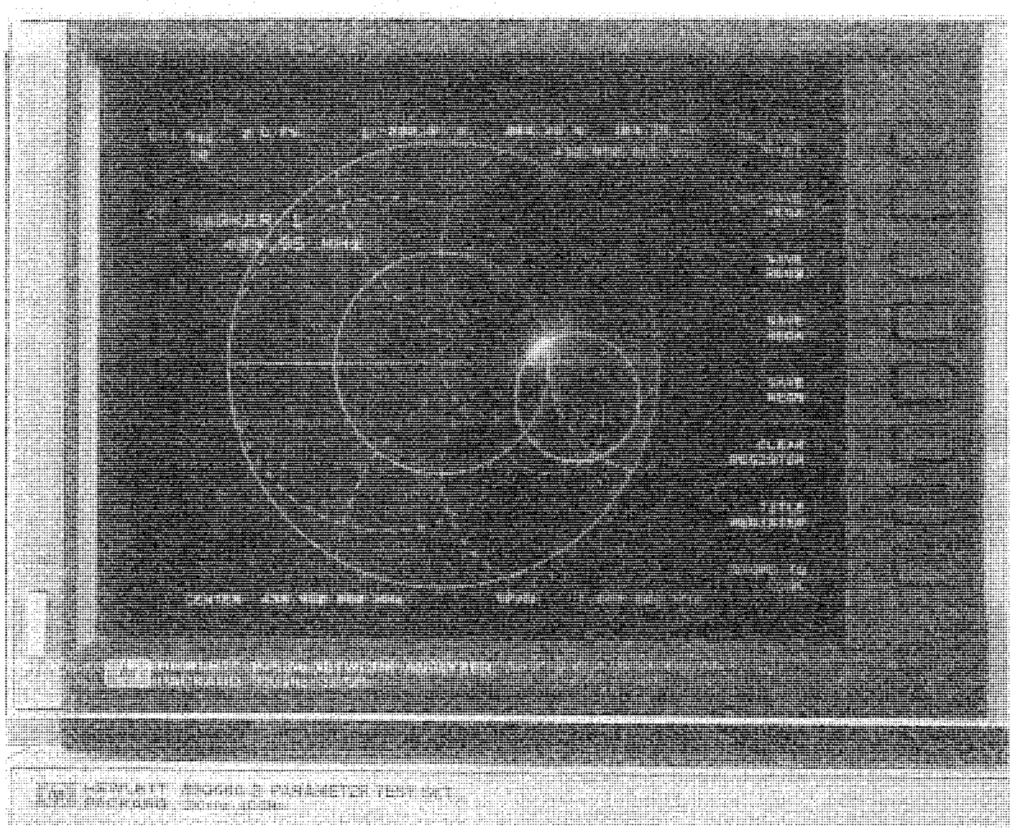

Figure 9: Narrowband plot

Summary

Performing S_{11} measurements on an oscillator circuit is a useful design and development tool. A Smith Chart plot at a high impedance node yields vital information in a form that is easily interpreted.

This technique can be used to investigate and eliminate the start up problems that are often encountered with oscillators. Incipient problems can also be detected. It is possible therefore to ensure a margin of safety in the oscillator circuit.

The technique described is suitable for virtually any oscillator design and is particularly useful for oscillators with additional stabilising elements, such as crystals or other resonators.

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