End of Line RF and Microwave PCM Testing of 6" GaAs pHEMT Wafers

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ABSTRACT

Our methodology for "end of line" RF and microwave testing of finished 150mm GaAs pHEMT foundry wafers is described. An end of line RF and Microwave Test facility comprising £ 2M of capital test equipment has been created. The capability exists for scalar measurements of power, noise and inter-modulation products as well as for vector measurements of s-parameters and noise parameters at frequencies of up to 40 GHz. A range of "Automated Test Equipment" and laboratory scale bench test systems are available. RF and Microwave "Process Control Monitor" (PCM) tests for the disposition of foundry wafer sales are supported as are custom device characterisation, model extraction and functional testing of integrated MMIC and discrete products. Procedures for software control are implemented using UNIX for our "Automatic Test Equipment" (ATE) systems, Labview for the integration and control of bench instruments and a SAS database for the archiving and statistical analysis of test data. An example of the implementation and transfer into production of a high volume RF test of a discrete 2x100μm pHEMT PCM device is described.

INTRODUCTION

Filtronic Compound Semiconductors represents a significant investment by Filtronic PLC in a state of the art facility for the development and supply of 150mm GaAs pHEMT foundry wafers. The supply of discrete and integrated GaAs pHEMT product wafers to key internal Filtronic business units, to carefully selected strategic alliance partners and to the merchant semiconductor marketplace is of critical importance to the development of new business opportunities for Filtronic. Discrete products include high power amplifiers for wireless infrastructure and for handset applications. Integrated products include Monolithic Microwave Integrated Circuits (MMICs) for broadband access as well as antenna and diversity switches for handsets. This paper describes the "End of Line" test function that has been created within Filtronic Compound Semiconductors GaAs facility at Newton Aycliffe, County Durham. The "End of Line" or "Back End" function has within its remit DC and RF electrical testing, visual inspection, die separation, product audit, packing and shipment to the customer. In particular this paper will outline the methodology adopted for high volume RF and microwave testing of GaAs pHEMT wafer products, which is of central importance to the assured supply of quality GaAs components to our customers. As an example the implementation of a high volume RF

process control monitor (RF-PCM) test to support discrete and MMIC pHEMT foundry wafer sales is described in detail.

END OF LINE FUNCTION

After all wafer fabrication processes have been completed it is vital that the finished wafers are subject to stringent final visual inspection, DC and RF electrical testing and a final audit before shipment to the customer. A separate "End of Line" area and staff has been created because of the need for strict control of this activity and because of the natural distinction between handling 150mm GaAs wafers during processing and handling finished wafers. The finished wafers are thinned to between 50 and 150 μm and mounted on adhesive film and supported on 300 mm stainless steel ring carriers. The functions of test, inspection, die-separation, die picking, packing and shipment all fall naturally within the remit of this area. Three process routes are supported, these are: whole wafer sales, die-separated wafer sales and discrete "picked" die sales. DC and RF electrical PCM testing, visual inspection, product audit, packing and shipment are common to all three routes. Additional processes such as customer specific testing, for example 100% DC and or RF die test for the supply of "known good die" can be optionally ordered. Wafer foundry sales however are principally supported by the strategy of "Wafer Acceptance Testing" (WAT) of identified DC and RF PCM test structures. PCM structures are identified and test specifications created during the "Process Development Review" (PDR) phase of new process introduction. For example during the 0.5 μm depletion mode pHEMT MMIC process (route FD05) introduction a RF PCM test of a discrete 2x100μm pHEMT was specified and implemented. On transfer into production Filtronic Compound Semiconductors routinely monitors the pass / fail yield over a wide range of DC and RF test parameters measured on a number of discrete and integrated passive and active PCM test components.

RF-PCM TEST IMPLEMENTATION

The test is implemented using an Anritsu 37369C 0.04-40GHz vector Network Analyser, Cascade Microtech Summitt 12000 semi-automatic wafer probe station and PC controller. Thinned finished wafers supported on film frames are manually loaded and aligned on the probe station. An automatic routine developed in Labview is used to control the probe station position, touch down on the wafer, apply DC bias and record the measured s-parameters and DC bias condition. Picoprobes from GGB Industries are employed to provide wide bandwidth 50ohm connections to the gate and drain terminals of the common source pHEMT as shown in Figure 1. Calibration of the Network Analyser to reference planes located at the probe tips is performed using LRRM calibration standards fabricated by Cascade Microtech on an Alumina Impedance Standard Substrate (ISS) tile. Independent verification of the quality of the calibration is assured by checking that the return loss of an open reflection (probes not at contact) is within +/- 0.1 dB to 40 GHz. Multi-bias s-parameter measurements over a range of gate and drain bias conditions are performed on each PCM site tested on the wafer and small signal equivalent circuit parameters are extracted. To optimise the throughput of the test system the number of bias points used is 18, which provides a sufficient range of bias conditions for accurate extraction. A number of the RF parameters, both measured and extracted are then monitored and used to determine the pass or fail criteria for the wafers.

RESULTS

Typical results for a series of RF measurements of 2x100μm pHEMTs made on all of the 38 PCM sites fabricated on one wafer are shown in figures 2 through 11. Figures 2 to 5 show the spread of s-parameters across the wafer measured at V_{ds} = 3V and I_{ds} = 150 mA/mm. Figure 6 and 7 shows the spread in the measured current gain and maximum available gain respectively also at the same bias condition as the measured s-parameters. Figures 8 through 11 show contour maps plotted across the wafer for the extracted small signal equivalent circuit parameters. Some of the principal extracted parameters are shown, these

are the current gain cut off frequency (f_T) the maximum available gain measured at 10 GHz (G_{max10}), the gate to source capacitance (C_{gs}) and the gate to drain capacitance (C_{gd}). All of the results show excellent uniformity of the RF parameters across the 150mm GaAs wafers typical of our 0.5μm d-mode pHEMT process.

CONCLUSION

The strategy for high volume on wafer end of line RF and microwave PCM testing has been described. As an example the implementation of an RF PCM test of a 2x100 μm discrete pHEMT PCM test structure for process control of the 0.5μm d-mode pHEMT process has been presented.

ACKNOWLEDGEMENTS

The author acknowledges Rob Davis for development of the small signal equivalent circuit extraction routines and Sumit Kumar for the provision of RF on wafer measurements.

FIGURES

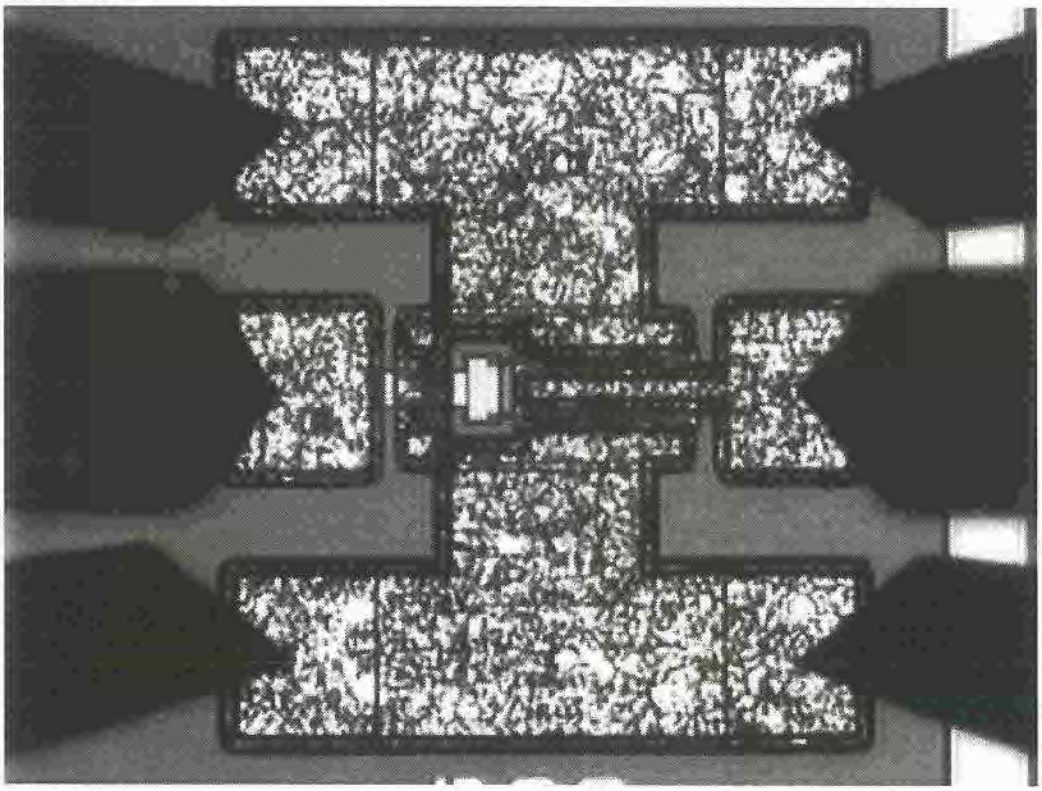

Figure 1. GGB Picoprobes contacting the Gate and Drain of the Common Source 2x100 μm pHEMT RF PCM device.

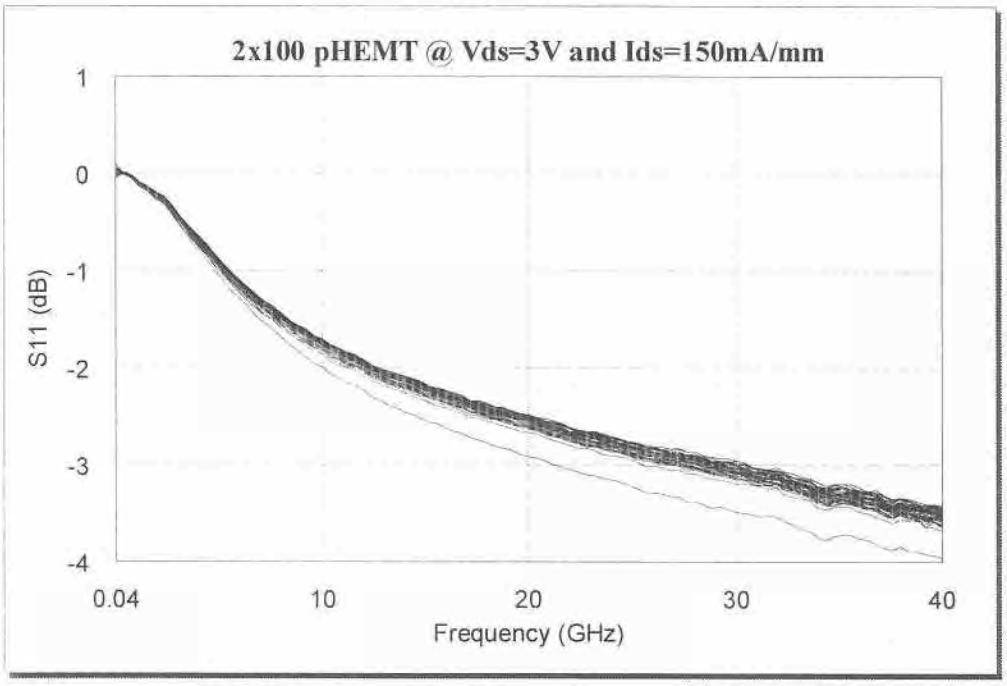

Figure 2. Spread of S11 magnitude (dB) measured on 38 PCM sites across the wafer.

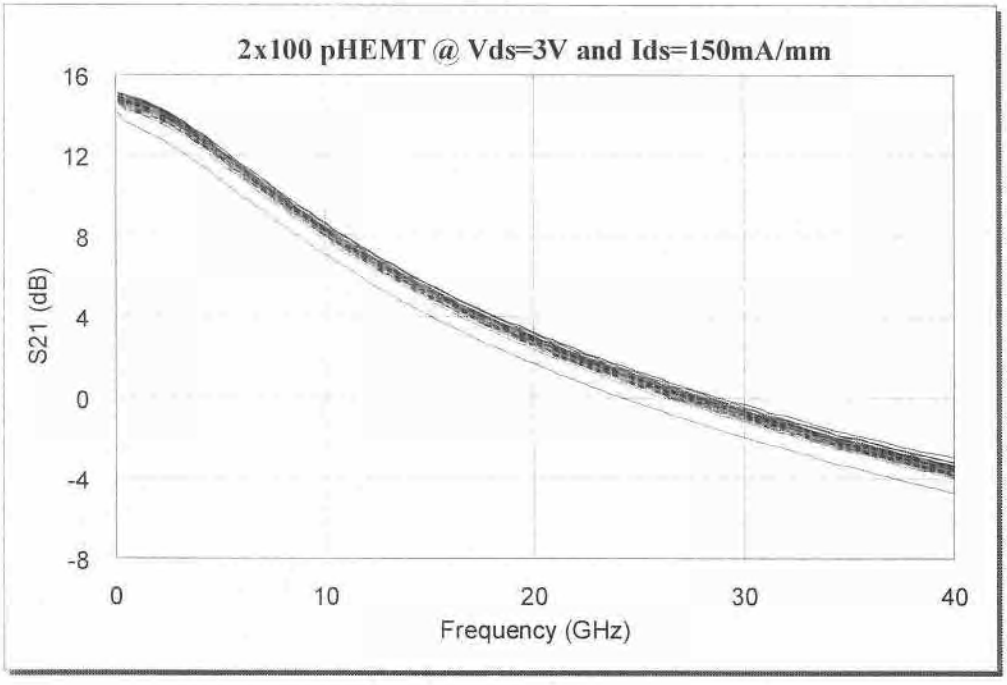

Figure 3. Spread of S21 magnitude (dB) measured on 38 PCM sites across the wafer.

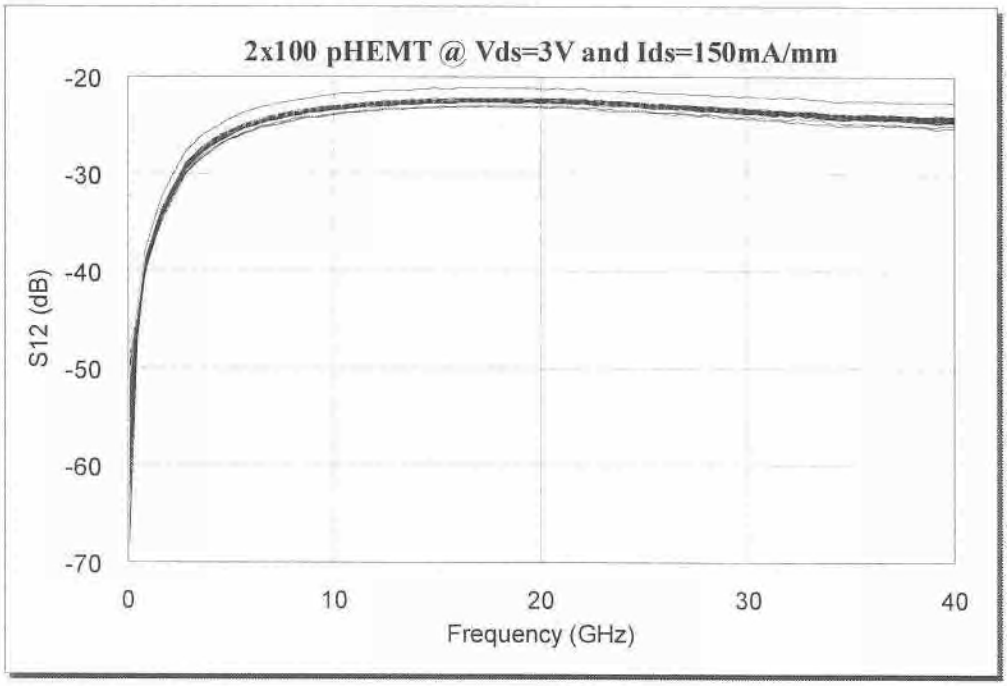

Figure 4. Spread of S12 magnitude (dB) measured on 38 PCM sites across the wafer.

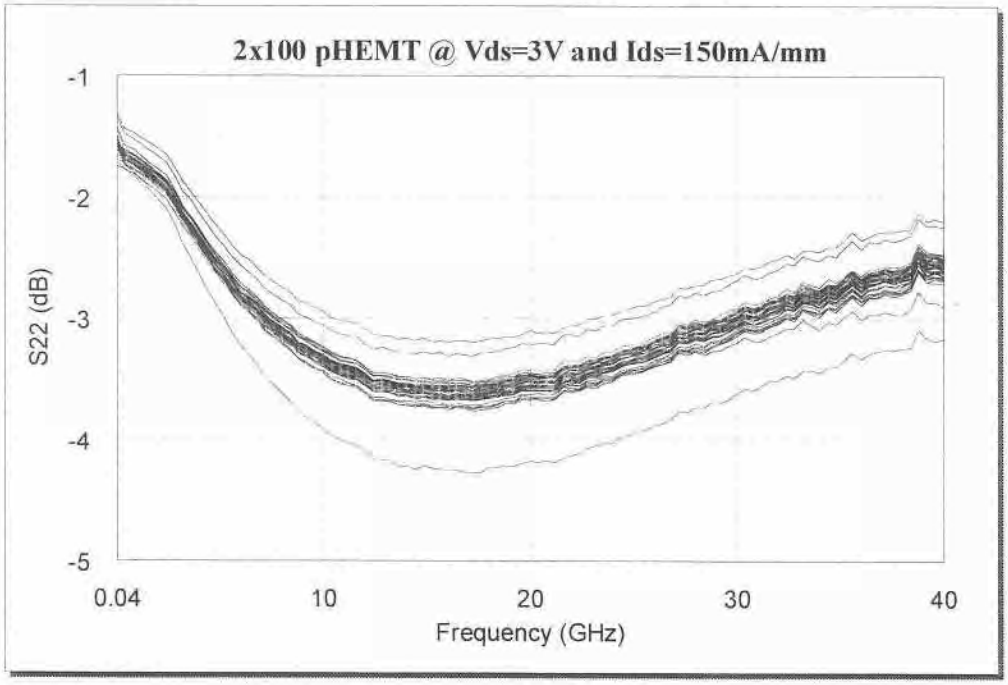

Figure 5. Spread of S22 magnitude (dB) measured on 38 PCM sites across the wafer.

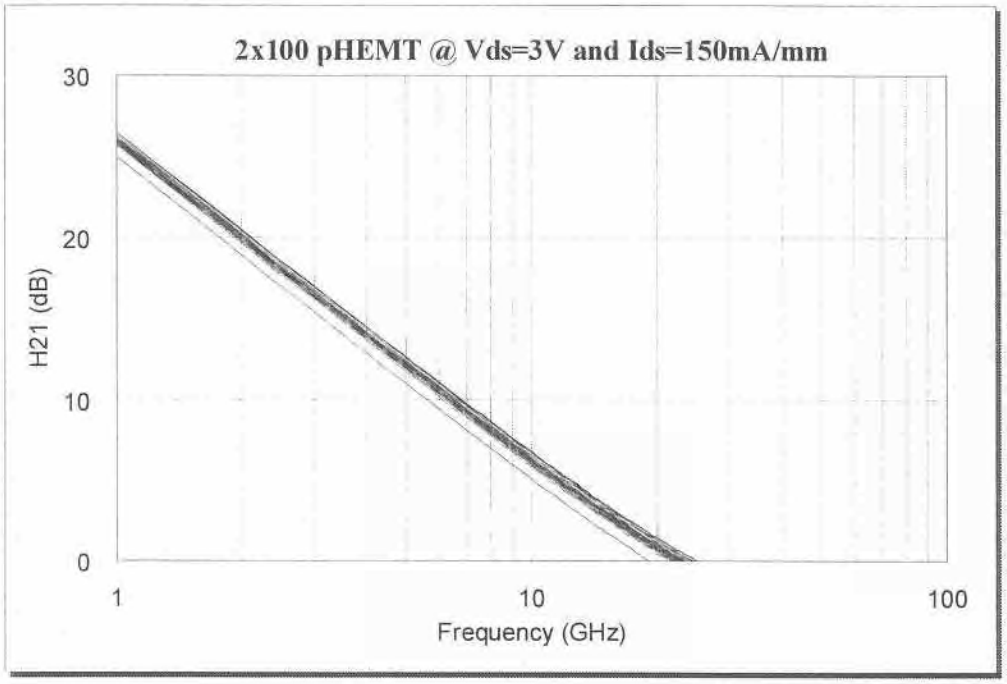

Figure 6. Spread of current gain (dB) measured on 38 PCM sites across the wafer.

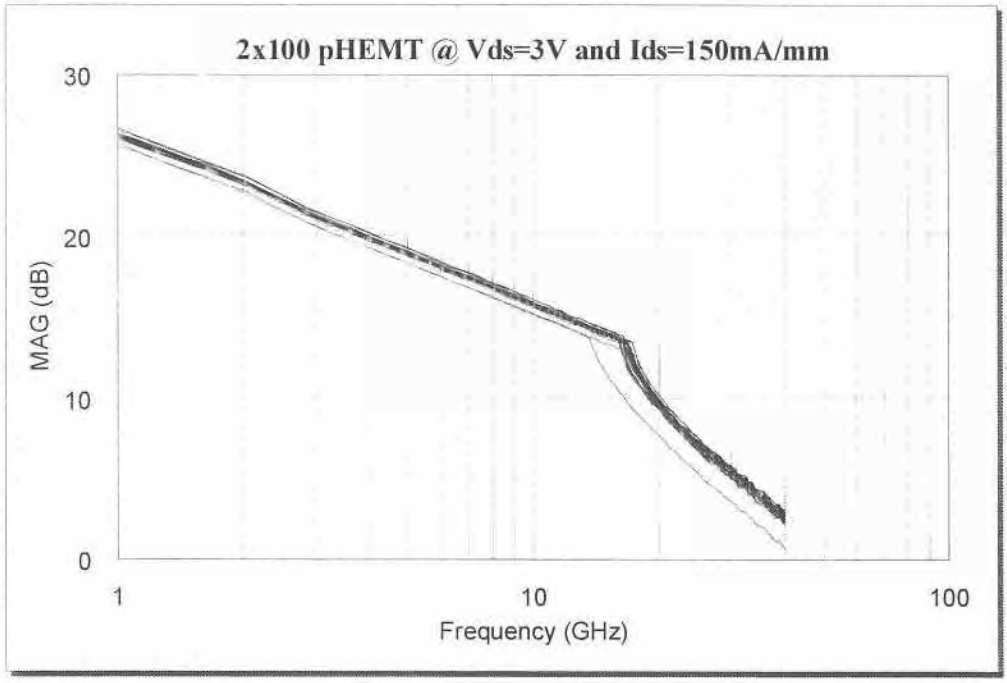

Figure 7. Spread of maximum available gain (dB) measured on 38 PCM sites across the wafer.

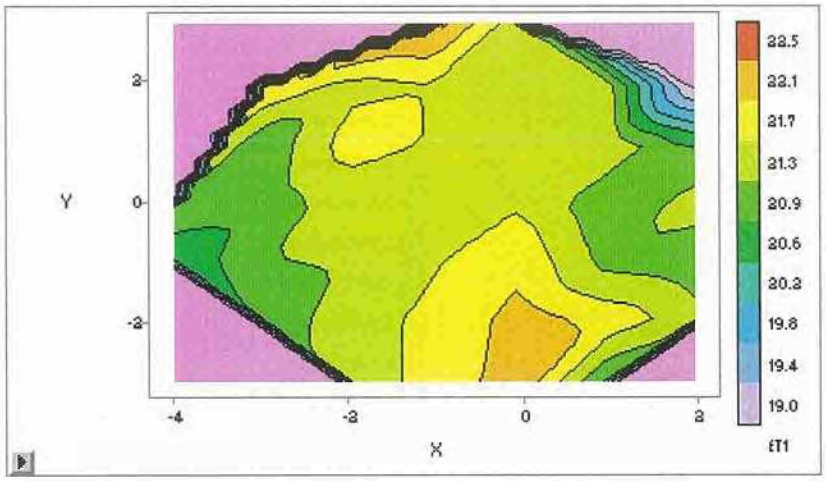

Figure 8. Contours of current gain cut off frequency, f_T (GHz) plotted across the 150mm GaAs pHEMT wafer. The coloured/shaded areas in the corners of the plot (outside the wafer) are artefacts.

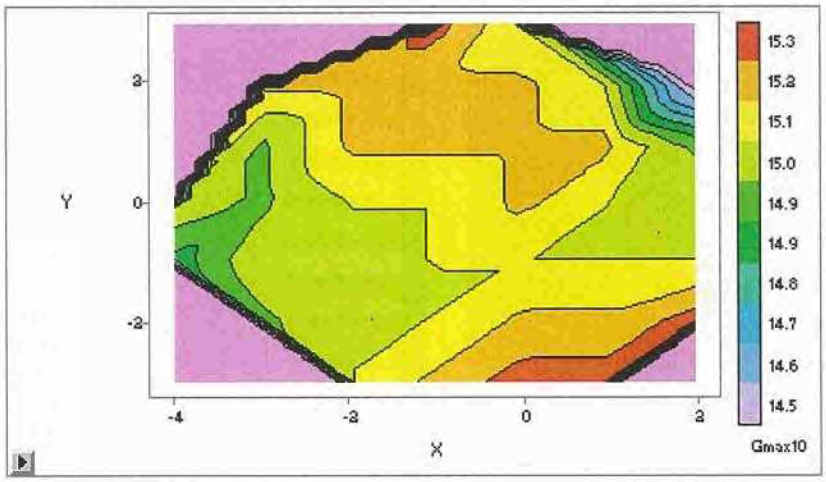

Figure 9. Contours of maximum available gain at 10GHz (dB) plotted across the 150mm GaAs pHEMT wafer. The coloured/shaded areas in the corners of the plot (outside the wafer) are artefacts.

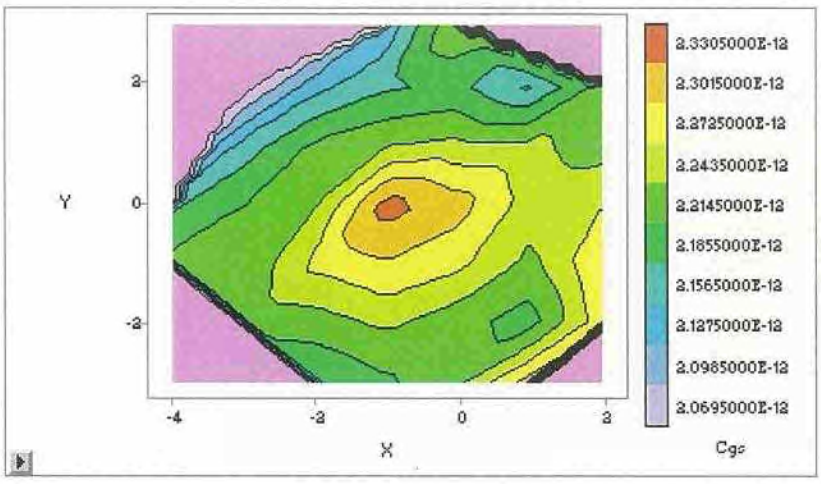

Figure 10. Contours of gate source capacitance, C_{gs} (F/mm) plotted across the 150mm GaAs pHEMT wafer. The coloured/shaded areas in the corners of the plot (outside the wafer) are artefacts.

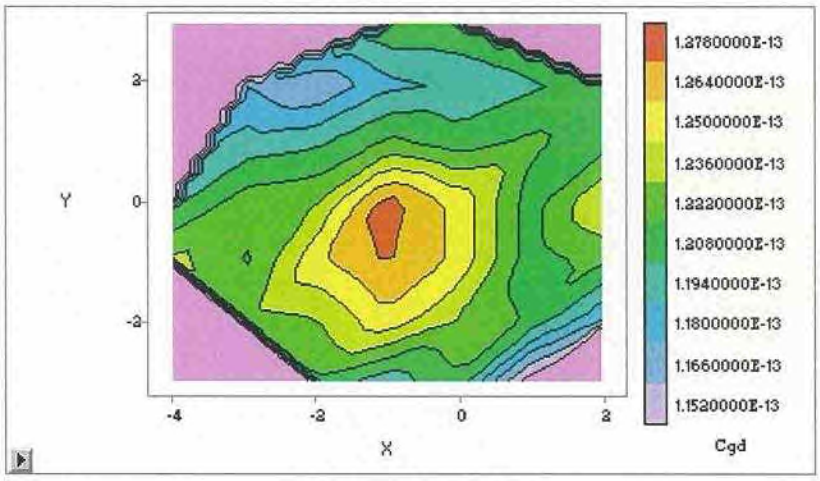

Figure 11. Contours of gate drain capacitance, C_{gd} (F/mm) plotted across the 150mm GaAs pHEMT wafer. The coloured/shaded areas in the corners of the plot (outside the wafer) are artefacts.