

DESIGN AND TESTING OF HIGH VOLTAGE RF ELECTRONICS

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Introduction

When one mentions High Voltage RF electronics, one thinks of the valve amplifier where the anode and grid supplies can be in the hundreds if not thousands of volts. But in a world where low voltage solid state devices are more usual, is there still a place for HV RF? We believe that there is, and to show our confidence in this, Roke has invested in a world beating High Voltage Testing Facility.

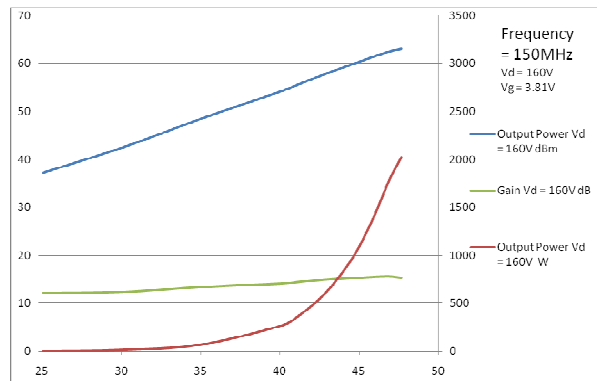
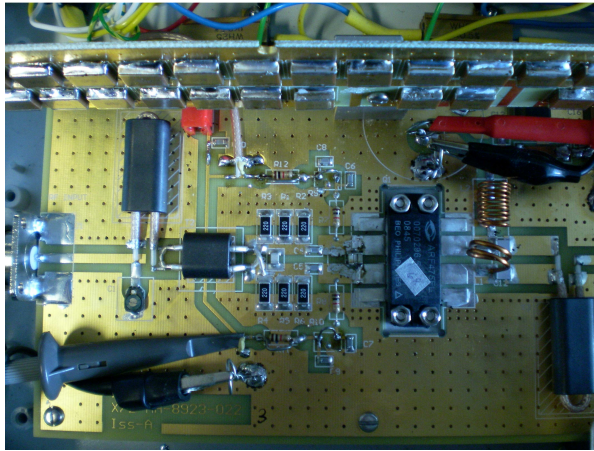
In this paper we will describe some of the recent HV RF activities that have been performed at Roke. The paper concentrates on work to significantly extend the duty cycle of a VHF SSPA design to make it more attractive for scientific, medical, and other less obvious applications where valve amplifiers still dominate.

We shall also discuss techniques and infrastructure for safely testing HV RF devices, from relatively simple interlocked test jigs to the workings of our new High Voltage Testing Facility.

Extending the duty cycle of a VHF SSPA

Previously we reported a low cost, high power, high voltage solid state amplifier which used commercially available MOSFET devices to achieve over 2kW of pulsed power [1]. This was designed for an application which required very short pulses and very low duty cycle (roughly 100 μ s pulse length and 0.1% duty cycle).

VHF SSPA and results



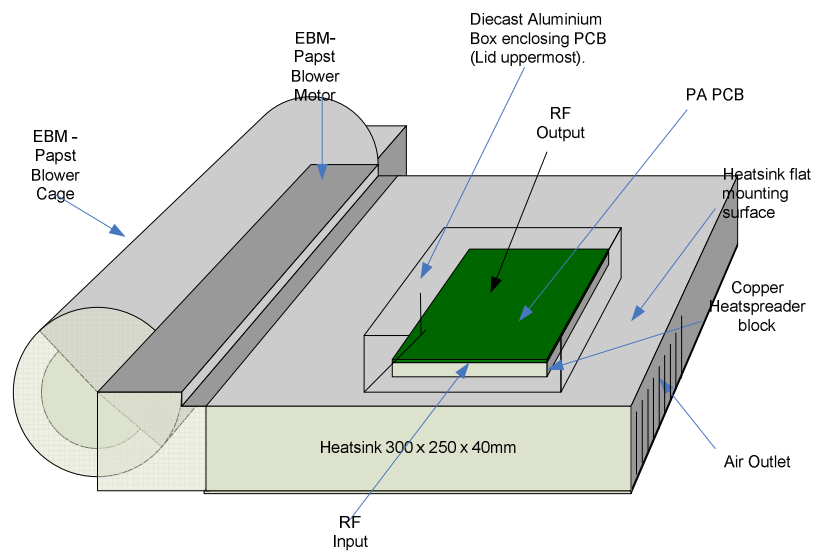
Following this exciting result, Roke conducted some market research into other applications and markets where this type of amplifier might be of value. Our research showed that the main exploitation routes were in the Medical, High Energy Physics, and EW areas. Further discussions with stakeholders showed that for our amplifier to be suitable, a higher duty cycle would be required. Indeed most potential customers required CW operation! Having assessed the market we decided to concentrate on improving the duty cycle.

For solid state devices a major contributing factor to the degradation of their performance with longer pulse lengths and higher duty cycles is the heat generated in the device. With Si MOSFETs the “on-resistance” of the device increases with temperature, and so in a worst case scenario, this leads to thermal runaway and eventual device destruction. The Junction Temperature is defined as the highest temperature of the actual semiconductor and can be significantly higher than the temperature of the exterior of the device packaging. The maximum junction temperature can range from below 100° to over 200°C depending on the technology.

The junction temperature should be kept as low as practically possible by good thermal design practices. The choice of the device packaging plays a major role in this. In short pulse/low duty cycle operation, this is not as important as the device has time to return to ambient temperature during the “off” period. However as the pulse length and/or the duty cycle increase then thermal issues become more critical. It has been demonstrated that solid state technologies suffer degradation in their performance as the pulse length and/or duty cycle is increased [2].

Microsemi provides quite detailed instructions for methods and techniques for mounting their devices in the most thermally efficient manner [3]. In the original implementation of the VHF SSPA the duty cycle was considered to be so low that we were not concerned with thermal aspects. A thin aluminium baseplate was used in the design but this was mostly to provide mechanical support to the device and PCB. We decided to make better use of this baseplate and conducted some thermal analysis using a commercially available solver. We decided on thickening the baseplate and changing the material to copper. This combined with an application of thermal grease between the device and the baseplate would help to remove the unwanted heat. The next issue to address was having moved the heat from the device, where would we dissipate it? The answer lay in a heatsink with forced air cooling.

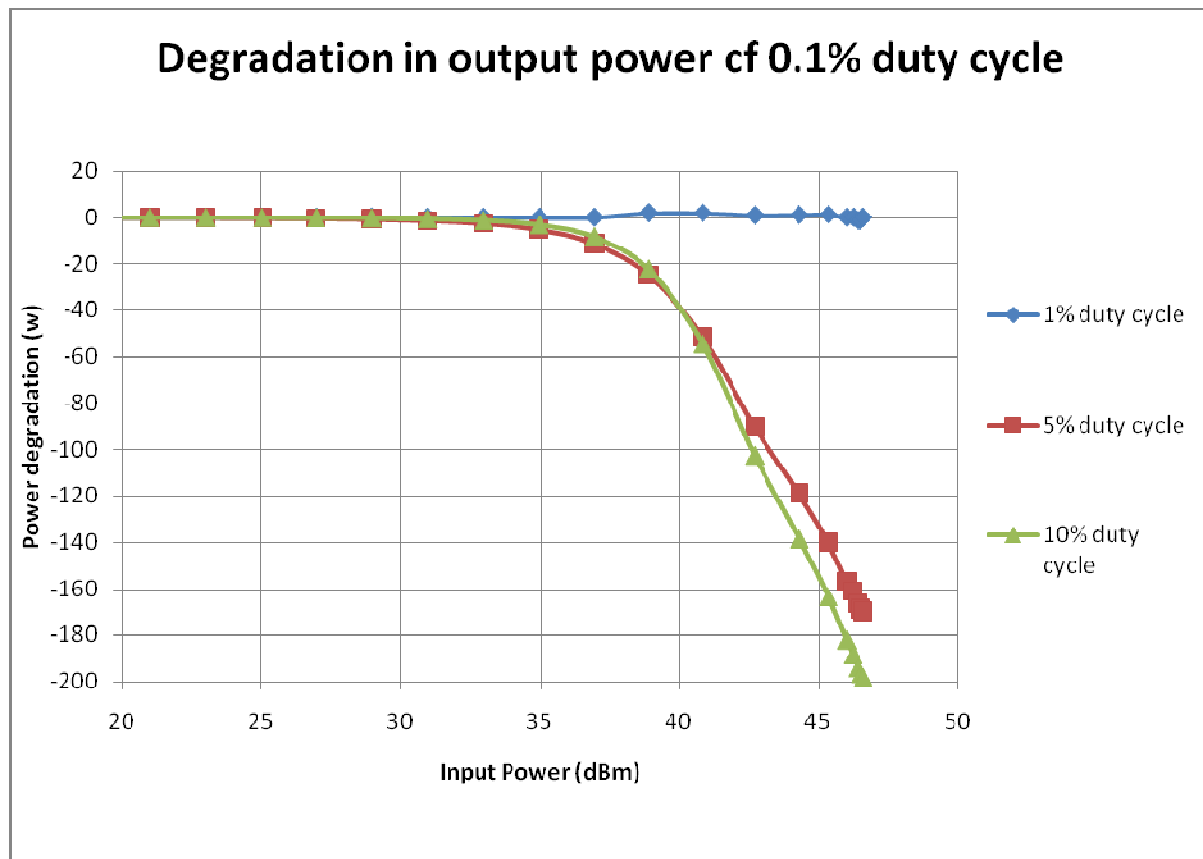
High Power VHF SSPA Physical Layout
Conceptual Diagram.



The temperature of the baseplate was monitored close to the where the device was mounted using a thermocouple. We also increased the charge storage of the test system by increasing the storage capacitance. This also required modification to the charging circuit to keep the RC time constant to a reasonable value.

Results

Measurements were made for various duty cycles and various pulse lengths. It was found that the maximum duty cycle that could be realistically achieved was 10% representing a hundredfold increase in the duty cycle over the earlier reported results. The average output power in the pulse was measured as a function of input power. The measurements were referenced to the output power for the SSPA when operated at 0.1% duty cycle. The pulse length (i.e. “on” time) was kept at 340us for all measurements.



The above graph shows that for 1% duty cycle the performance is the same as for the 0.1% duty cycle case. However as the duty cycle is increased the output power degrades.

The baseplate temperature measurement remained constant during these measurements, indicating that the drop in performance was not due to thermal issues. If the drop in performance at high duty cycles was not due to thermal issues, then it was probably due to power supply issues. The drain supply was monitored on the SSPA board by means of a high voltage probe and a Digital Phosphor Oscilloscope (DPO). This showed that during the “on” pulse the drain voltage could droop quite dramatically (of the order of 30V), despite the addition of extra capacitance. Such modulation of the drain supply would have an adverse effect on the performance of the device. This demonstrates the need for active monitoring and deliberate modulation of the drain supply (such as is employed by Nujira with their patented HAT™ technology [4]).

Testing HV Electronics

In an age where digital electronics and low battery voltages dominate the RF and Microwave community, the art of testing HV electronics seems to have become the preserve of the electricity supply and distribution industry. Valve amplifiers with their high voltage anode and grid supplies are a rare exception. Even the tube in your living room is rapidly becoming a thing of the past.

However as shown in this paper HV semiconductors do exist, and when testing them the safety implications need to be taken into consideration. “Volts jolt but current kills” is an oft quoted simplification, but more correctly it is the total energy discharged through a person that is arguably the most important consideration. The most obvious place for storage of energy in a HV circuit is in the capacitors, but also remember that tracks on PCBs, supply cables (especially co-ax) and even inductors can store significant charge.

It is generally accepted that 3J of energy stored in a capacitor is sufficient to kill if the current path passes through the heart, and that an energy level of 10J any discharge path will result in an almost certain fatality. If we take a ‘factor of ten’ precautionary approach that stored charge greater than 0.3J is to be treated as potentially dangerous, then we can calculate that at 1kV, the total capacitance in an experiment should not be allowed to exceed 1 μ F!

S.I.D.E

When working with HV electronics, the principles of S.I.D.E. offer a good form of defence;

- Switch off** i.e. remove the source of mains power from the experiment
- Isolate** i.e. provide a suitable air gap in power supply chain
- Discharge** i.e. bleed any residual hazardous stored energy to earth
- Earth** i.e. clamp the experiment to earth

How this is realised can be scaleable with the size and potential risk of the experiment from simple interlocked boxes to major facilities such as Roke’s High Voltage Test Facility (HVTF) [5].

The VHF SSPA described above was tested using an interlocked safety box. The box was rated to withstand energies of up to 1J. The lid incorporated DPDT switches which connected the device and storage capacitors to the power supply when the lid was closed, and connected the device and the storage capacitors to earth through dump resistors when the lid was opened. Key elements of this design included multiple switches in an attempt to prevent “user intervention” and redundancy in discharging circuits and warning signals in case of component failure.

A modified version of this safety box was supplied to a customer to enable production testing of a HV amplifier design. This enabled them to test production batches safely and quickly and increased their test throughput significantly.

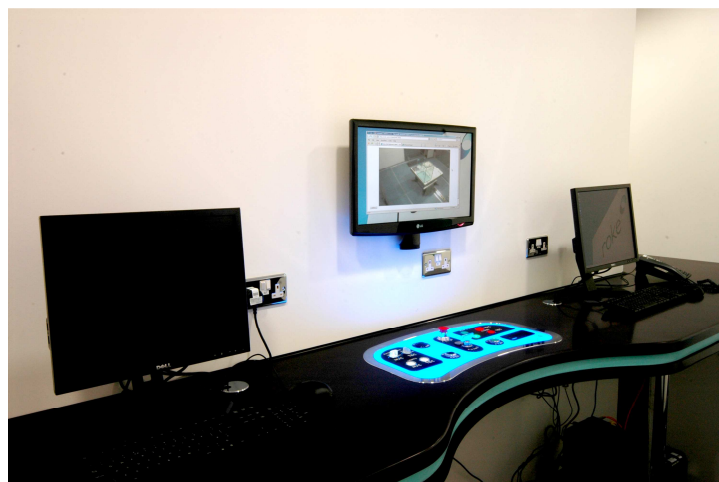
At the other end of the scale are test facilities such as the HVTF. This facility consists of two screened chambers and a separate control office. The screened chambers act as Faraday Cages around the experiment and measurement equipment to prevent any leakage of the electric field. They also act as physical barriers. The principle of operation is that the experiment is contained within the main High Voltage Chamber (HVC). The second Test Equipment Chamber (TEC) contains the measurement equipment, which is galvanically isolated from the actual experiment, which in turn is isolated from the control office where the experiment is controlled and monitored. No mains voltage is able to be present in the HVC when the doors are open, by means of a pneumatically operated isolation switch. This covers the first two requirements for S.I.D.E.

Discharge and Earthing can be achieved with the aid of discharge and earth sticks, but this is heavily discouraged, and we place a requirement on the designers of each experiment that they include at the very least automatic discharge of the experiment once the supply voltage is removed. Automatic earthing is harder to achieve but we ensure that all exposed metal that could conceivably store an induced charge are earthed. This includes any object left in the HVC, even if not directly connected with the experiment (e.g. gantries and step ladders).



HVTF – High Voltage Chamber

HVTF – Control Office



Conclusion

The methods of extending the duty cycle of a pulsed VHF SSPA have been discussed and the results presented. Our efforts concentrated mostly on improving the thermal aspects of the design. We have demonstrated a hundredfold increase in duty cycle with less than a 10% drop in output power. We now believe that this amplifier has significant potential for Medical, High Energy Physics and particularly EW applications.

Further we have discussed methods of safely testing HV electronics.

References

- [1] M. Walden, R Harrison, *et al*; A Low Cost High Power, High Voltage, 150MHz Solid State Amplifier For Pulsed Applications; ARMMS Conference; November 2009; Corby.
- [2] M. Walden, "Pulsed Power Operation of Commercially Available Silicon Carbide MESFETs" Proc. GAAS 2001 – The European Gallium Arsenide and related III-V Compounds Application Symposium, September 2001, London, UK
- [3] G Krausse, D Frey, G Choi; DRF Device Mounting Procedures and Power Dissipation; Application Note 1810
- [4] <http://www.nujira.com>
- [5] <http://www.roke.co.uk/20091029469/press-releases/roke-launches-world-first-in-high-voltage-testing.html>