The Design and Evaluation of a Plastic Packaged Single-Chip FEM for 28GHz 5G

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Abstract

The Front End Module (FEM) will be an essential component in future mm-wave 5G systems. It consists of a PA, LNA and transmit/receive switch to allow time division duplex (TDD) operation and must demonstrate high linearity in transmit mode and low noise figure in receive mode. This paper describes the design, realisation and evaluation of an FEM MMIC for the 28GHz 5G band (27.5 to 28.35GHz). The part was developed on a 4V, 0.15µm enhancement mode GaAs pHEMT process and so only positive supply voltages are required. The compact, low-cost 5mm x 5mm plastic overmoulded QFN package means that the MMIC is suitable for the high volume and low cost manufacturing that will be required for 28GHz 5G systems.

The transmit path is optimized for high efficiency when backed-off for linear operation. When driven at 1dB gain compression it produces an output power of around 20.2dBm at a PAE of 20%. When backed off for linear operation, to an IMD3 point of -35dBc, the measured PAE is 6.5%; an impressive result that demonstrates simultaneous linear and power-efficient operation. The measured receive path gain is around 13.5dB with a noise figure of around 3.3dB. The receive path also demonstrates impressive linearity for a modest power consumption of just 40mW with a measured IP3 of 20dBm.

Introduction

The mmWave 5G research and development activities of the industry's key players are now well advanced to the point where custom components have been specified designed and evaluated with the expectation that roll-out will commence in the very near future. One essential component required to enable future mm-wave 5G systems is the Front End Module (FEM), which provides the final stages of amplification in a transmitter and the earliest stages of amplification in a receiver together with transmit/receive (Tx/Rx) switching of the RF path to allow time division duplex (TDD) operation. The FEM must demonstrate high linearity in transmit mode and low noise figure in receive mode. Because mm-wave 5G systems are likely to include electronic beam steering using phased array or switched antenna beam architecture, they will contain multiple FEMs. This means the FEM must also be highly efficient, compact and low cost.

This paper describes the design, realisation and evaluation of an FEM MMIC for the 28GHz 5G band (27.5 to 28.35GHz) which satisfies all of the above requirements. The part was developed by Plextek RFI and designed on WIN Semiconductors' PE-15 process which is a 4V, 0.15µm, enhancement mode GaAs PHEMT process. It is realised in a compact and low-cost 5mm x 5mm plastic overmoulded SMT compatible QFN package making it suitable for high volume, low cost manufacture. It comfortably covers 27GHz to 29GHz and so encompasses the full 28GHz 5G band.

28GHz 5G Transmit RF Front End Architecture

As 5G systems will require linear amplification, the design of the FEM's transmit path focused on achieving high efficiency when operating at back-off. A target PAE of 6% when operating with IMD3 levels below -35dBc (around 7dB backed-off from P-1dB) was specified. When driven at 1dB gain compression the RF output power (P-1dB) was specified at 20 dBm. For the receive path, a noise figure of below 4 dB (including the switch and packaging losses) was required. Very low current consumption was essential and a target of 15 mA maximum from the +4V supply was specified.

Figure 1 is a block diagram showing the functionality of the FEM MMIC. The transmit signal path is the top half of the diagram, running from left to right with the input at the pin labelled 'PA_RFin'. The RF input signal is amplified by a 3 stage PA, which is followed by an RF power detector. The signal is then routed to a single pole double throw (SPDT) Tx/Rx switch and on to the antenna port. The on-chip directional power detector allows temperature compensated monitoring of the transmitted RF output power. The detector output is given by the difference between the voltages 'Vref' and 'Vdet'. An on-chip 'PA Enable Circuit' facilitates fast on/off switching of the PA and is controlled by the (active low) logic signal 'PA_ON'. This is used to rapidly power up and power down the PA when switching between Tx and Rx mode such that it draws a mere 0.1mA when not in use, maximizing the overall system efficiency.

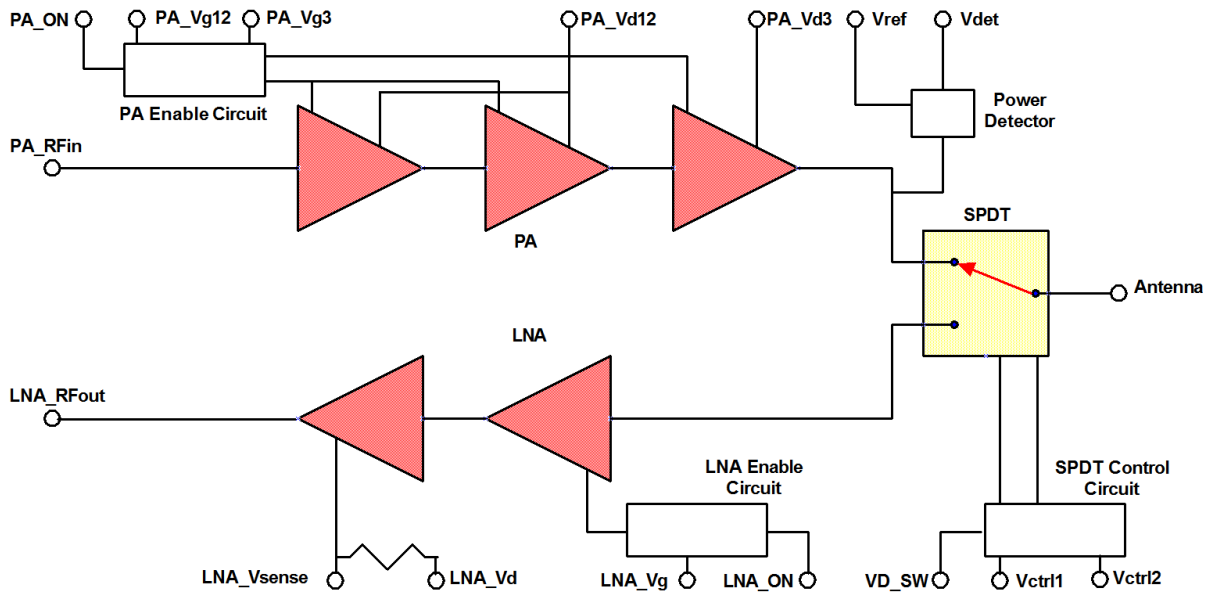

Figure 1: Block Diagram of the FEM IC

The PA is typically operated backed-off from compression to preserve modulation fidelity of the transmitted signal. With this in mind, the design approach adopted was to optimize the PA's performance when operating at 7dB back-off from 1dB compression (P-1dB). A deep class AB bias scheme was utilised to allow the Power Added Efficiency (PAE) to be optimised at this operating point. The design commenced with selection of the optimum transistor size for the output stage followed by load-pull simulation trials to assess the optimum impedances for best linearity and PAE at back-off at different quiescent bias conditions. The trade-off in gain, linearity and PAE was then evaluated and the optimum bias condition determined.

Optimum transistor sizes for the driver and pre-driver stages were selected as the design of the complete 3-stage PA progressed. Again careful trade-offs were considered; larger transistor sizes improve the overall linearity but reduce the PAE. With the size and bias of all transistors selected the detailed design of the matching and biasing circuitry could proceed. The layout was considered from an early stage of the design process to ensure a practical implementation was possible without incurring unacceptable parasitics. A common gate bias line was used for stages one and two (applied at pin PA_Vg12) and a separate bias line for stage 3 (PA_Vg3). This allowed the possibility of separately optimizing the two voltages for potential linearity or PAE improvements to the PA. The drain supplies were similarly applied through two separate pins, although these were connected on the PCB; the +4V drain supply is applied at 'PA_Vd12' and 'PA_Vd3'.

The SPDT switch is a series-shunt design with improved linearity incorporating multiple transistors in both the series and shunt arms [1]. The off-state capacitance of the transistors limits the inherent isolation of the off-state device at high frequencies; at 28GHz the switch transistors will have an isolation of just a few dB [2]. Reducing the transistor size to improve the inherent isolation increases the on-state insertion loss and degrades its linearity and so was not an option. The approach taken was to include on-chip inductive compensation to improve the off-state isolation. Care was taken to ensure low insertion loss in the on-state to enable a high output power from the transmit path and a low noise figure from the receive path. The switch is controlled by a single bit, 'Vctrl1', which is set to 4V for Tx mode or 0V for Rx mode. Single bit control is facilitated by the 'SPDT Control Circuit' which is essentially a 1 to 2 line decoder. The combined supply current drawn by both the control circuit and the SPDT itself is just 1mA from the +4V applied at 'VD_SW'.

The receive path input is at the 'Antenna' pin which is routed to the input of a 2 stage LNA by the SPDT. The output of the receive path is at the pin labelled 'LNA_RFout'. As with the PA, the LNA also has a fast switching enable circuit such that the LNA draws as little as 0.1mA when not in use. A key part of the LNA design process was to produce a design which had low current consumption but good noise figure and adequate linearity. Selection of appropriate transistor sizes was an important first step. Multiple short fingers were used to reduce the gate resistance of the transistors and improve the noise figure. Series inductive feedback was added to both stages to shift the impedance required for optimum noise figure closer to that required for a conjugate match and optimum gain.

The first stage of the LNA was optimised for noise figure but still had to produce enough gain to adequately reduce the impact of the second stage noise figure. The noise figure of the second stage is not as critical, and this stage was designed with higher gain than the first. The resulting LNA design requires just 10mA of DC supply current from its +4V supply. The gate bias voltage is applied at pin 'LNA_Vg' and the +4V drain bias is applied at 'LNA_Vd'. The 'LNA_Vsense' pin is provided to allow for bias current monitoring. Monitoring the bias current allows control of the gate voltage to compensate for changes in environmental conditions, for example a change in temperature. When correctly biased this monitoring pin is at 3.9V. The use of an enhancement mode process meant that only positive supply voltages were required, making the MMIC very convenient for system integration.

To ensure good RF performance from the various blocks, careful EM simulation was essential. A step by step approach was adopted adding a part of the circuit to the EM simulation at a time with the rest of the block still simulated using PDK (Process Design Kit) models. As the IC was destined for

packaging in an overmoulded plastic package, the presence of the moulding compound on top of the IC also needed to be accounted for in the EM simulation.

Figure 2 shows a photograph of the FEM MMIC die. The die measures just 3.38mm x 1.99mm. Its pad / pin positions are similar to those shown in the block diagram above although it incorporates a number of GND pads in order to make it fully RF on Wafer (RFOW) testable. It was designed to be packaged in a low-cost plastic overmoulded 5mm x 5mm QFN. In addition to accounting for the effects of the moulding compound, the RF transition from IC to PCB needed to be carefully designed. A custom leadframe was designed to facilitate this and the RF ports of the package are all implemented as ground-signal-ground interfaces.

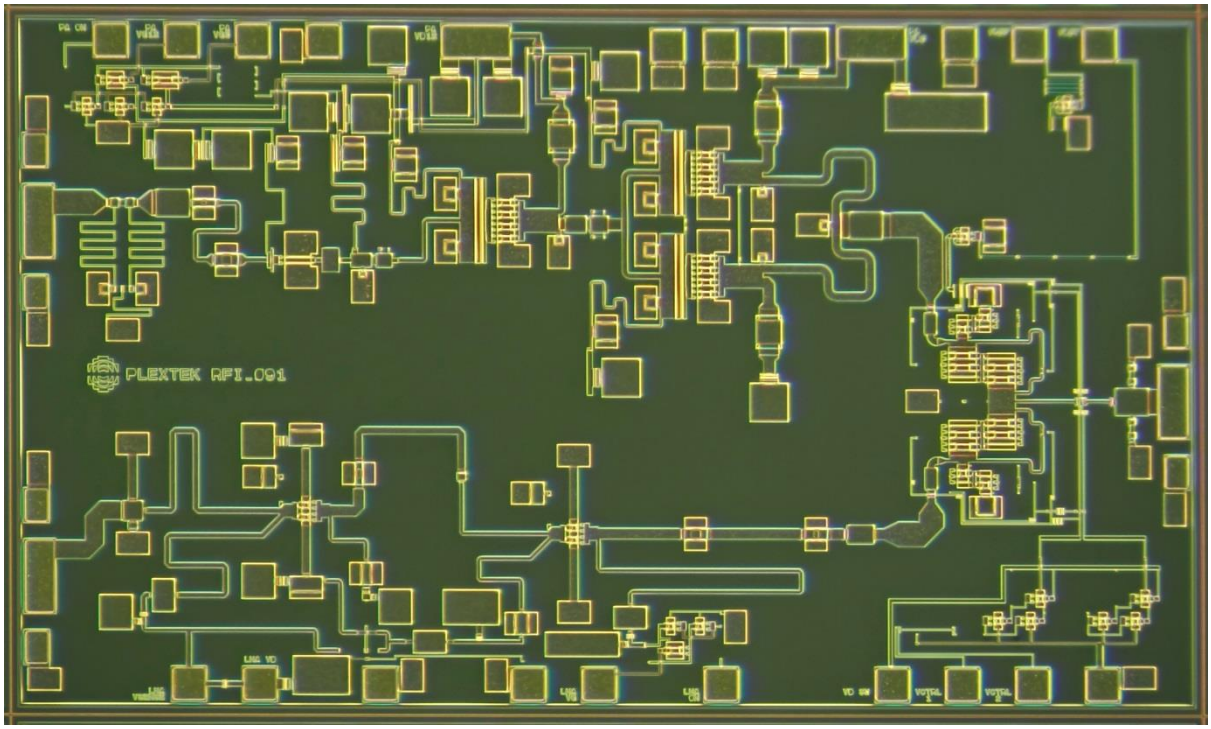

Figure 2: Photograph of the FEM die

Measured and Simulated Performance

Prior to packaging, several of the die were tested RFOW which confirmed that the first pass design had been successful. The RFOW results are not presented here all measurements were made on a packaged assembled IC mounted on a representative evaluation PCB.

The evaluation PCB was designed using a low cost laminate PCB material suitable for volume mass production. Samples of the packaged FEMs were assembled on to the evaluation PCBs; all of the measured performance is calibrated to the package pins on the evaluation PCB and include the effects of the IC to PCB transition. A TRL calibration tile was designed to allow the calibration of the measured performance to the reference planes of the package. A photograph of one of the evaluation PCBs next to a TRL calibration PCB is shown in Figure 3.

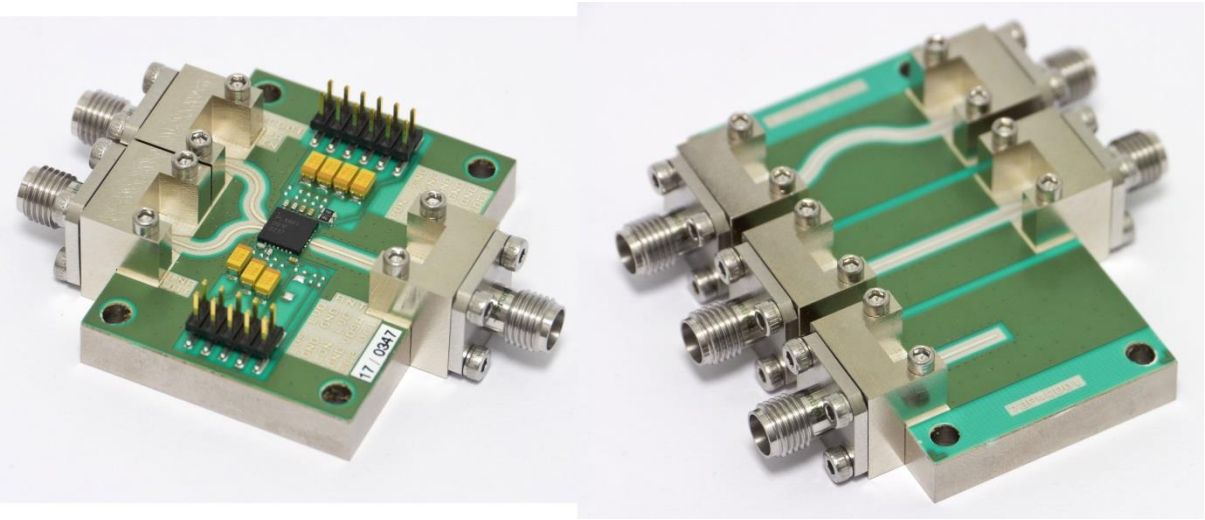

Figure 3: Photograph of FEM Evaluation PCB and TRL Calibration Tile

Evaluation results referenced to the package's RF pins are shown below for the packaged FEM MMIC mounted on the PCB. Throughout the evaluation, a commercially available multi-channel DAC and ADC IC was used to control and monitor the FEM. Conveniently the FEM does not require any negative voltages as it was designed on an enhancement mode process.

Figure 4 shows a comparison of the measured to simulated S-parameters of the Tx path of a typical FEM. The solid traces represent the measured data and the dashed traces are simulated results. In this mode the LNA is powered down, the SPDT control bit 'Vctrl1' is toggled high and the PA biased to around 70mA total quiescent current from +4V. Small signal gain (S21) is 17.1dB ±0.4dB from 27GHz to 29GHz. The input return loss (S11) is better than 18dB across the band. The output is matched for best PAE at back-off rather than best S22 but the measured S22 (not shown) is 8dB or better across the band.

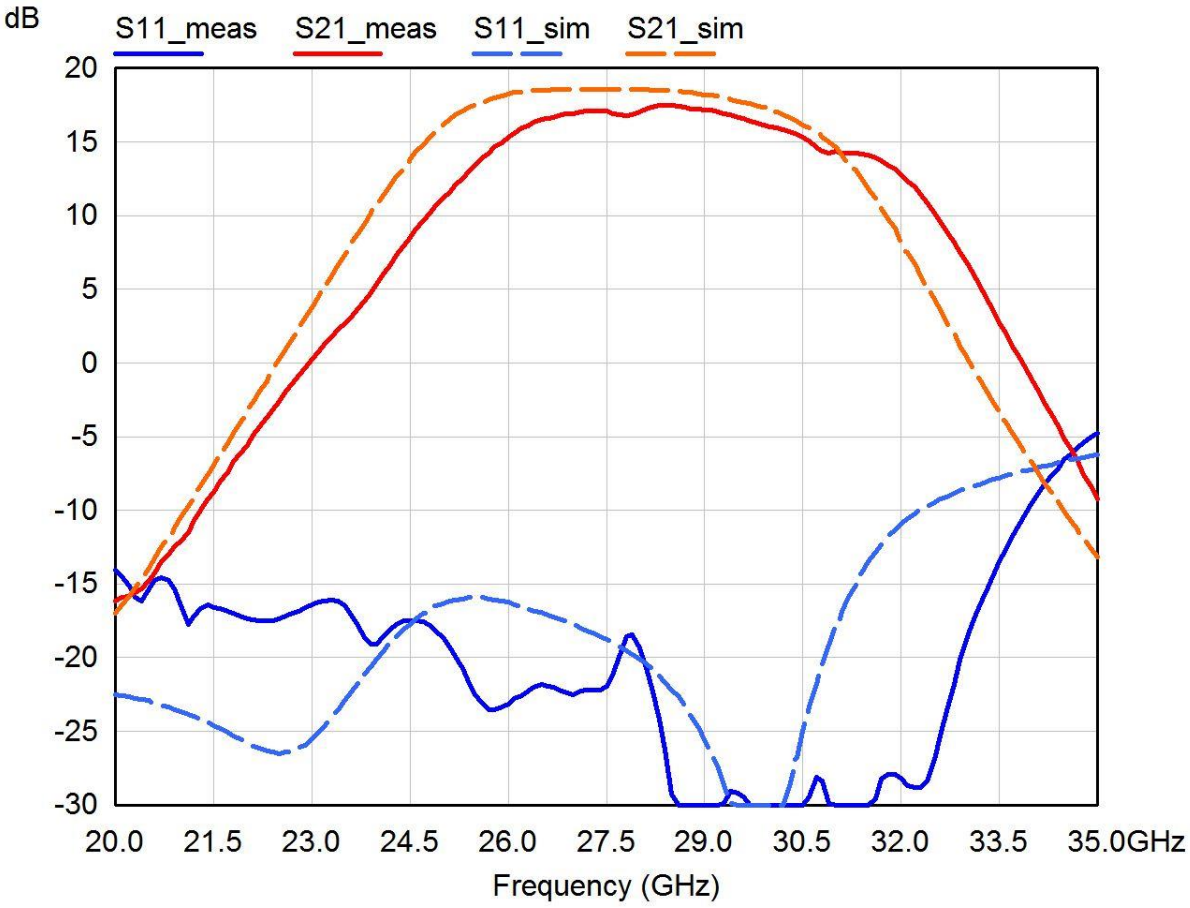

Figure 4: Measured and Simulated S-parameters of Tx Path

To reflect the wide channel bandwidths anticipated in 5G systems, the output referred third order intercept point (OIP3) of the Tx path was evaluated with a tone spacing of 100MHz. The measured OIP3 of a typical FEM is plotted in Figure 5 with the wanted output tone powers ranging from 1dBm per tone to 11dBm per tone. It can be seen that the OIP3 is around +28dBm across the 5G band and shows very little variation with tone power over a 10dB dynamic range. A plot comparing the measured to simulated OIP3 versus frequency is shown in Figure 6 and demonstrates very good agreement.

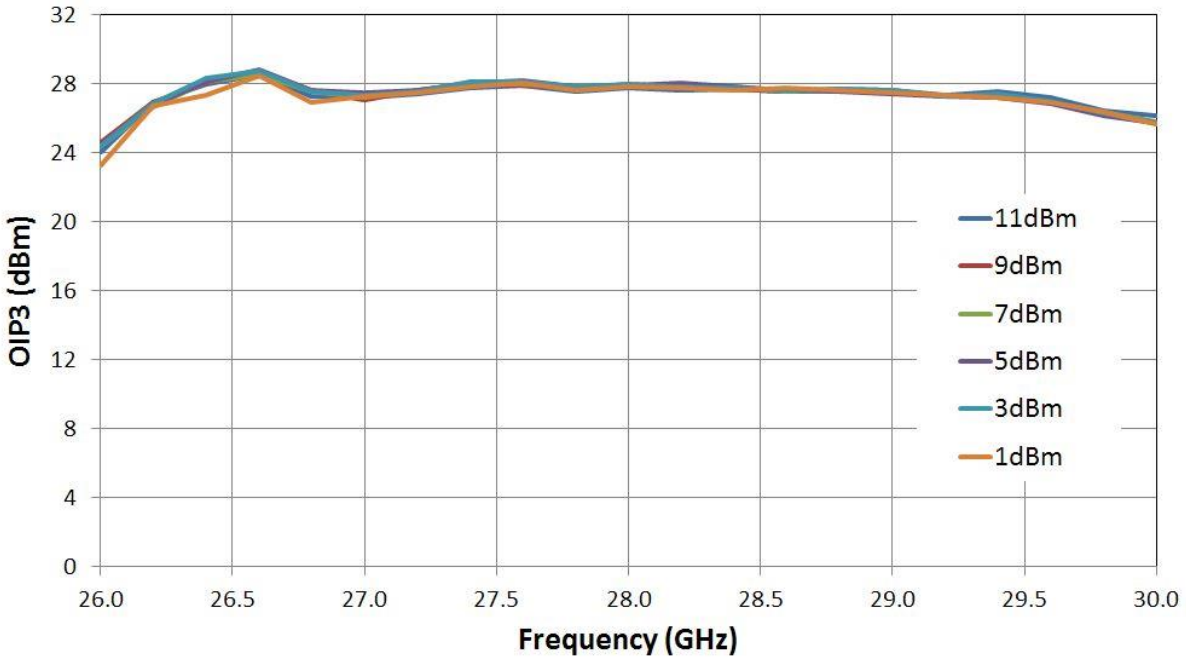

Figure 5: Measured OIP3 of the Tx Path versus Frequency for Different Signal Levels

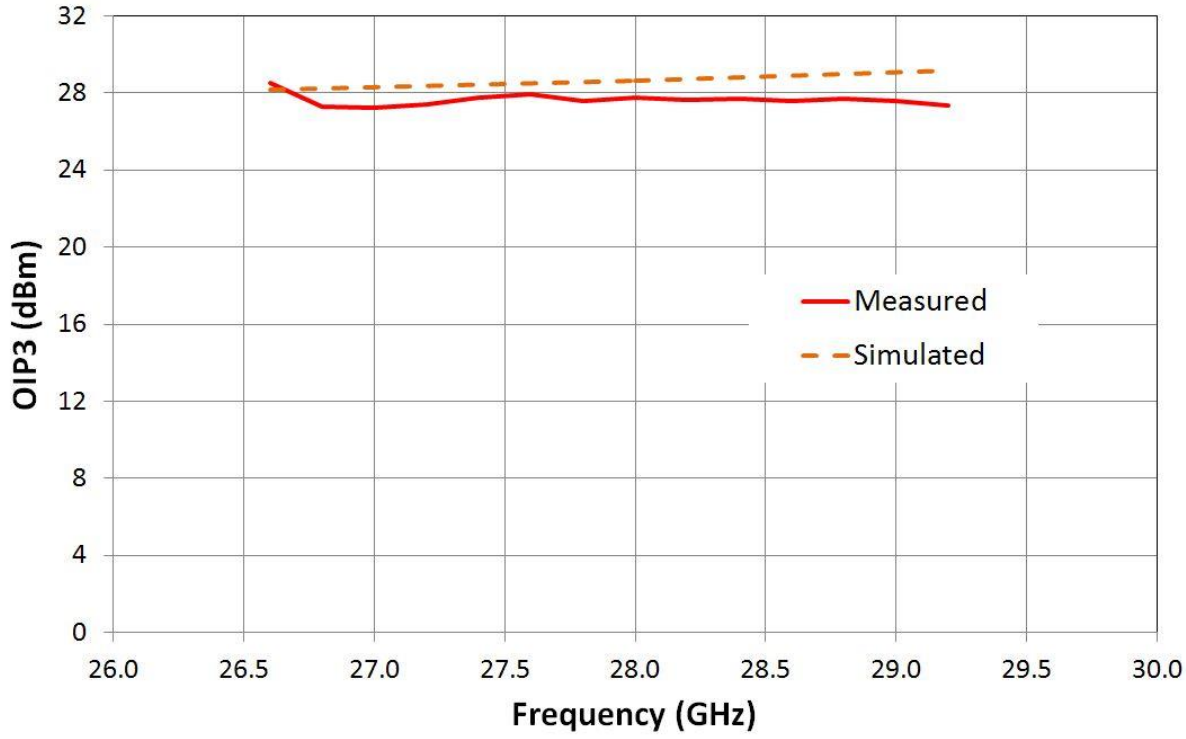

Figure 6: Comparison of Measured to Simulated OIP3 versus Frequency

To provide a figure of merit for comparative purposes, the output referred 1dB gain compressed output Power (P-1dB) and Power Added Efficiency (PAE) were also measured, although 5G systems will require linear amplification to preserve modulation fidelity. The measured performance is shown in Figure 7 and shows a P-1dB around 20.2dBm at 1dB compression, which rises to 21dBm at saturation. The PAE of the FEM Tx path is around 20%, falling slightly at the top of the band.

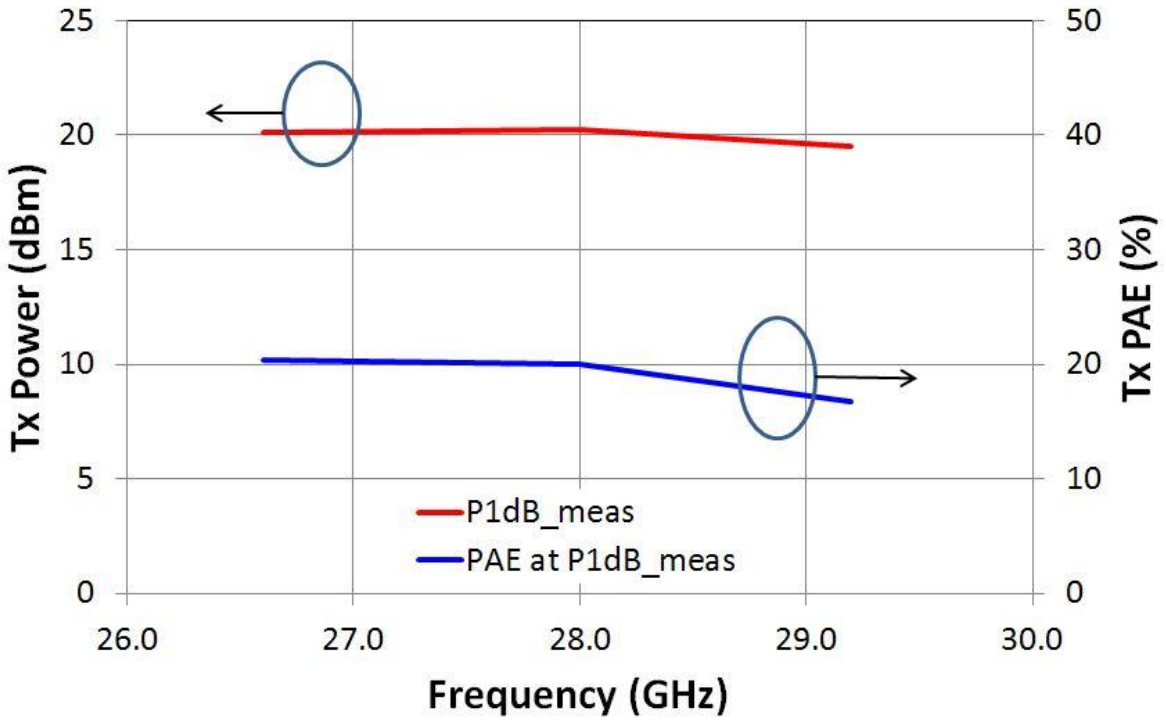

Figure 7: Measured Tx Path P-1dB and PAE versus Frequency

As mentioned above, the FEM is designed for optimum performance (OIP3 and PAE) when operated at around 7dB backed-off from P-1dB, specifically with the third order intermodulation products (IMD3) at a level of below -35dBc relative to the wanted products during a 2-tone test with 100MHz tone spacing. This operating point is close to that envisaged in the 5G system for which the FEM was designed.

A plot of the measured to simulated PAE and total RF output power when operating at an IMD3 point of -35dBc is shown in Figure 8. The measured PAE is 6.5%, which is a very good result and is largely due to the PA being designed to operate in deep class AB. The total RF output power is around 13.5dBm, which equates to an OIP3 level of +28dBm.

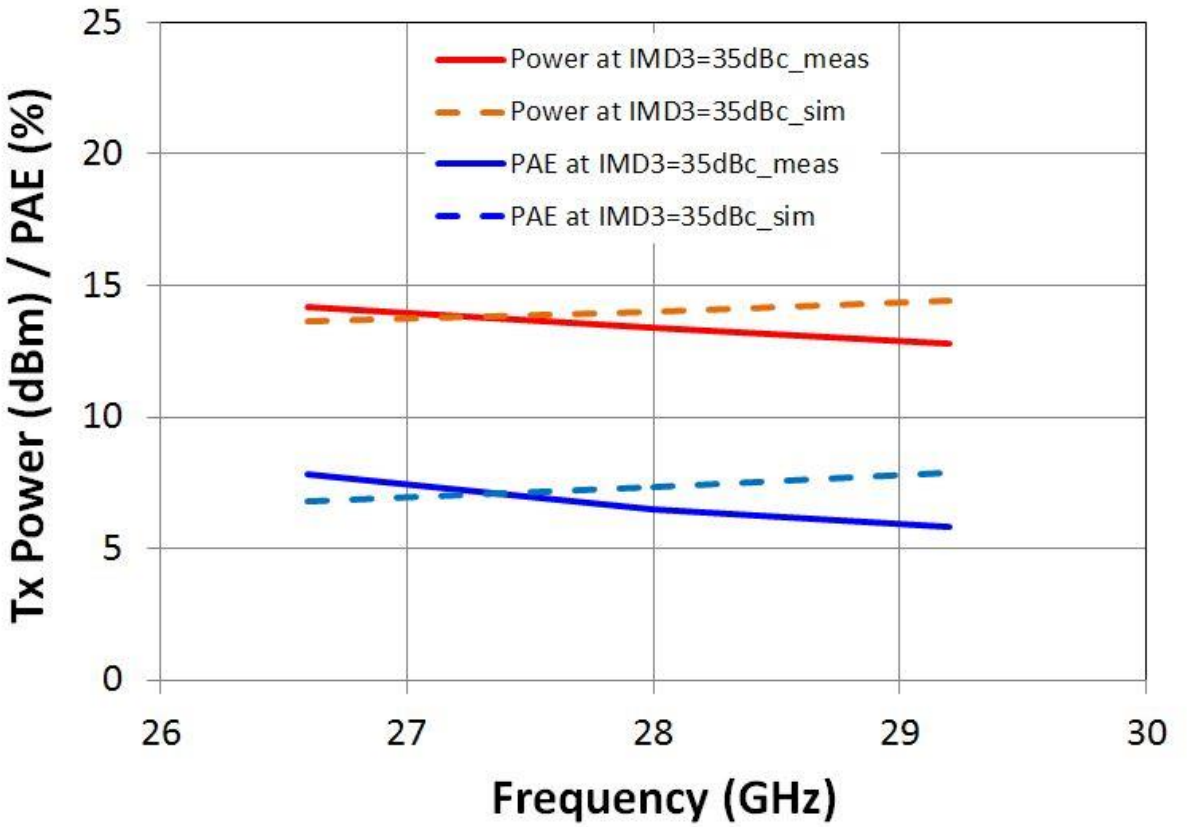

Figure 8: Measured to Simulated Tx Power and PAE Operating at ~ 7dB Backed-off

A DC voltage that allows monitoring of the RF output power is provided by the on-chip Tx power detector characteristic. The temperature compensated detector output 'Vref-Vdet' is plotted in mV on a logarithmic scale against output power in dBm over a 15dB dynamic range in Figure 9. On this scale the characteristic is linear making power monitoring easier.

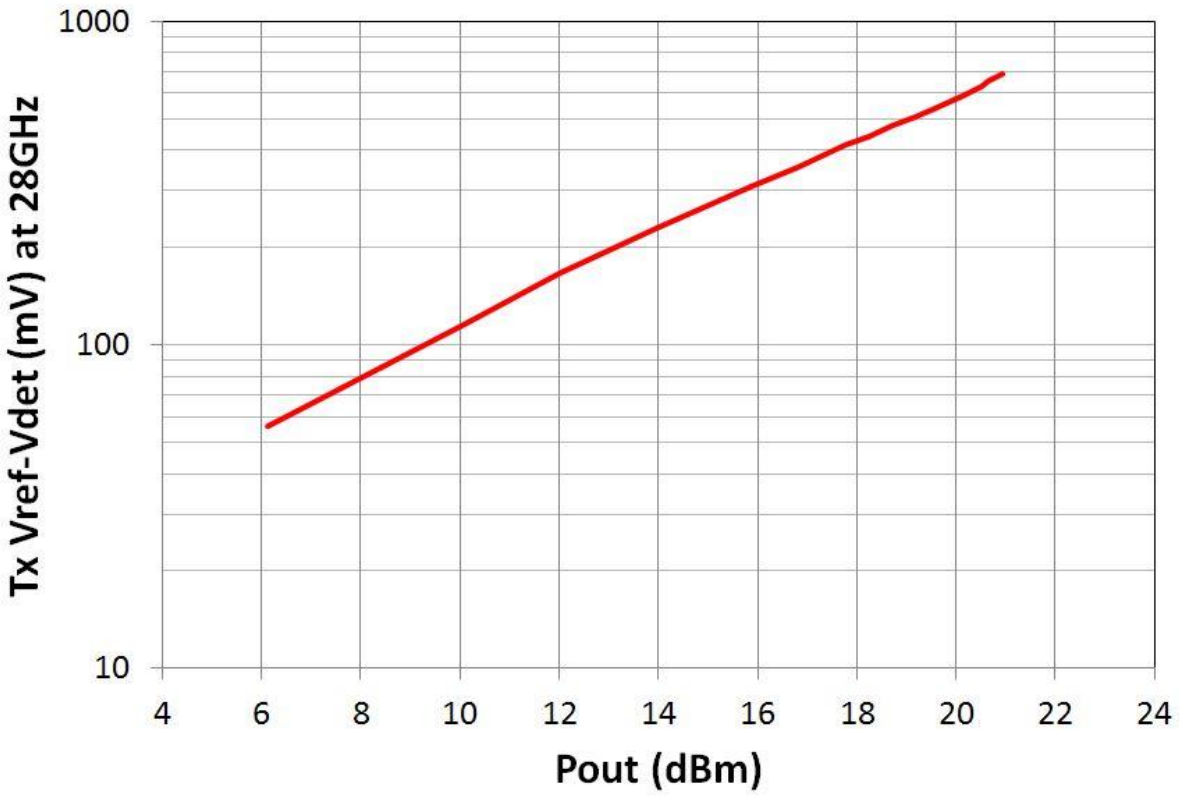

Figure 9: FEM Tx On-Chip Power Detector Measured Characteristics at 28GHz

When the Rx path of the FEM is selected the PA is powered down, 'Vctrl1' is set to 0V and the LNA biased to around 10mA from +4V with 3.9V observed on the 'LNA_Vsense' pin. Figure 10 is a plot comparing the measured to simulated gain and Noise Figure (NF). The measured small signal gain is around 13.5dB with a gain flatness of just ±0.3dB across the band. The Rx path has an excellent noise figure of typically 3.3dB from 27GHz to 29GHz band with very good agreement between simulated and measured performance.

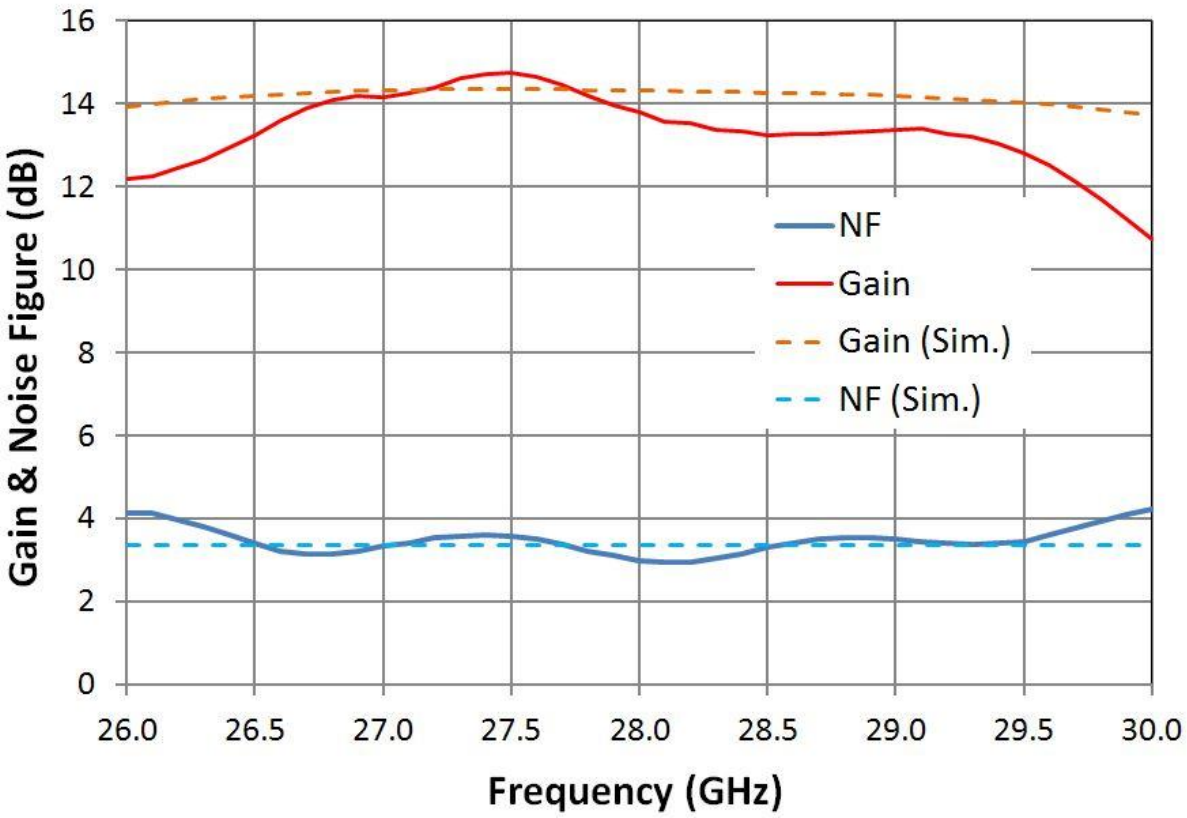

Figure 10: Comparison of Measured to Simulated Gain and NF for the Rx Path

For the modest power consumption (just 40mW: 10mA at 4V), the Rx path also demonstrates impressive linearity. Key parameters such as P1dB and OIP3 are around 6.2dBm and 21dBm respectively across the band. Figure 11 is a plot of the measured P-1dB and OIP3 versus frequency.

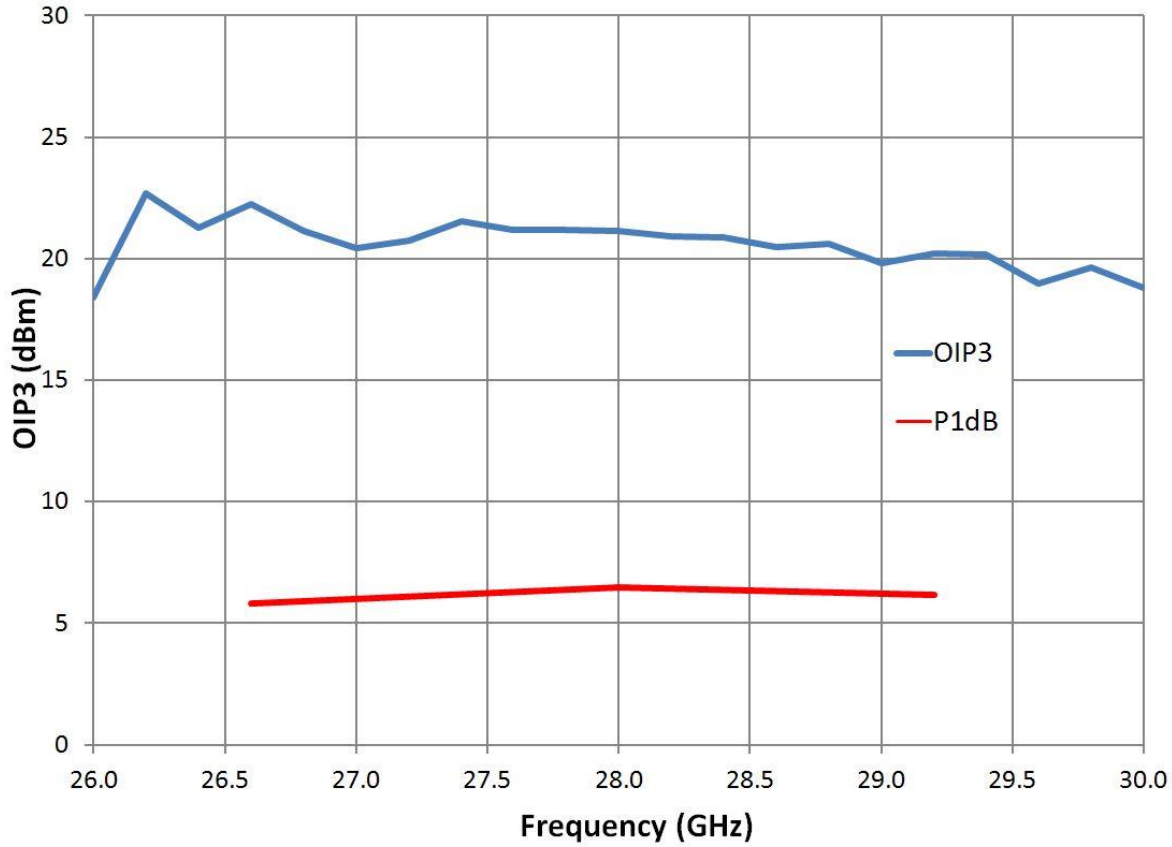

Figure 11: Measured OIP3 and P-1dB versus Frequency for the Rx Path

Summary and Conclusions

The FEM MMIC described here will potentially play a vital role in future 28GHz, 5G systems. The part has been shown to address all the requirements for integration into mm-wave phased-array or beam switched terminals and offers excellent Tx linearity and efficiency together with outstanding Rx noise figure. The key performance specifications for both transmit and receive paths were met, ensuring that the part is highly suitable for mm-wave 5G applications. The IC also includes useful features such as a Tx power detector, Tx and Rx enable circuits, an SPDT decoder circuit and Rx bias monitoring. Realised on a state of the art 0.15µm enhancement mode GaAs P-HEMT process the part is extremely easy to control and monitor using widely available multi-channel ADC and DAC ICs. In addition, the part is conveniently housed in a compact and low cost 5mm x 5mm plastic overmoulded QFN SMT package.

References

[1] Liam Devlin, “The Design of Integrated Switches and Phase Shifters”, Proceedings of the IEE Tutorial Colloquium on “Design of RFICs and MMICs”, Wednesday 24th November 1999, pp 2/1-14

[2] Stuart Glynn and Liam Devlin, “The Design of a Dual-Band PA for mm-Wave 5G Applications”, proceedings of the RF and Microwave Society (ARMMS) Conference, November 13th and 14th, 2017