PHASE LOCKING TECHNIQUES ADAPTABLE FOR A RANGE OF RF MICROWAVE SOURCES

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Abstract

The use of programmable frequency synthesisers enables the flexibility of adapting a pre-made phase-locked loop (PLL) circuit to control a wide range of microwave sources, e.g. voltage controlled oscillators (VCOs), dielectric resonance oscillators (DROs). This flexibility greatly reduces the cost and time of production and maintenance compared to the conventional method of using discrete components (e.g. frequency detector, divider etc.)
This paper discusses the methodology for the design and production of a microwave VCO and the phase locking circuit that can be adapted to frequency synthesise the VCO. Hybrid chip & wire technology on an Alumina substrate was used for the VCO and surface-mount technology (SMT) for the phase-locked loop. The computational modelling and design was carried out with AWR Microwave Office.

Programming the phase locking circuit enables the output frequency (or frequencies) to be precisely locked within the frequency range of the VCO or multiples of the VCO's frequency. This serial information is then programmed on a memory chip to enable automated operation when the unit is powered up. Whilst reducing production time and cost, this approach, achieves synthesised frequency sources up to and beyond 20GHz with competitive phase noise (e.g. 100dBc @100kHz offset), suitable for either commercial or military applications.

1 Introduction

Traditionally, phase locking of frequency sources for military applications has been achieved using discrete components (see fig.1). The principle here is the most basic, where the signal from the VCO is coupled-off, fed back and divided before it is compared with a clean reference signal. For the two signals to be compared, their frequencies have to match precisely. For an X-band frequency output of, say, 10GHz, a large divider of exactly 100 is required in order to be compared with a reference source of, say, 100MHz. If the crystal and the frequency divider have fixed frequency values the phase locked output is restricted to a fixed frequency. In the past, this problem has been overcome by the following methods: (1)

the use of multiple crystal sources and (2) programmable frequency dividers. The first method combines the sum and difference frequencies of the crystals to produce a multiple of channels [1]. This is an undesirable option mainly due to the cost of the number of crystals required, particularly if where there are a large number of channels. The preferred option is to have a programmable frequency divider; this has been the technology for decades and the range of divisions has a wide range. A programmable divider does require a microprocessor or digital controller since its operation is a digital process involving the counting of signal pulses.

The requirement of reduced size, cost and flexibility for PLL synthesisers have resulted in electronic manufacturers of PLL systems (such as Analog Devices, Linear Tech., Fujitsu, Philips , Texas Instruments) to integrate the phase frequency detector and frequency divider on-a-chip. A diagram of this is shown in fig. 2 [2]. These integrated PLL synthesisers boast a reduced size, lower cost and added design flexibility. The circuitry that encompasses the integrated PLL synthesiser can be premade to phase lock a range of VCOs. Recent advances with the improved phase noise of these integrated PLL devices has resulted in noise performance that meets most commercial and military specifications [3],[4].

In order to improve the noise performance of an N-integer PLL it is desirable to minimise the N counter value and maximise the phase detector frequency f_{pd}.[5] Given that N is an integer the maximum phase detector frequency value is limited to the size of the channel spacing Δf. If N is a fractional value however, N can be made lower and this can therefore substantially reduce the phase noise. In the past, the drawback of fractional-PLLs has been fractional spurs, but, nowadays, there are methods to supress these, e.g. analogue compensation [6]. Fractional-PLLs also have improved locking time. For high frequency applications with low channel spacing fractional-PLL synthesisers are therefore the preferred option [6]

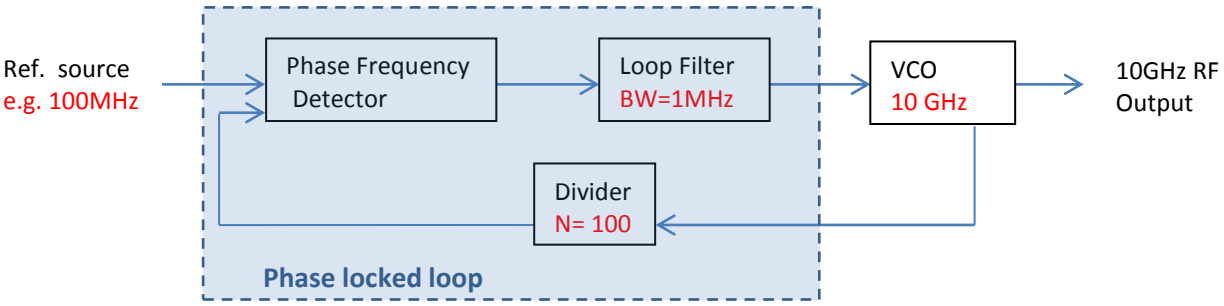

Fig 1: Block Diagram of a synthesised frequency source

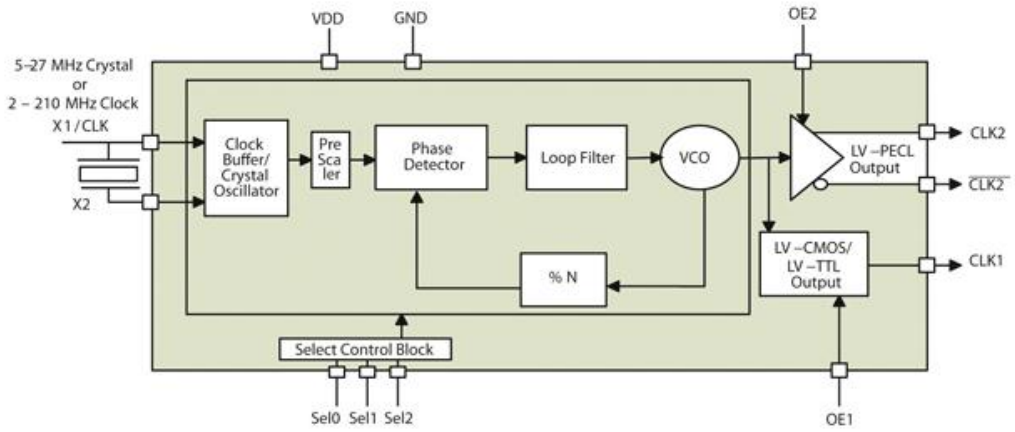

Fig 2 integrated PLL *circuit.* : Block diagram of ON Semiconductor's NB3N3020 programmable clock Multi-PLL programmable clock solutions for set-top box [2].

2 VCO Development

A VCO development at SMS Ltd has been accomplished by modelling a range of active device models and simulating these with an arrangement of passive devices so as to drive the transistor into a mode where it generates RF gain combined with negative resistance, thus producing a self-oscillating condition. These passive devices are also carefully chosen and the circuit simulated so that the self-oscillation is achieved at a predetermined frequency.

As the circuit is designed and built using chip and wire technology on a small scale there exists some amount of capacitive feedback, which can be modelled in an EM simulation. Some inductive feedback was also added from the drain to the gate of the F.E.T. in order to achieve the necessary conditions for oscillation. The oscillatory conditions were mainly determined from analysing the S-parameters; ensuring good transmission gain (i.e. magnitude S21) at the point when the phase of S21 passes through zero (as shown in fig 3a). Because the oscillation arises from negative resistance in the circuit it is necessary to ensure that the real part of the input impedance Re(Z(1,1)) is less than, say, 50Ω whilst the reactance IM Z(1,1) is zero, as shown in fig 3b.

The second-half stage of the VCO design involves the design of the varactor circuit. This was positioned at the gate of the FET (or base for the BJT). As the tuning voltage applied to the varactor is varied, the change in capacitance at the gate causes the output frequency of the VCO to vary. The varactor circuitry is to be modelled so that, this output frequency variation is linear as a function of tuning voltage, and all other oscillatory conditions are consistent across the chosen tuning range, particularly the magnitude of S21 (representing the output signal amplitude). As with the transistor model, a correct varactor model is important to achieving a good agreement with experiment.

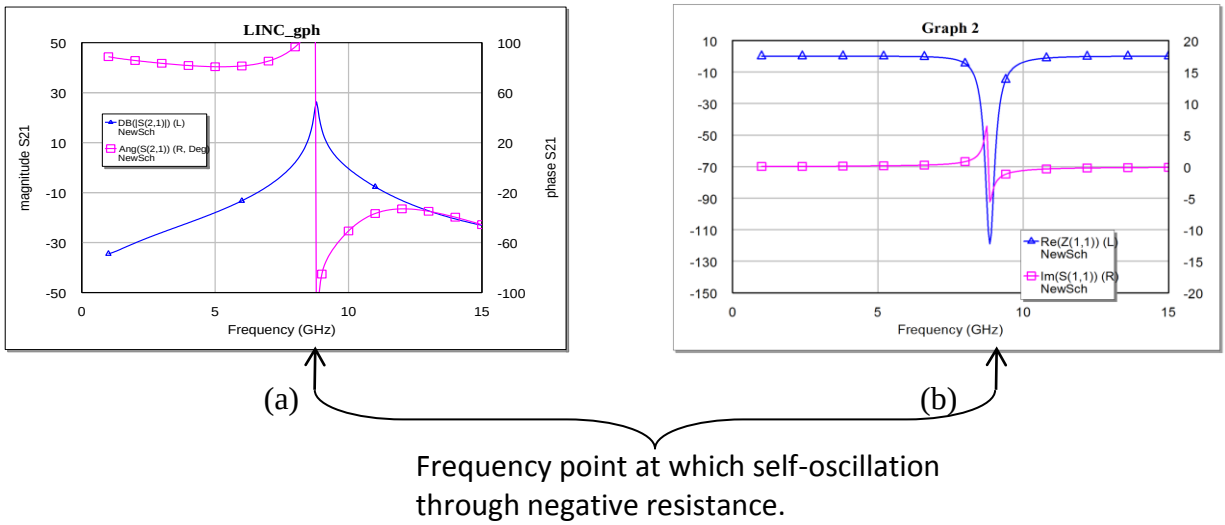

Fig 3. Plots of the (a) magnitude and phase of S21 and (b) the real and imaginary parts of the input impedance

Various VCO topologies covering frequency ranges within the range of 4 to 9GHz and wide varactor tuning of up to 1GHz, were modelled and drawn. Fig 4a shows the layout (drawn using AutoCAD) of the VCO on an alumina substrate cut to sizes of 4.8 by 4.4mm. The bare die parts of the VCO are wire bonded and the VCO is positioned on a carrier which can be fitted onto hybrid assemblies and subsystems. Fig 4b shows the fabricated VCO housed in a carrier with the output RF line leading to an SMA port.

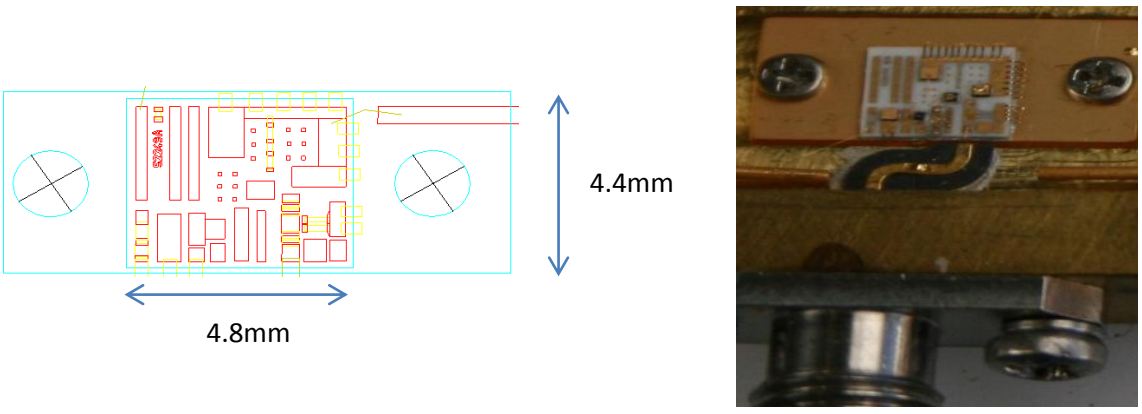

Fig 4. VCO Prototypes: (a) drawing design of mask on a carrier (b) physical build

3 The Phase Locking Circuit

A standard circuit was designed to phase lock (i.e. frequency synthesise) a VCO. The circuit, in fig 5, mostly comprises of passive components and regulators which supply and support the integrated packaged PLL synthesiser that lies at the heart of the circuit, these integrated devices are produced by various manufacturer as listed in section 1.

The PLL device is able to phase lock a VCO at user-defined frequencies by adjusting the charge-pump currents. This gives the circuit the flexibility to function with any VCO that is placed in the carrier slot. For VCOs with a different tuning slope (MHz per volts) minor adjustments to the loop filter may be required.

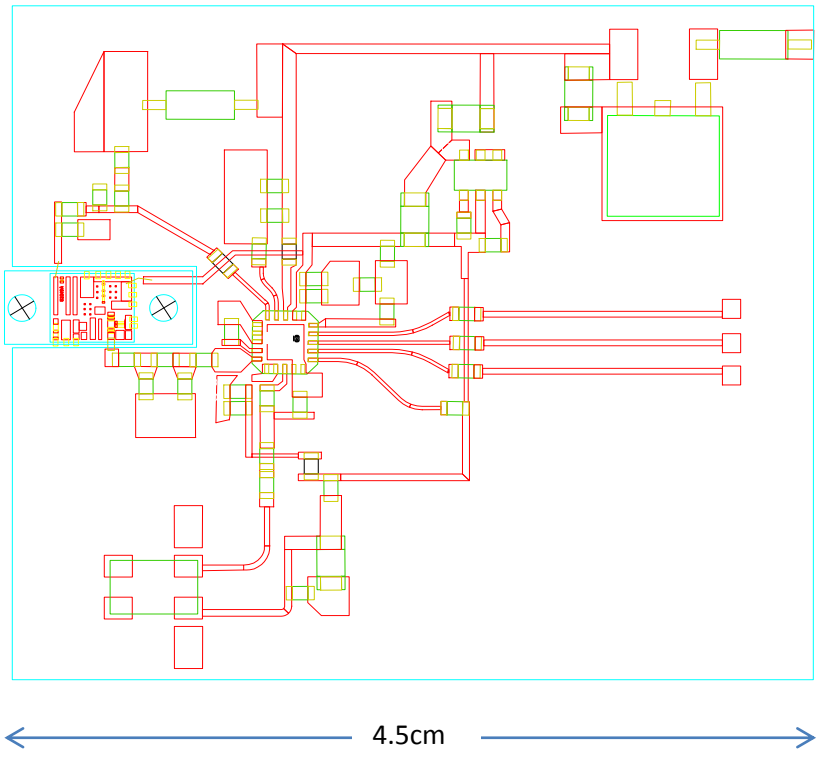

Fig 5. Design layout of the phase locking circuit

Another variation of the PLL circuitry is to synthesise external VCOs. An example of a manufactured board is shown in fig. 6. Here, the layout of the board has similarities to that shown in the drawing (in fig 5). Additions are added to this board however, for example an OpAmp to enable active filtering. Active filtering enables a wider tuning voltage required for certain types of VCOs, whereas the passive filter arrangement in fig. 5 limits the tuning voltage adjustment from 0 to 5V (depending on the charge pump power supply).

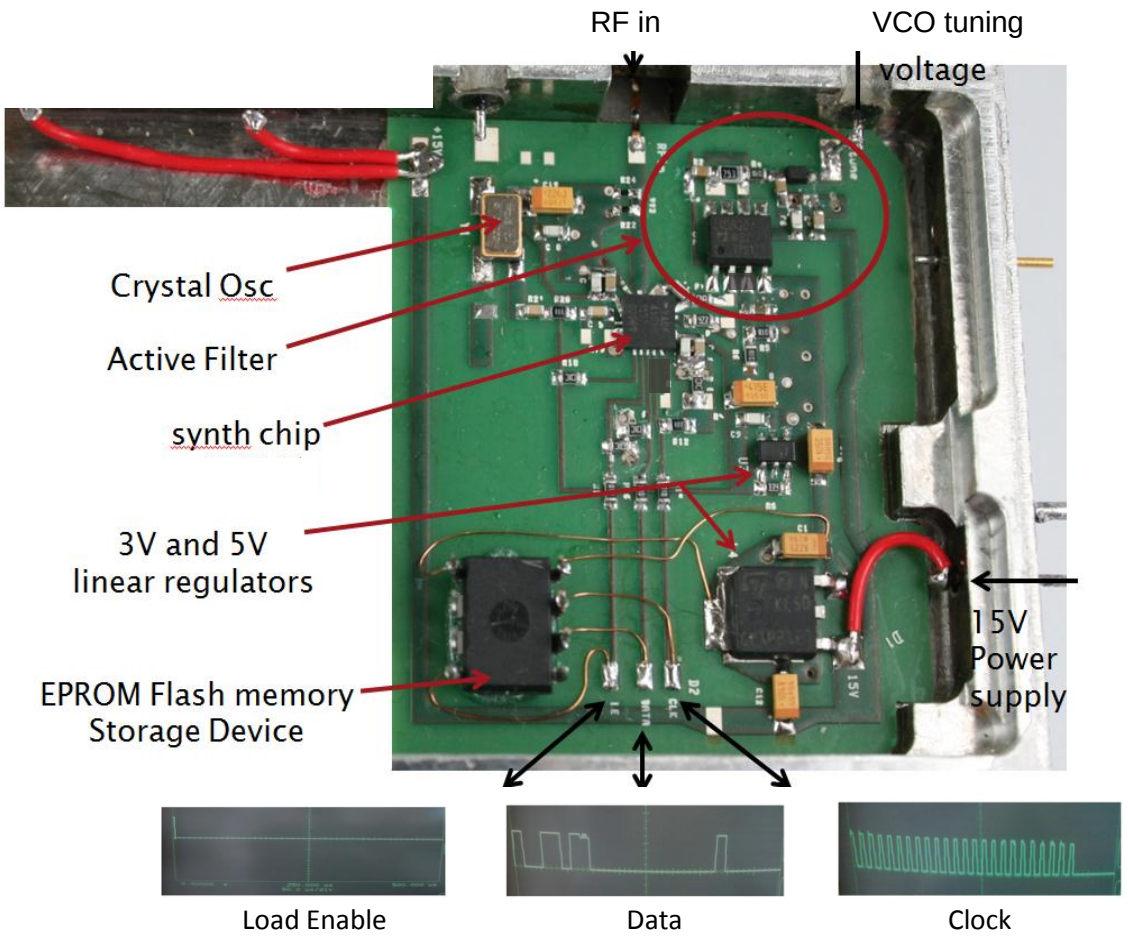

Fig 6. Hardware photo of phase locking circuit with the serial data signal traces

The other addition to this board is the EPROM Flash memory device. This is normally an essential device as this enables the unit to be synthesised at a particular frequency (or frequencies) at start-up without the need to re-program the PLL device after the power supply has been disconnected. Most PLL synthesiser devices are volatile i.e. they lose their memory when power is interrupted. Synthesis is normally achieved via serial commands fed through 3 input lines: load enable, data and clock. This contains all of the necessary data required to synthesis the frequency source. The EPROM device is pre-programmed (in assembly code) to transmit the data stream through the three lines when the power supply is connected, thus enabling immediate synthesis at start-up.

3 Phase Noise and Spurious Emissions

There are important considerations that are taken into account when designing the PLL circuit, such as thermal dissipation and RF noise. It is the RF considerations that are more subtle due to RF phenomena such as cross coupling and matching. In order to minimise phase noise and spurious emissions it is important to ensure that the RF design guidelines are followed. Focussing specifically on PLL design, a higher phase detector frequency can result in lower phase noise. Spurious emissions can be minimised by ensuring that the

charge pump currents are matched and any leakage is prevented and to ensure that the loop bandwidth is not too narrow [5].

The overall phase noise of the synthesiser unit is strongly dependant on the VCO phase noise. For a PLL circuit with an external VCO, the spectral output and phase noise is given in figs. 7a and b respectively. In this case the phase noise is -85dBc.

The loop filter on the PLL circuit is normally designed to minimise the high frequency ripple noise from the phase-frequency detector, it can also suppress spurious emissions from the detector (known as reference spurs). The design of the loop filter does present a trade-off however, between noise suppression and settling time: with more damping of noise the settling time is increased. The loop filter design that produced the outputs in fig's 7a and b was modified and the measured results are shown in figs. 8a and b. The modified filter (in fig. 8a) produces a more distinctive (narrowband) peak than that shown in fig. 7a. By comparing the phase noise plots (figs 7b and 8b), modifying the PLL loop-filter has shown in significantly reduce the close-to-carrier phase noise by over 5dBc/Hz. (within a 0 to 500kHz offset).

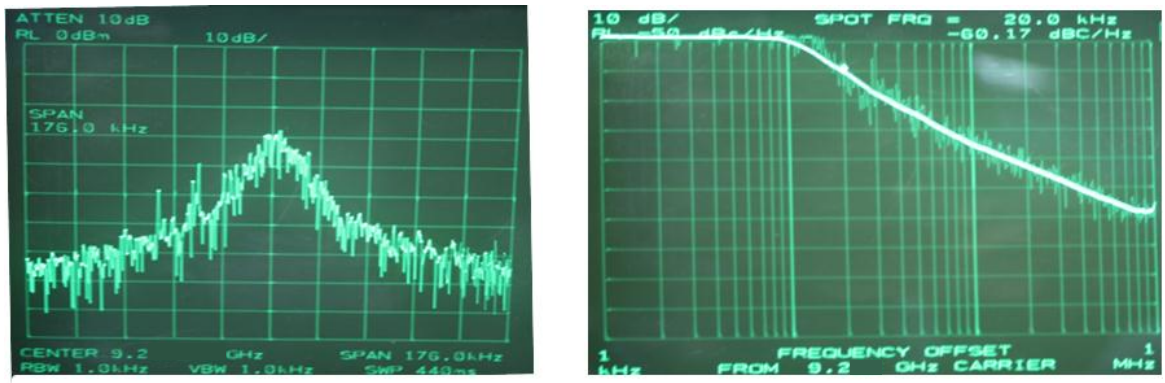

Fig 7(a) spectral response and (b) phase noise plot of a phase locked VCO

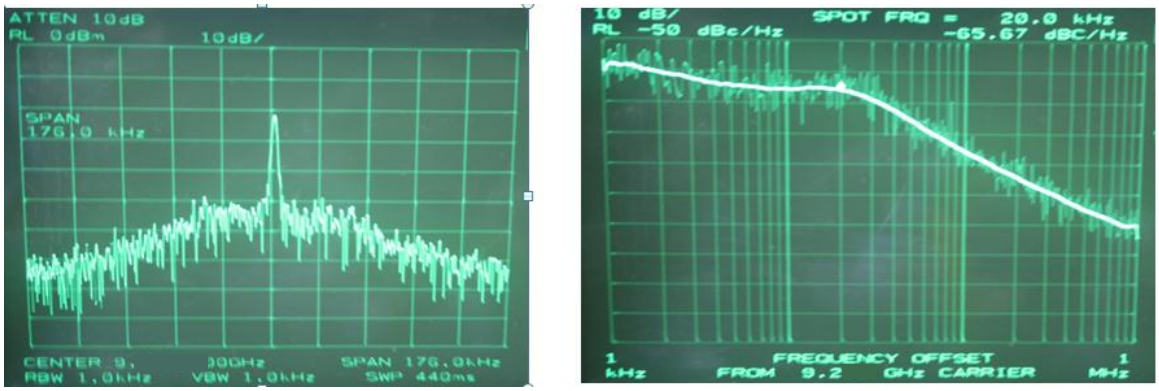

Fig 8(a) spectral response and (b) phase noise plot of a phase locked VCO with a modified loop filter

4 Conclusions

It has been described, in this paper, how a range of different VCOs can be phase locked with a predesigned programmable frequency synthesiser. This approach results in reduced cost and time of production compared to the conventional method of using discrete components.

The design and manufacture of a microwave VCO was described using the chip & wire technology and how a pre-designed PLL circuit board can synthesise this, or indeed, any type of VCO. A programmable PLL device is able to precisely select the locking frequencies (defined by the used) by adjusting the charge-pump currents. This is the most effective way of compensating for the variation of loop bandwidth with VCO tuning sensitivity. The user-defined frequencies are limited to the frequency range of the VCO, unless a pre-scalar or frequency divider is used in which case the output would be at chosen multiple frequency values of the VCO anywhere up to and beyond 20GHz.

The programmed information containing the frequencies of operation, phase detection frequency and other parameters are stored in an EPROM (memory chip) to enable immediate synthesis when the unit is powered-up. The whole units containing these devices have been tested to qualify for military as well as commercial applications. Assuming that a low phase noise VCO is used, a phase noise of -100dBc (at 100kHz offset) of the synthesiser is achievable.

References:

(1) W. Gosling, ed., "Radio Receivers", Peter Peregrins, London, 1986.

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(3) Hittite Microwave, "Compact PLLs Integrate VCOs", Microwaves and RF, Oct. 22, 2009

(4) Datasheet: http://www.linear.com/product/LTC6946

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(6) D. Banerjee, National Semiconductor Application Note 1879 "Fractional N Frequency Synthesis", Lit No. SNAA062, 10th December 2008.