New Qualified Industrial 0.5μm AlGaN/GaN HEMT Process : Status on GaN developement

D. Floriot[2], H. Blanck[2], D. Bouw, F. Bourgeois1, M. Camiade[2], L. Favède[2], M. Hosch[1], H. Jung[1], B. Lambert[2], A. Nguyen[2], K. Riepe[1], J. Splettstöße[1], H. Stieglauer[1], J. Thorpe[1], and U. Meiners[1]

[1] United Monolithic Semiconductors GmbH, Wilhelm-Runge-Str. 11, 89081 Ulm, Germany.
[2] United Monolithic Semiconductors SAS, 10 Avenue du Québec, 91140 Villebon-sur-Yvette, France.
http://www.ums-gaas.com

***Abstract* — This paper describes the performances of a new power 0.5 μm gate length AlGaN / GaN HEMT process named GH50_10. This process has been developed to address applications and market needs up to 7 GHz. A specific emphasis has been attached to find a trade- off in between power / efficiency and linearity . After an introduction of the context, a short description of the process manufacturing is given including spread of the DC parameters. From the qualification procedure, key reliability figures of the process are presented like the main energy of activation and an evaluation of the Median Time to Failure, evaluated respectively to 1.95ev and 10^6 hours at 200°C. Power performances are presented from L to C bands from 15W for the elementary power transistors to 50W for high power packaged transistors. This technology is presently available at industrial level to address products requirements for telecom and military needs. Finally, a status is presented concerning the development of a 0.25μm gate length process which is on the way to enter in qualification process.**

Keywords : AlGaN/GaN HEMT, power transistor, technology, reliability, robustness

I. Introduction

The RF technologies based on GaN wideband semiconductor have been now widely introduced by industrials since many years. In the domain of RF frequencies, most of these industrial processes [1] are in competition at the level of the foundry or packaged power transistors & MMIC. This paper describes all the elements & results of a new qualified process to address high power / high voltage needs up to 7 GHz. This development has benefited from many years of intensive researches in Europe involving the main prestigious and actives labs in this domain. Main objectives of these developments were dedicated to find the best compromise in between linearity behavior, power density and reliability figures, offering a competitive technology for end- users. This technology was developed to consider stringent requirement in term of reliability and robustness. The second point of this paper is dedicated to the process description giving element on the DC parameters and low- level RF characteristics. The third one details power characteristics of the transistors at 3 and 6 GHz followed in the next point by key results and figures of merit in term of reliability. Finally, some results are presented corresponding to design of High Power amplifiers in C band.

II. Technology description 0.5μm AlGaN/GaN process

The process has been qualified on a 3" inch substrate diameter. The AlGaN / GaN epitaxy, the overall process and the passivation have been optimized to find the better compromise in term of current density and thus power density. A 0.5μm gate length with a source field plate termination is used helping to reduce the Gate-Drain capacitance. The sequence of passivation has been optimized to reduce the leakage current measured at 50V below an criteria of -200 μA/mm. The average value is well below this limit and guarantees a high stability level of the Schottky associated to strong robustness at high temperature. A low value of the ohmic contact, close to 0.2-0.3 ohm.mm participates to get high RF performances. The cleaning step after opening of the first passivation layer, the thickness of the metallization and the topology by itself of the gate foot were carefully optimized as being part of the key to get a high reliable process. A pinch-off Vp (average value) of -2.2V is characteristic of the Schottky. The breakdown limit VBDs (defined @ Id=1 mA/mm) is above 200V.

The uniformity of the process is well supported by the spread of the maximum Gm (in mS) (figure 1)

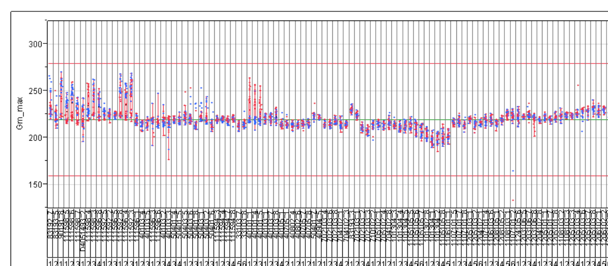

Fig. 1. Spread of Gm versus the reference of wafers in production.

Thin film metallic resistors and active ones based on the AlGaN sheet resistance are also used to stabilize the transistors. Power bars up to a maximum 36 mm of total gate development have been manufactured based on the combination of elementary transistors.

The wafer is thinned down to 100μm followed by a via hole process for source grounding and final back side metallization. The figure 2 summarizes the main DC characteristic parameters of the technology:

	min	typ	max
Vg_100 (1% of Idss) (V)	-2.5	-2.2	-1.9
Idss (mA/mm)		430	500
Ig leak (Vds=50V) (μA/mm)		50	200
Vds		50	55 (absolute max rating)

Fig. 2. Main DC characteristics of the process.

III. RF PERFORMANCES OF THE 0.5μM ALGAN/GAN PROCESS

A complete family of power transistors has been designed to develop a full scalable non- linear model. Two different topologies have been derived and applied to the design of a set of power bars; one is applied for very high power up to S band, the other one specifically to address needs in C band for which we put specific attention to the decreasing of the source inductance.

A gate to gate pitch of 50μm to 70μm is used in function of the thermal budget. Power transistors combining 4 to 10 fingers have been also designed with gate width ranging from 200 to 400μm.

A. RF performances

An example of characterization is shown in S-Band at 3.3 GHz for different drain quiescent current (5 to 50mA/mm) on a 3.2mm gate periphery transistor. These measurements are done on-wafer at ambient temperature for Vds=50V and transistors were matched at the input and output by external tuners (figure-3). Due to thermal constraint during on-wafer measurements, these measurements were performed in pulsed mode (10% duty cycle for a pulse length of 10μs)

In pulsed mode, power densities from 4.5 W/mm to 5.5W/mm (15 to 20 W) are measured, the PAE ranging in between 55 to 60%. During these characterizations, the 2nd & 3rd harmonics were put at 50 ohms. For longer pulse length, until 0.5 ms, no difference was noticed. Finally, by optimization of the load at 2.fo, the PAE could be improved by a minimum of 5 points for a large part of the Smith area.

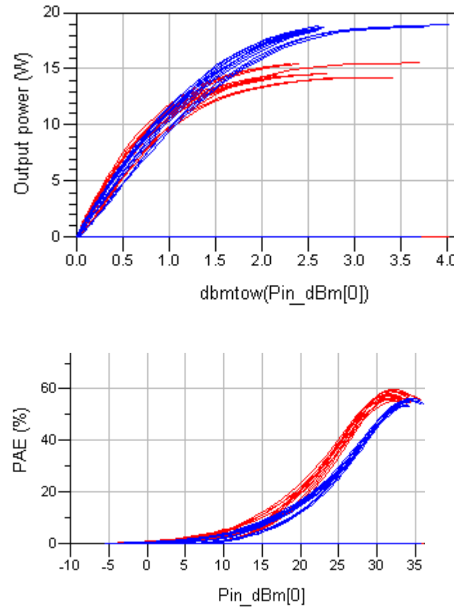

Fig. 3. Optimum in power (blue) and PAE (red) – on-wafer characterization of a 3.2mm transistor at 3.3 GHz.

B. Modeling – elementary power transistor

A full non- linear model has been developed to simulate the behavior of the transistor in large signal mode of operation. The current source has been fitted with a "modified" Tajima model. A comparison is carried out on a 2mm (8x250μm) transistor. First a complete I(V) and Sij pulsed measurements are completed in short pulses to limit the heating of the device. Different biasing points around Vds=50V and quiescent drain current are used. The non- linear capacitance laws Cgs and Cgd are fitted along the most probable load line of the transistor. Second, a temperature dependant model is activated based on the same measurements performed at different case temperatures (figure 4).

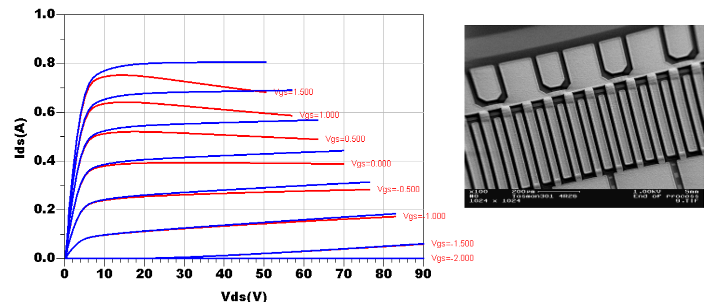

Fig. 4. I(V) curves with (red) and without (blue) the activated contribution of the thermal network and dependencies. At right, layout of the 2mm transistor.

A comparison in between the non linear model and the measurement is applied in C band at 6 GHz on a load-pull

result giving the optimum efficiency. Both, measurement & simulated contours are plotted in the same Smith diagram (figure 5).

This library of models should be used in the following recommended operating field:

- Bias point in the range : Vds, 30 up to 50V-Ids, 10 up to 100mA/mm
- Small signal frequency range: up to X band
- Large signal frequency range: up to C band
- Maximum compression level in large signal: 5dB

Thermal dependency: a thermal circuit is implemented in the model associated to temperature dependency of the non- linear I(V) equations.

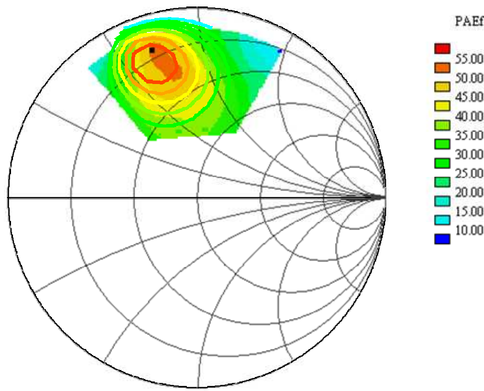

Fig. 5. Comparison measurement / simulation on a 2mm device at 6 GHz of the load-pull contour – Vds=50V – Idsq=150mA.

IV. Reliability & qualification : 0.5µm AlGaN/GaN process

In order to assess the reliability of the process, a complete qualification plan was defined. This one includes different class of tests to evaluate separately the effect of environment, the wear- out mechanism and an evaluation of the Mean Time To failure. Many papers have stressed the fundamental role of the inverse piezoelectronic root cause [2-3] to explain failures in AlGaN/GaN HEMT. To limit or delay this effect, the optimization of the surface treatment during the different steps of the process (passivation, opening gate cleaning …) and an appropriate epitaxy scheme is necessary. A trade off in between the GaN cap, the AlGaN thickness associated to the Al content is one the key aspect. As a consequence, it has a direct influence on the capabilities of the technology in term of power density (W/mm) as the Al content influence directly the maximum current density in the channel.

The qualification plan is based on :

- Thermal Humidity Biased (THB) test : 85%-85°C
- VRT : --65°C to +125°C – 1000 cycles
- Storage test : 250 & 300 °C – 1000 hours
- High Temperature Reverse Biased test (HTRB) : Vgs=-7V / Vds=100 & 120V / Tj=175°C, > 2000 hours. This test is used to evaluate the Schottky stability
- High Temperature Operating Life test (HTOL) performed at different temperature. Used to extract the wear out mechanism (MTF). The tests are performed at various temperature from 265 to 335°C at Vds=50V. 70% failures were targeted during this experiment.
- IdQ life test to evaluate the Mean Time To failure of the process and the associated number of Fits (Failure In Time). This test is performed on a 40W packaged power transistor.
- DC & RF step stress to evaluate the Safe Operating Area (SOA) with tests performed at increasing VSWR.
- The figure 6 gives the graph of the Median Time to Failure (MTF) in an arhenius plot. A energy of activation of 1.95 ev is found which is comparable to the values already published on industrial process [4]. At 200°C, a MTF of 10^6 hours is extrapolated.

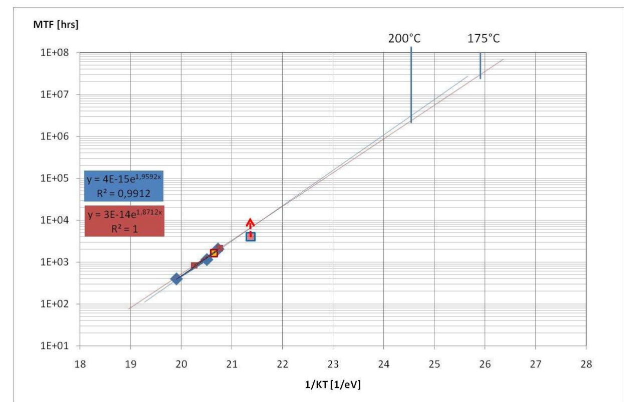

Fig. 6. MTF versus 1/kT – Vds=50V - 10^6 hours @ 200°C

V. Product development

Aside from technology development, a complete set of product are under development and qualification addressing needs from L to C Bands. An example of 50W – C band fully internally matched transistor is shown in the figure 7 followed by an example of characterization.

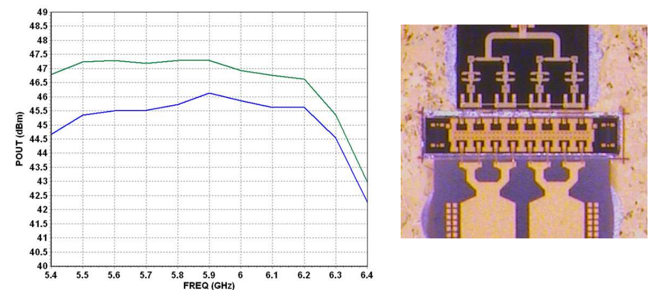

Fig. 5. Output power vs frequency at Pin = 36 (blue) and 40 dBm (green) – CW mode of operation - Vds=50V – Tc=25°C.

VI. STATUS OF DEVELOPMENT ON THE 0.25μM ALGAN/GAN PROCESS

The process development of the 0.25μm gate length process is derived from the preceding one with slight modification. The epitaxy has been reviewed offering an improved power density around 4W/mm in X band. A modification of the parameters governing the deposit of the different passivation layers has also been optimized again to reduce the leakage current density and the reproducibility from lot to lot.

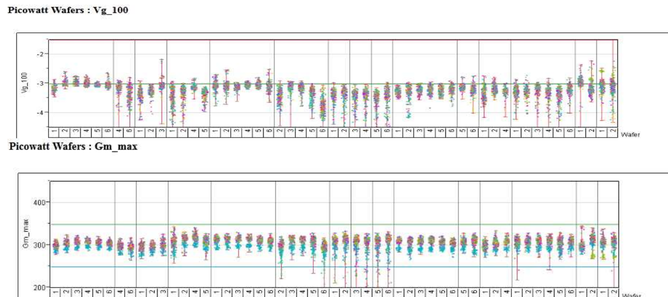

Fig. 6. Spread measured on 50 wafers : Pinch-off voltage (Vg_100) and transcoductance (Gm).

Active devices (transistors & diodes) and passive elements have been fully characterized to cover all requirements of a complete design kit. It includes support for hot and cold FET, low noise and diode models (switching, limiter). Each kind of models exhibits some scaling capability and temperature dependencies. The exact limitations (DC & RF) would be definitively defined after the completion of the qualification phase. It includes the set of parameters for the recommended and maximum ratings.

An example of RF performances are given in figure 7.

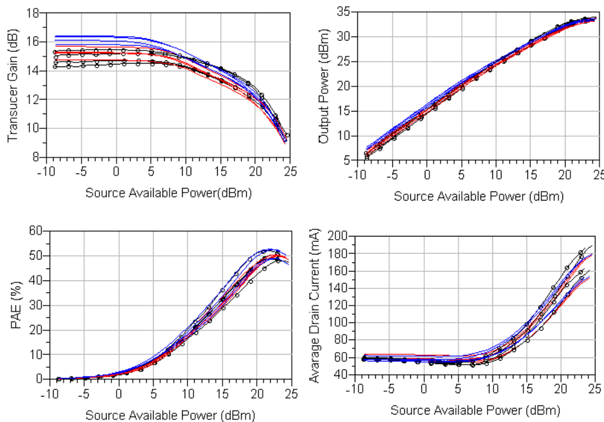

Fig. 7. RF parameters (Gain – Power – PAE – drain current) measured at 10 GHz – CW – Vds=25V – IdQ= 100mA/mm -

This process referenced as GH25_10 would be compliant of application ranging up to 20 GHz. This process have been continuously evaluated through multiple designs and foundries (medium & wideband MPA & HPA, LNA, power switch) with always excellent results.

VII. CONCLUSIONS

In this paper, we present in first hand the core results of a 0.5μm GaN HEMT process fully qualified through intensive tests. Excellent reproducibility has been obtained on more than 100 wafers. To support foundry activities and the design of a product line of power GaN transistors, a complete design kit have been put in place. Demonstrations in S-Band (40 & 80W) & C-Band (50W) giving high PAE have supported this qualification. In second hand we synthesized some elements concerning the stabilization phase of the 0.25μm gate length process. This work has been mainly supported by French (DGA) & German (BWB) Ministries of Defense through the contract, by NXP though specific support contract.

REFERENCES

[1] "Reliability Of GaN/AlGaN HEMT MMIC TECHNOLOGY ON 100 mm 4H-SiC" , Donald A. Gajewski, & al, 2010, MTT-S

[2] " Gate Current Degradation Mechanisms of GaN High Electron Mobility Transistors", J. Joh & al, IEDM 2010

[3] "GaN on SiCDegradation Modes and Reliability Evaluation", Tutorial Jimenez, ESREF 2011,

[4] "A Manufacturable, High Power RF Gallium Nitride (GaN) Technology Portfolio With 65V Operation And Enhanced Linearity", J.B. Shealy & al, COMCAS 2011