A COMPACT, AGILE, LOW-PHASE-NOISE FREQUENCY SOURCE WITH AM, FM AND PULSE MODULATION CAPABILITIES

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ABSTRACT

This paper presents a broadband frequency source featuring high technical characteristics and extended functionality. The source is a compact (5 by 7 by 1 inches) module that covers the 0.1-to-10 GHz frequency range with a 0.001 Hz step size. The module is based on a novel (patent pending) PLL design that combines fast switching speed, low phase noise, and low spurious characteristics. The measured phase noise at an output frequency of 10 GHz and 10 kHz offset is –122 dBc/Hz. For an output frequency of 0.1 GHz and 10 kHz offset the phase noise drops down to –150 dBc/Hz. The switching time is about 20 uSec to be within ±1 MHz from the final frequency and less than 100 uSec to be within ±50 kHz respectively. Spurs do not exceed the –70 dBc level. The output power is leveled between –25 and +15 dBm. The module can be controlled through either SPI or USB interface and also includes AM, FM and pulse modulation capabilities. The developed module can be used as a broadband, agile signal source in a variety of test-and-measurement, communication, and monitoring systems.

INTRODUCTION

The frequency synthesizer is a key element of virtually any RF/microwave system. It generates a stimulus signal or is used as a local oscillator in a variety of up- and down-conversion schemes. The industry feels persistent pressure to deliver higher-performance, higher-functionality, smaller-size, and lower-cost synthesizer designs.

Aside from frequency coverage and resolution, phase noise and spurious content are critical parameters that impose the ultimate limit in the system's ability to resolve signals of small amplitude [1]. Another key parameter of the synthesizer that impacts overall system performance is the frequency switching speed [2], [3]. The time spent by the synthesizer transitioning between frequencies becomes increasingly valuable since it cannot be used for data processing. While many systems still work adequately with millisecond switching speeds, newer requirements demand microsecond operation together with comparable spectral purity of the lower-speed designs.

Another challenge is to increase the synthesizer functionality by implementing various functions such as output power control, output power mute, frequency and power sweep, and list mode. Many applications also require various modulation options such as amplitude, frequency, and pulse modulation. Inside a synthesizer, there are always many devices that can carry these functions and be reused to increase the functionality without a significant cost penalty.

DESIGN

Direct analog, direct digital, and indirect approaches are used for modern synthesizers. Each has tradeoffs. For example, direct-analog synthesizers can provide the best performance in terms of speed, but they are complex and expensive. Direct-digital synthesis (DDS) is fast and less expensive, although it still needs to improve in terms of frequency coverage and spurious performance. Thus, the most popular synthesizer designs utilize indirect (or phase locked) solutions based on either YIG or VCO devices.

Historically, high-performance PLL synthesizers have relied on YIG-tuned oscillators featuring broadband operation and excellent phase noise characteristics. However, the high power consumption, big size, and especially low tuning speed, inherent to YIG oscillators, have contributed to a shift to solid-state VCO architectures. VCO-based synthesizers are significantly faster; however, their phase noise has traditionally been considered to be inferior when compared to YIG-based designs.

We present an innovative VCO-based synthesizer design that provides a unique combination of fast-switching speed and very low phase noise characteristics. The phase noise within the loop filter bandwidth depends on the reference as well as residual noise characteristics of individual PLL components (such as phase detector, reference and feedback divider, loop filter, etc.) and is further degraded by large division ratios required to provide a high-frequency output with a fine resolution. In contrast to traditional approaches (which tend to minimize the PLL loop division ratio), the proposed design takes a more radical step by eliminating the divider from the PLL feedback path. Moreover, it inverts the PLL division ratio by applying a multiplication within the PLL as depicted in Fig. 1. This drastically improves both phase noise and spurious characteristics.

Furthermore, the PLL bandwidth is significantly extended in comparison to conventional PLL designs in order to suppress the VCO noise within the loop bandwidth. This results in very small frequency acquisition time and consequently fast switching speed. Additionally, the wide PLL bandwidth suppresses undesired microphonic effects.

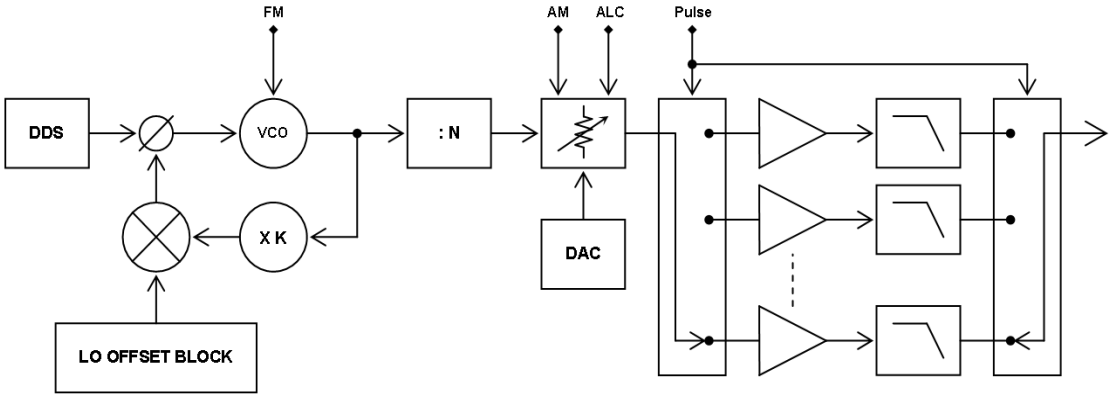

Fig. 1: Simplified block diagram

A simplified block diagram of a frequency synthesizer developed with this concept is shown in Fig. 1. The main PLL includes a fundamental VCO covering the 5-to-10 GHz frequency range. The VCO is locked to a low-noise reference with the help of a frequency offset block generating course frequency steps. A desired frequency resolution of 0.001 Hz is provided with a DDS module that fills in the gaps between the LO offset steps. The DDS spurs are suppressed with a combination of software and hardware (upconversion followed by division) techniques as shown simplistically in Fig. 2 and discussed in more detail in [4]. The PLL circuit also includes a separate input for a signal that accesses the VCO tuning port directly and is used for frequency modulation.

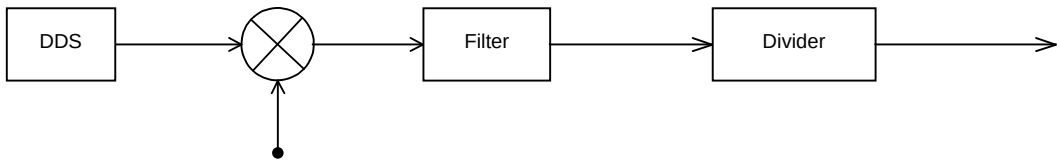

Fig. 2: DDS spur suppression

The frequency coverage below 5 GHz is accomplished with a programmable frequency divider. The signal between 100 MHz and 10 GHz is amplified and filtered with a switched amplifier-filter bank that results in reduced harmonics. In addition to the harmonic filtering, the switches are also used for pulse modulation. The signal level in front of the amplifiers is controlled with a variable gain attenuator. The attenuator is driven by a DAC that carries output power calibration functions as well. The attenuator can be also accessed directly to provide a closed-loop ALC capability. By adding an external coupler and RF detector, the signal from the detector can be fed back to the attenuator control input in order to close the loop. This configuration ensures precise, instrument-grade output power characteristics regardless of the output match. The attenuator is also used to provide amplitude modulation. Thus, the design provides all major modulation functions including AM, FM, and pulse modulation.

The synthesizer includes a highly stable internal OCXO that sets the desired phase noise performance and also provides a 10-MHz reference signal to the outside world. The internal oscillator automatically locks to an externally applied reference when it is present.

The synthesizer is built on a printed circuit board that is placed into a compact metal enclosure measuring 7 by 5 by 1 inches in dimensions. The module can be controlled through SPI and USB interfaces, which are realized with a built-in processor. The processor supports all necessary frequency tuning algorithm calculations as well as a number of features such as output power calibration and control, independent frequency and power sweep, and list mode. The module is biased from a single +12V DC supply and includes custom-built active filters to prevent signal contamination. The overall power consumption does not exceed 20 Watts.

TEST DATA

The synthesizer is tuned between 0.1 and 10 GHz with a 0.001 Hz step. The maximum unleveled power is close to +20 dBm and can be calibrated between –25 and +15 dBm levels

across the entire operating range. The power variations do not exceed ±1 dB as depicted in Fig. 3.

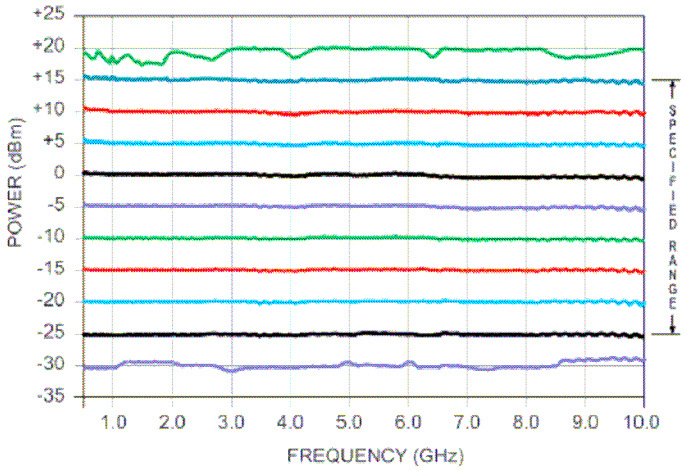

Fig 3: Output power response at various power settings

The frequency switching speed of the main PLL loop is less than 20 uSec to be within ±1 MHz from the final frequency as shown in Fig. 4. However, the LO offset block as well as the synthesizer control add extra delays required to receive a tuning command, perform all necessary calculations, and program individual devices. The overall throughput time is in order of a few tens of microseconds and is specified at 100 microseconds for a ±50 kHz frequency accuracy.

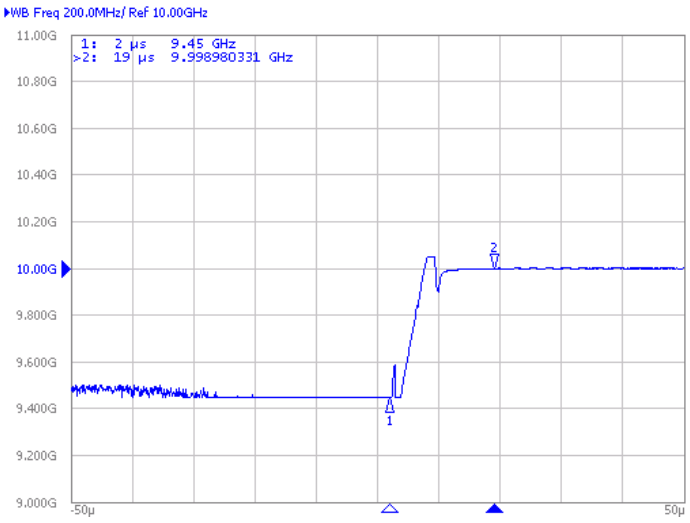

Fig. 4: Switching speed measurement

The phase noise plots taken at 10 GHz and 100 MHz outputs are shown in Fig. 5 and 6 respectively. The phase noise at 10 kHz offset is about -122 dBc/Hz with a 10 GHz output signal.

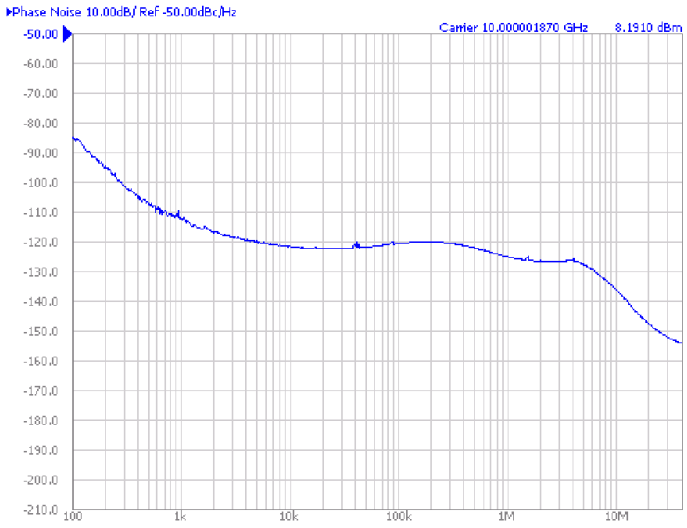

Fig. 5: Phase noise at 10 GHz

The noise drops down to about -150 dBc/Hz at 100 MHz (limited by the divider and test setup noise floor). The phase noise profile also reveals that the loop bandwidth is close to 5 MHz which results in fast tuning speed as mentioned above. Spurious levels do not exceed –70 dBc at the highest operating frequency as shown in Fig. 7.

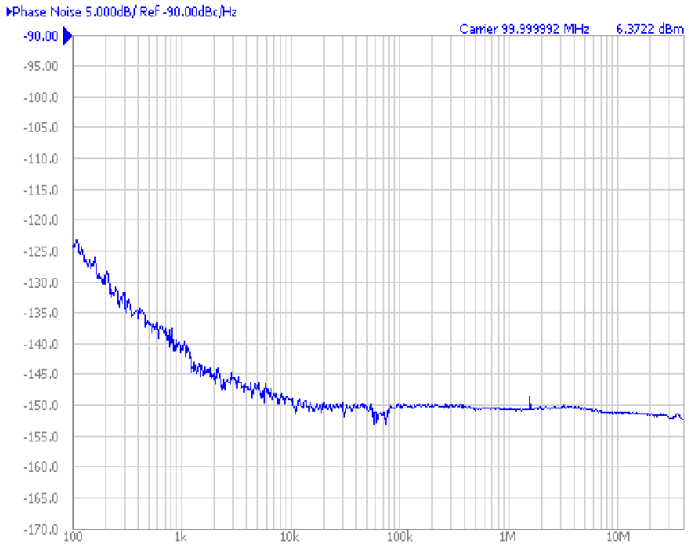

Fig. 6 Phase noise at 100 MHz

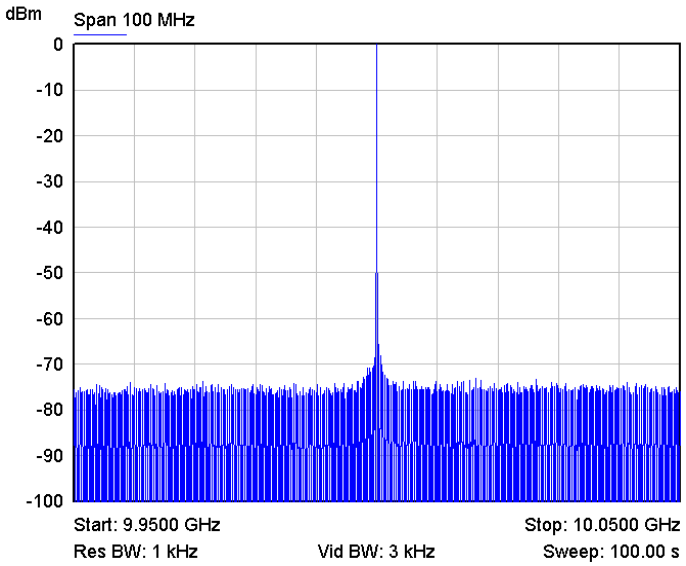

Fig. 7: Output spectrum at 10 GHz

The synthesizer has a pulse modulation input accepting 3.3V CMOS modulating signal between DC and 5 MHz. The measured on/off ratio at 10 GHz RF output exeeds 80 dB level as indicated in Fig. 8. The rise and fall time at the same RF output frequency are less than 20 nSec as shown in Fig. 9.

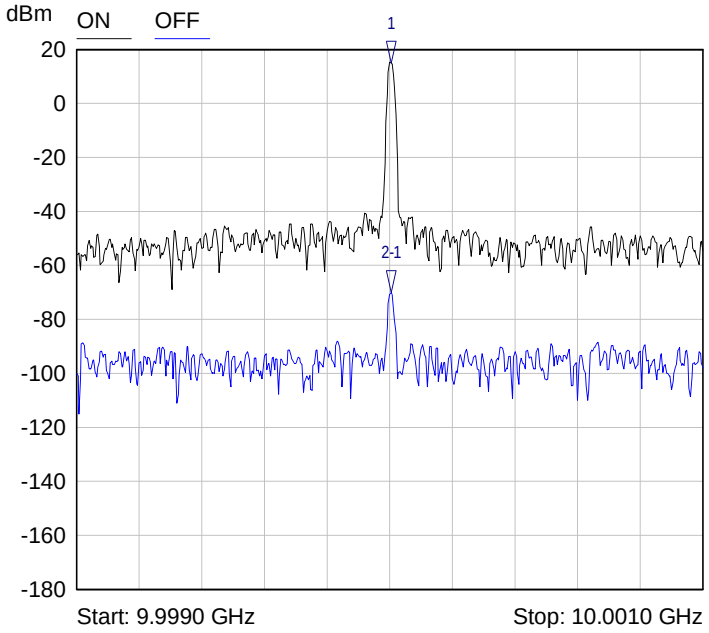

Fig. 8: Pulse modulation on/off ratio at 10 GHz

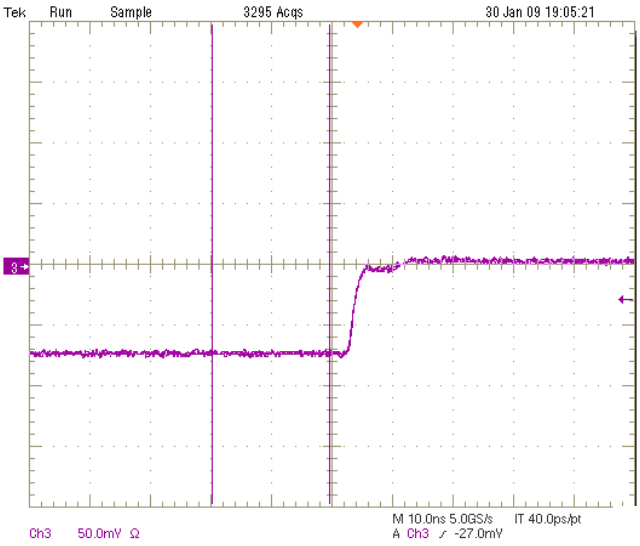

Fig. 9: Pulse modulation rise/fall time measurements

The synthesizer accepts a ±1V AM modulating signal between DC and 100 kHz delivering more than ±20 dB modulation range centered at -5 dBm RF output. It also provides up to 100 MHz frequency deviation at a 10 GHz RF output and ±1V modulating signal that can vary between 50 kHz and 1 MHz.

CONCLUSIONS

A compact VCO-based frequency synthesizer has been developed. The synthesizer covers the 0.1-to-10 GHz frequency range with a 0.001 Hz step size and 100 usec tuning speed that allows realizing digital sweep functions without sacrificing sweeping time. The spurious level does not exceed -70 dBc and phase noise at 10 GHz is measured to be better than –120 dBc/Hz at 10 kHz offset. This corresponds to or even exceeds the phase noise performance of traditional YIG-based designs. Furthermore, the synthesizer provides output power control as well as all major modulation functions including AM, FM, and pulse modulation.

These technical characteristics together with compact size will benefit various applications where a broadband operation, high spectral purity, and fast switching speed are simultaneously required. Possible applications include test-and-measurement, telecommunications, and monitoring systems.

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