Design of Ultra Broadband Highly Efficient GaN Power Amplifiers Using Voronoi Diagrams

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ABSTRACT

This paper presents the design, implementation and experimental results of a broadband high-efficiency GaN-HEMT power amplifier. The proposed method defines the optimal impedance regions of a PA at several frequency steps across the operational band. Those regions contain the impedance that maintains high output power and high power added efficiency (PAE) levels simultaneously. The source-pull and load-pull simulations are employed to determine the optimal input and output impedance of a GaN transistor across 0.3-2.3 GHz regarding PAE and output power level. The matching network is then synthesized with those optimal impedance regions using a Voronoi diagram. A low-pass matching network is applied to implement the optimal impedance over the band. The measurement results indicate a power of gain better than 10 dB and a typical output power of 43 dBm. The measured PAE is 58%-69% across a 7.6:1 bandwidth.

I. INTRODUCTION

Power amplifiers (PAs) are essential devices of many communication and radar systems. The features of a PA regarding the bandwidth, power gain, linearity, output power and power added efficiency (PAE) could significantly affect the overall performance of a system. Particularly, a high-power, high-efficiency broadband PA is in high demanded by the industry and market. Consequently, more and more research effort has been made in this area.

This paper introduces a simple and efficient method for the design of a broadband high-efficiency PA. This approach defines the frequency dependent optimal impedance regions which maintain high output power and PAE levels over the operational band. Then, a direct computation method based on a Voronoi Diagram is introduced to synthesize the matching networks. The detailed design method is presented and explained in this paper, including how to define the optimal impedance regions and how to match the impedance with a low-pass LC-ladder network. A 25-W Cree GaN HEMT CGH40025F is used as the active device in this work, whose package parasitic is carefully analyzed. The source-pull/load-pull simulations are performed to obtain the frequency dependent optimal impedance regions for the PA. A PA operating over 0.3-2.3 GHz with 58%-69% PAE at a typical output power of 43 dBm is designed. The PA has been fabricated and measured to validate the method.

II. DESIGN OF POWER AMPLIFIER

The impedances presented to the source and load of a transistor could significantly affect the performance of a PA regarding output power and PAE. Therefore, the matching network (MN) should present a proper impedance to the transistor to achieve desired performance. Designs reported in [1],[2],[3] use a filter-prototype MN to match the fixed optimal impedance at the center frequency for the PA over a wide bandwidth. This technique achieves the optimal performance at the center frequency and compromises the performance at other frequencies over the band at a reasonable level. However, this approach is not suitable for designs where the optimal impedances at different frequencies are not close to each other, which is almost always the case in multi-octave PA designs. A load-pull simulation was carried out to find the optimal impedances for a CGH40025F transistor from Cree to achieve high PAE. The PAE contours are shown in Fig.1. The contours vary with the frequency and are not very close to each other.

A. Define the Optimal Impedance Regions

At different frequencies, the optimal impedances for high efficiency and high output power are not close to each other. The high output power and high PAE contours of the transistor at 1 GHz are shown in Fig.2. To maintain high output power and high efficiency of a PA across a wide band simultaneously, the optimal impedance should not be a fixed value at each frequency step. Several frequency-dependent optimal impedance regions across the operational band should be defined, which contain the impedance that allows the PA to have a performance better than the lowest acceptable PAE and output power as shown in Fig.2.

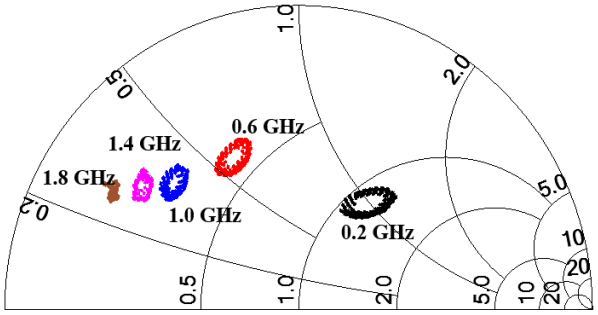

Fig.1. Simulated PAE contours of a CHG40025F at different frequencies.

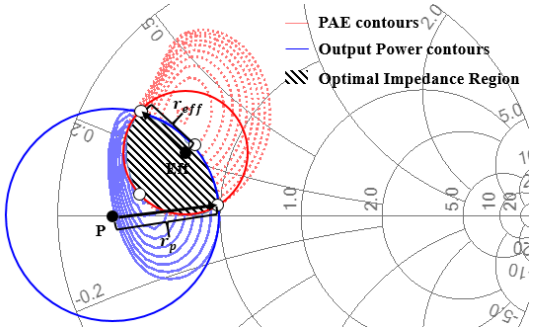

Fig. 2. Optimal impedance region at 1 GHz.

The proposed method of defining the optimal impedance regions can be described as follows: 1) Divide the entire operation bandwidth into *k* frequency steps. The number of frequency steps is chosen depending on the required bandwidth and the variation of the optimal impedance at different frequencies. 2) For each frequency step, the output power and PAE contours can be obtained via source-pull/load-pull simulations. The boundary of the contours defines the lowest output power and PAE acceptable for the design. 3) The overlap region of output power and PAE contours is selected as the optimal impedance region at the corresponding frequency step. If the contours do not overlap, a sacrifice is necessary to extend the contours until they have an overlap (if the output power is the priority concern, the lowest acceptable PAE level should be reduced and vice versa). 4) For mathematical convenience, the overlap region of output power and PAE contours can be approximated by the interception of two circles as shown in Fig.2. Any three non-collinear points define the circumference of one circle, and one circle only. The impedance of the region can be expressed as a function of frequency as:

$$\begin{cases} d_P(\omega_k) \le r_P(\omega_k) \\ d_{Eff}(\omega_k) \le r_{Eff}(\omega_k) \end{cases} \tag{1}$$

where $\omega_k=2\pi f_k$, k is the frequency step, d_P and d_{Eff} are the Euclidean distance from the impedance point to the center of the PAE and output power circles, r_P and r_{Eff} are the radius of the PAE and output power circles respectively.

Therefore, two intercept points of the PAE and output power contours boundaries and another point on the PAE contour boundary inside the output power contour will define the PAE circle. The circle of output power contours can be found likewise. Then the overlap region of the PAE and output power circle is the optimal impedance region at the corresponding frequency.

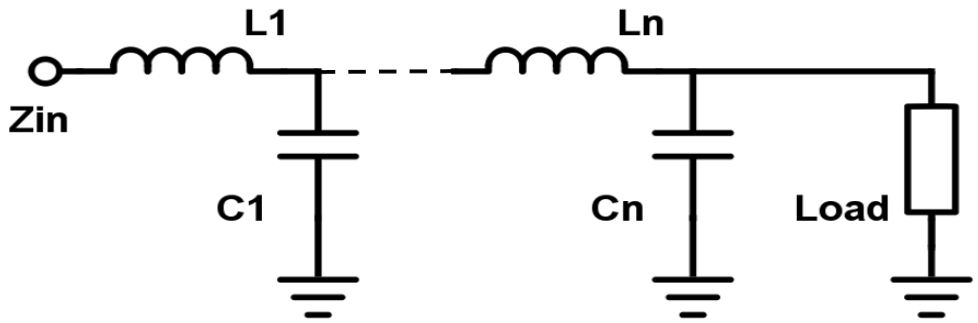

Fig. 3. The lumped low-pass matching network.

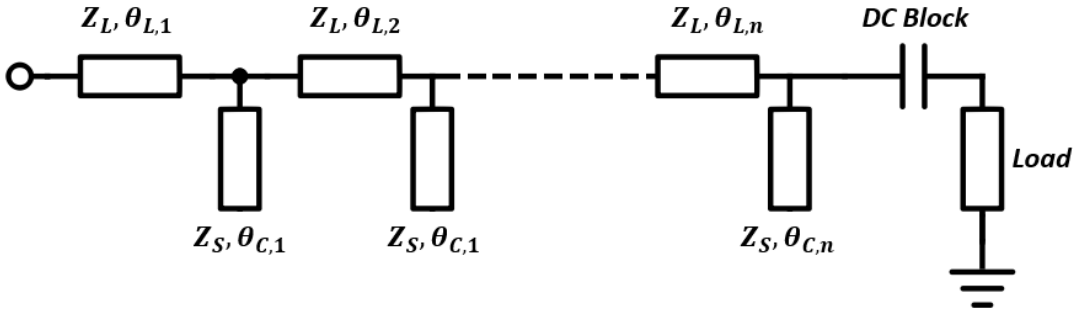

Fig.4. The distributed low-pass matching network with DC block.

B. Design of Matching Networks

Once the optimal impedance regions are defined, the task resides in realizing the desired impedances at different frequencies using a proper matching circuit topology. A low-pass LC-ladder network in Fig.3 is chosen to implement the MN due to its in-band and out-of-band behavior as analyzed in [4]. The input impedance of the MN can be described as a function of frequency and element values. The MN can be treated as a cascaded structure of several LC sections. The ABCD matrix of the MN can be expressed as:

$$\begin{bmatrix} A(\omega_k) & B(\omega_k) \\ C(\omega_k) & D(\omega_k) \end{bmatrix}_{LC} = \prod_{i=1}^{n} \begin{bmatrix} 1-\omega_k{}^2 L_i C_i & j\omega_k L_i \\ j\omega_k C_i & 1 \end{bmatrix} \tag{2}$$

where $\omega_k = 2\pi f_k$, k is the number of the frequency steps and n is the number of LC-ladder sections used in the network. Therefore, the input impedance Z_{in} of the matching network can be described as a function of the ABCD matrix in:

$$Z_{in}(\omega_k) = \frac{Z_{load} * A(\omega_k) + B(\omega_k)}{Z_{load} * C(\omega_k) + D(\omega_k)} \tag{3}$$

where *A*, *B*, *C* and *D* are the values obtained in (2) and Z_{load} is the load resistance of the MN, typically 50 Ohms. With the expression in (3), the input impedance at each frequency steps of the MN can be obtained once the LC values are determined. If the corresponding Z_{in} of the MN at each frequency step is inside the corresponding optimal impedance regions, the MN will provide optimal performance for the device. Considering the availability of high-quality inductors and capacitors to implement the design, the LC components are realized by transmission lines while the DC block capacitor is kept lumped as shown in Fig.4.

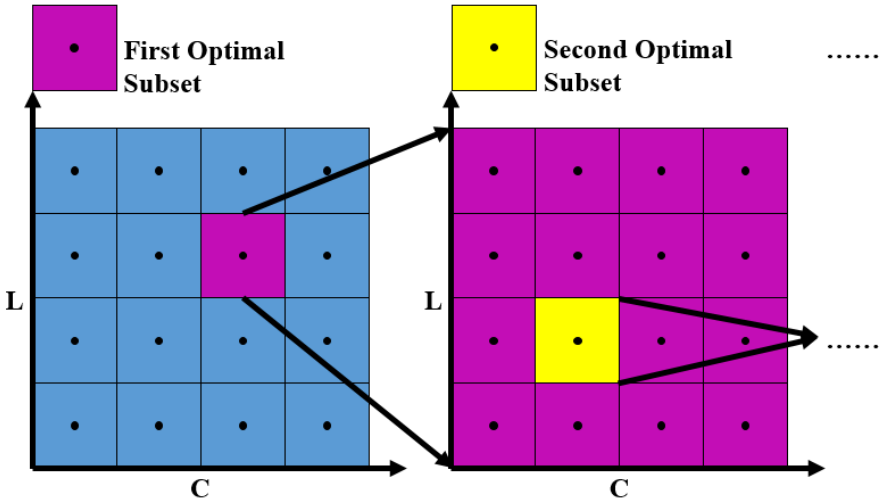

Fig. 5. .Illustration of the Voronoi diagram and the optimal subset.

The inductors can be implemented by high-impedance transmission lines while the capacitors can be realized by low-impedance open stubs. The ABCD matrix of the MN can be described as [5]:

$$\begin{bmatrix} A(\omega_k) & B(\omega_k) \\ C(\omega_k) & D(\omega_k) \end{bmatrix}_{LC} = \left(\prod_{i=1}^{n} \begin{bmatrix} \cos(\frac{\omega_k}{2\pi}\theta_{L,i}) & jZ_L \sin(\frac{\omega_k}{2\pi}\theta_{L,i}) \\ j\frac{\sin(\frac{\omega_k}{2\pi}\theta_{L,i})}{Z_L} & \cos(\frac{\omega_k}{2\pi}\theta_{L,i}) \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ j\frac{\tan(\frac{\omega_k}{2\pi}\theta_{C,i})}{Z_C} & 1 \end{bmatrix} \right) \cdot \begin{bmatrix} 1 & \frac{1}{j\omega_k C_{DC}} \\ 0 & 1 \end{bmatrix} \quad (4)$$

where $\omega_k = 2\pi f_k$, Z_L and Z_C are the characteristic impedances of the series lines and the shunt stubs respectively, θ is the electrical length of the transmission lines. The input impedance of the MN at each frequency can be calculated. If the corresponding Z_{in} of the MN at each frequency step is inside the optimal impedance regions as defined, the MN will provide optimal performance for the device.

The problem now is to find the proper electrical length for series lines and shunt stubs of the MN. The Voronoi diagram, a method that divides a plane into parts based on the distance to points in a specific subset of the plane, can be applied [6],[7]. Let $\theta_L = \{\theta_{L,1}, \theta_{L,2}, \dots, \theta_{L,n}\}$ and $\theta_C = \{\theta_{C,1}, \theta_{C,2}, \dots, \theta_{C,n}\}$, where n is the number of the LC sections used in the MN. The dimension of the variable can be equivalently visualized using the two-dimensional L-C plane, where the L and C represent the electrical length for inductor and capacitor respectively. The elements in variable θ_L and θ_C can be defined as $\theta_{L,n} = \{\theta_{L,n}{}^{(1)}, \dots, \theta_{L,n}{}^{(m)}\}$,$\theta_{C,n} = \{\theta_{C,n}{}^{(1)}, \dots, \theta_{C,n}{}^{(m)}\}$, where m is the number of samples in the subset. Due to the possible electrical length is from 0 degree to 180 degree, we divide all the possible values of electrical length into m samples as shown in the Fig.5 (the value of the black dot represents the square). With the sampled LC electrical length values obtained in the Voronoi diagram, use equations (2), (3) and (4) to calculate the corresponding input impedance $Z_{in}(\omega_k)$ of each subset. The shortest Ecudiclne distance from the input impedance to the output power and PAE contour $d_P^{(m)}(\omega_k)$ and $d_{Eff}^{(m)}(\omega_k)$ can be calculated. If $d_P^{(m)}(\omega_k)/r_P(\omega_k) \le 1$ and $d_{Eff}^{(m)}(\omega_k)/r_{Eff}(\omega_k) \le 1$, it indicates that the input impedance of the m^{th} subset is in the optimal impedance regions over the desired band. This subset will be used to synthesize the MN. If no subset can meet the requirements, the shortest Ecudiclne distance from the input impedance to the optimal impedance region should be calculated. The matching quality of the subset can be evaluated by:

$$\Lambda^{(m)} = \sum_{i=1}^{k} \left| d_{in}^{(m)}(\omega_i) \right|^2 \quad (5)$$

where the $d_{in}^{(m)}(\omega_i)$ is the shortest Euclidean distance from the input impedance of the m^{th} subset at i^{th} frequency step to the corresponding optimal impedance region. The m^{th} subset that has the minimum $\Lambda^{(m)}$ will be selected as the optimal subset for further optimization. Repeat the Voronoi partition for the optimal subset until the requirements are satisfied as illustrated in Fig.5. If the requirement cannot be satisfied after repeating the partition, it indicates that the obligation cannot be met with the current

order of the MN. Herein, it will be necessary to increase the order of the MN or decrease the lowest limits of the output power and PAE and define the new optimal impedance regions.

The solution of the LC values obtained using this method may not be the best one because the calculation cannot include every single possible combination of LC values. However, a solution that could ensure the input impedance at each frequency step is inside the corresponding optimal impedance region is sufficient to realize a PA with the desired performance. An infinitely small separation of the LC value and infinite order of the MN will offer a very accurate result, whereas the implementation will be very computationally intensive. Consequently, the trade-off between accuracy and computation cost should be considered when determining the size of the separation and the number of iterations.

III. FABRICATION AND MEASUREMENTS RESULTS

The designed broadband PA and the measurement setup are shown in Fig.6. A 25-W Cree GaN-HEMT (CGH40025F) was chosen to realize the design. The transistor was sealed in the Cree 440166 package. The high breakdown voltage will ensure the safe operation of the transistor. The PA was implemented on a 1.52 mm thick Rogers 4350B substrate with $\varepsilon_r = 3.48$ and 1 oz/sqft copper. A heat sink was attached underneath the PA to reduce the heating effect.

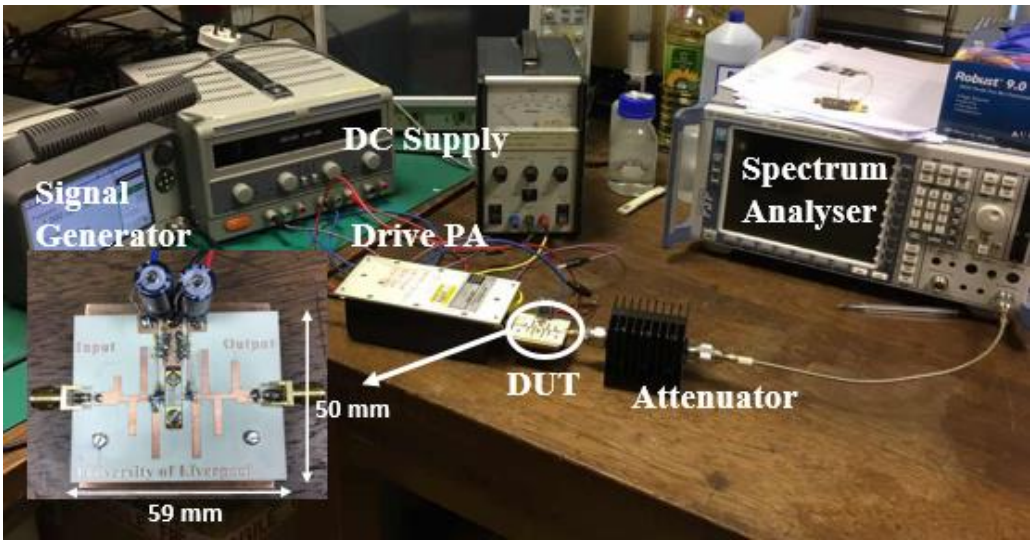

Fig.6. A photo of the fabricated PA and the measurement setup.

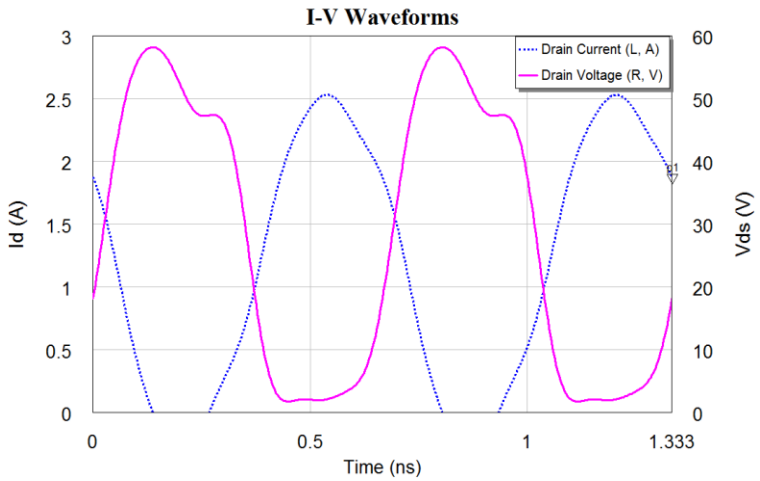

Fig.7. Simulated drain voltage and current waveform at 1.5 GHz.

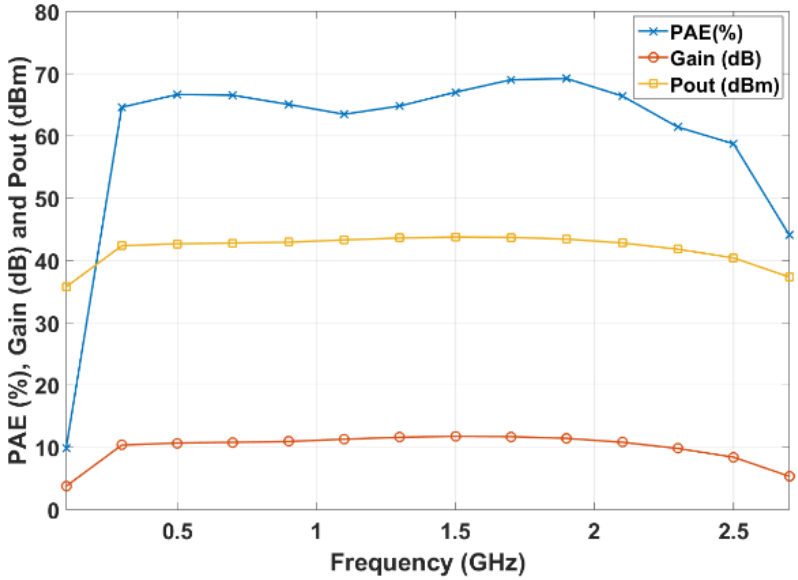

Fig. 8. Measured Gain, output power and PAE versus frequency at fixed 30 dBm input power.

The simulated voltage and current waveforms on the drain at 1.5 GHz are shown in Fig.7. The overlap between the voltage and current is relatively small which indicates that the PA can achieve a very high efficiency. The fabricated broadband PA was characterized by large signals to investigate its performance. The PA is tested with a single-tone CW input signal from 0.3-2.3 GHz generated by a KEITHLEY 2920 RF Signal Generator. The gate of the transistor was biased at -3V, and the drain voltage was 28 V. The measured PAE, gain and output power across the operational band are shown in the Fig.8. The broadband PA has a PAE higher than 59% over the desired bandwidth. The PAE is slightly lower at the high-frequency end. The gain is better than 10 dB, and the corresponding output power varies from 40 dBm to 43.5 dBm. The broadband high-efficiency performance of this PA validated the proposed design method.

IV. CONCLUSION

This paper has presented a general method of designing wideband high-efficiency PAs. The optimal source and load impedances for a transistor have been defined by optimal impedance regions instead of fixed values based on source-pull/load-pull simulations. A low-pass LC-ladder network has been applied to match the predefined optimal impedance regions. A method of synthesizing the MN has been presented based on using the Voronoi diagram. The designed PA has been fabricated and measured. The large signal experimental results have shown a PAE of 59-69%, a gain better than 10 dB and a typical output power of 20 W over a wide bandwidth from 0.3 GHz to 2.3 GHz. The state-of-the-art performance is better than any other reported works. The results have indicated the potential of the proposed method for future communication systems where high-efficiency and wideband amplifiers are needed.

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