Signal Integrity by Design

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Abstract

Today's electronic system designers are faced with the twin challenge of modern products supporting greater functionality together with increasing clock speeds. For complex integrations of radio standards we need to look no further than the advanced mobile phones. These mass produced devices can now come equipped with many radios; Edge/GSM, UMTS, Bluetooth, GPS, FM and Wireless LAN. PDA, Infrared link, and MP3 capabilities add to this mix. Perhaps the name mobile phone is becoming a misnomer! Supporting this rich combination of personal communication technology is the infrastructure or system backbone carrying packet and streaming data. The nodes of these systems are realized using printed circuit board technology. The trend towards higher speeds is not only confined to communications technology (voice and digital data), for example computers now employ high speed serial data transfer standards such as S-ATA, PCI Express etc. The push for higher data rates on cheap low grade materials has meant that the design methodology for PCBs now needs to account for the propagation properties of tracks on FR4 laminates in a more sophisticated manner. This paper will focus on the design issues associated with such high speed analogue designs.

Introduction – The SI problem

It is now well understood that in many electronic sectors there is an increase in the number and data-rate of high-speed I/Os used in electronic systems. Companies developing products with increasing frequencies and edge rates need to account for the physical propagation of high speed signals. High speed analogue chips are required to drive signals through their immediate environment (bond wires, BGA connections, CSP), through the packaging interconnect, and onto the board, then across the board along to the receiver circuits. Some designers may only be interested in the transport of signals across the board; others may be designing chips with pulse pre-emphasis and need better insight into both package performance and PCB propagation.

In the past, the task of PCB design has been carried out by draughtsmen working primarily in the 2D mechanical domain. Their aim has been to interpret the schematic diagram, package the circuit components and to ensure a robust solution with the minimal manufacturing issues. Put simply; make sure that the components fit within the board outline, ensuring that thermal requirements, mechanical stress and automated manufacturing rules are met in parallel with the trace connectivity reflecting the netlist. Current density limitations and impedance requirements have also been communicated to the layout engineer either directly using netlist annotation or simply by supplying notes. The PCB has been viewed simply as a vehicle for connecting the components together. A component carrier … but not a significant electronic component in its own right!

Often when using traditional PCB signal integrity solutions it is seen that these designs look good in simulation but when they are built and tested in their prototype form, the designers achieve very different results. As a consequence, these design groups (circuit and layout engineers) find themselves spending a lot of time and money on redesigns, re-spins, excessive time experimenting on the test bench, and adding cost to their final products with additional "fix-it" components like caps and inductors, etc.

With a 'slow' waveform edge or transition, the chip bond wires, package leads and PCB routing can be considered as a lumped system, perhaps reduced to a simple RLC network. Indeed this model

simplification technique has served the design community well from the time that SI issues became an issue with PC designs operating in the low tens of megahertz. A single lumped element equivalent circuit RLCK model of the interconnecting tracks was good enough that SI analysis could be done to confirm that interconnect timing constraints were sufficient to ensure the quality of the signal. The K term captures coupling between adjacent conductors. The simulation would have been conducted using a transient time domain solver.

Transmission Line Models and dispersion

At higher frequencies and faster edge rates, these RLCK approximations begin to break down for several reasons. The capacitances of the various bond pads, cannot simply be summed into a single C equivalent, and nor can the inductances of the wires, package leads and interconnects be summed into a single equivalent L. The interconnect model needs to recognize the finite propagation velocity and thus needs a transmission line model. More importantly the dispersive nature of the interconnecting tracks also needs to be recognized. The result is that the commonly used RLCK modelling and simulation technology can no longer provide accurate or dependable results. This means that the lumped capacitive and inductive model of the track is abandoned and replaced with a true transmission line model. At this point we have two choices, account for the average propagation delay by using the ideal transmission line model that is found in all EDA tools or more accurately account for dispersion and use the microstrip model traditionally found in RF/Microwave design tools. Dispersion means frequency dependent propagation velocity. This manifests itself in the observation that short bursts of ones and zeros propagate at a different rate when compared to long streams of ones and zeros. This leads to timing jitter which is most conveniently viewed by using the so-called eye diagram. The eye diagram is produced by the overlaying or folding of many traces of the received RF voltage amplitude at the instant of data sampling.

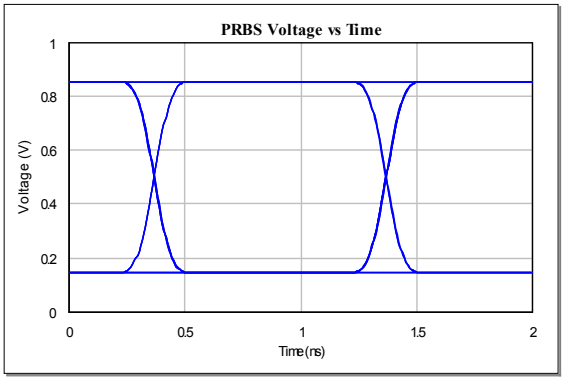

Figure 1: Perfect Eye Diagram

The eye diagram of an ideal dispersive less system (Figure 1.) illustrates several important characteristics. No jitter at the data transitions, no drop or pulse distortion and a healthy eye width are observed. If the same data is transmitted through a system that exhibits significant dispersion the eye diagram (Figure 2) illustrates several characteristics. The pulse transition phase shows considerable jitter, the height of the eye has been reduced and lastly an amplitude ripple has been introduced into the steady state period of the pulse. It is important to remember that the jitter has been introduced into the system by a passive structure. No account has been made of the PLL jitter of clock recovery circuits and phase detector noise. The behaviour of the trace represents the jitter floor beyond which improvements can only be made by reducing the trace length or introducing some form of dynamic pre-emphasis.

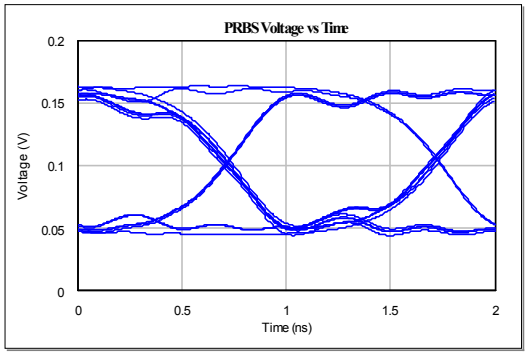

Figure 2: Simple Dispersion Example

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The analysis above used the simple case of 300mm of 50 ohm track on a 1mm thick substrate (Er = 3.38). A more realistic analysis of signal propagation takes account of the chip / package / trace / Via effects. When these effects are accounted for the eye diagram becomes even further degraded (Figure 3.).

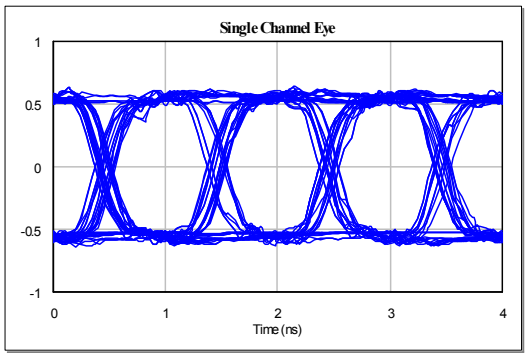

Figure 3: Dispersion and termination effects

With poor package design, coupling to adjacent traces, poor via design the eye diagram can become significantly degraded (figure 4.).

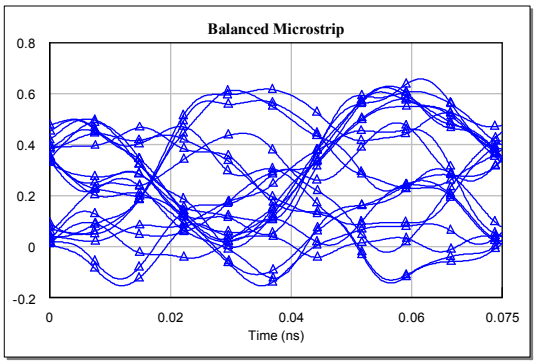

Figure 4: Poor system design

Printed Circuit Board Technology

For the vast majority of technologies employed in modern electronic systems the signals are being transmitted along copper traces embedded in epoxy fibreglass laminates (FR4). A typical multilayer stack consists of several double sided FR4 sheets laminated together using glass cloth, pre-impregnated with epoxy resin (pre-preg). Typically FR4 has a loss factor of approximately 0.02 at 1GHz, an order worse than exotic materials such as Alumina or PTFE derivatives. Higher cost materials with improved resins can reduce this to 0.009 or so. Whilst these improved materials represent a significant additional cost; where possible, designers are employing stacks which only require the improved materials to accommodate the layers containing the high speed tracks. This can be a cost effective method of achieving a high-performance board for mixed signal applications and remain commercially competitive. Of equal importance is the dielectric constant (Er) of the fibreglass which has a direct influence on the characteristic impedance of the tracks. The magnitude of Er needs to be as low as possible to allow for reasonable impedance levels in single and multilayer designs. By switching to a lower Er material, higher impedances than would otherwise be possible can be achieved for a given track width; and at the same time minimize conductor losses. This is particularly beneficial with stripline traces. If balanced stripline is employed for the best quality interconnect then the lower Er allows the gap between the tracks to be relaxed, in turn easing manufacturing problems with etch tolerance.

Several physical processes give rise to propagation velocity dispersion. Firstly let us consider a lossless system of conductors. For microstrip, either balanced or unbalanced, the conductor(s) sit on top of the FR4 dielectric, which in turn has a ground plane backing. Above the copper tracks, air is the main dielectric. The field patterns surrounding the conductors are found in both the FR4 and the air. As the frequency of the signal changes so does the ratio of energy in the fields in the FR4 and air regions leading to a phase velocity change. Ideal stripline is constructed using a homogenous system of dielectrics; the tracks are buried between two ground planes separated by a uniform dielectric. In this homogenous system the phase velocity is constant. Modern RF/Microwave tools are able to model such systems with ease, and trade offs between microstrip versus stripline or unbalanced versus balanced signal paths can readily be made. With the frequency dependence of loss added to the transmission line model it is seen that all systems exhibit dispersion. Edge and skin effects mean that the current density changes with frequency leading to resistance changing with frequency. These effects are well known to the microwave community, and models that account for them have been available to microwave designers for some considerable time.

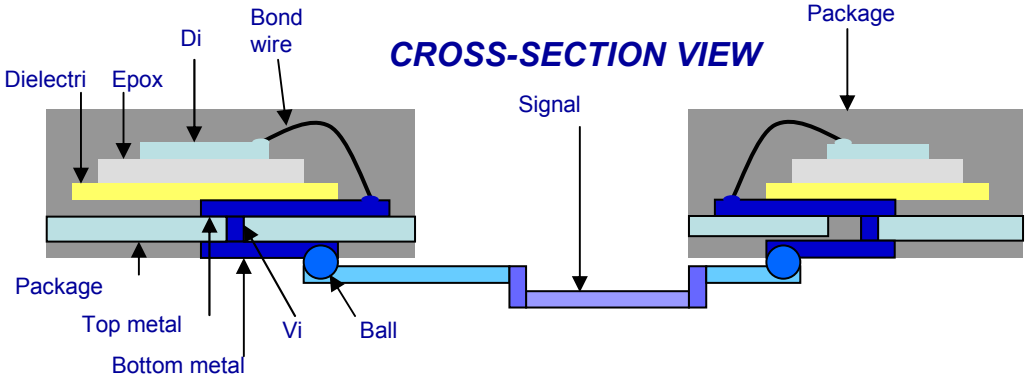

Figure 5: A signal path

Up to this point the discussion has concentrated on the propagation properties of the tracks used between packaged high speed chips. The other issues that need to be addressed for a successful circuit design are the design and the careful use of Vias, signal coupling between adjacent tracks,

impedance mismatches dues to unwanted steps in track width, the models for packages and chip models.

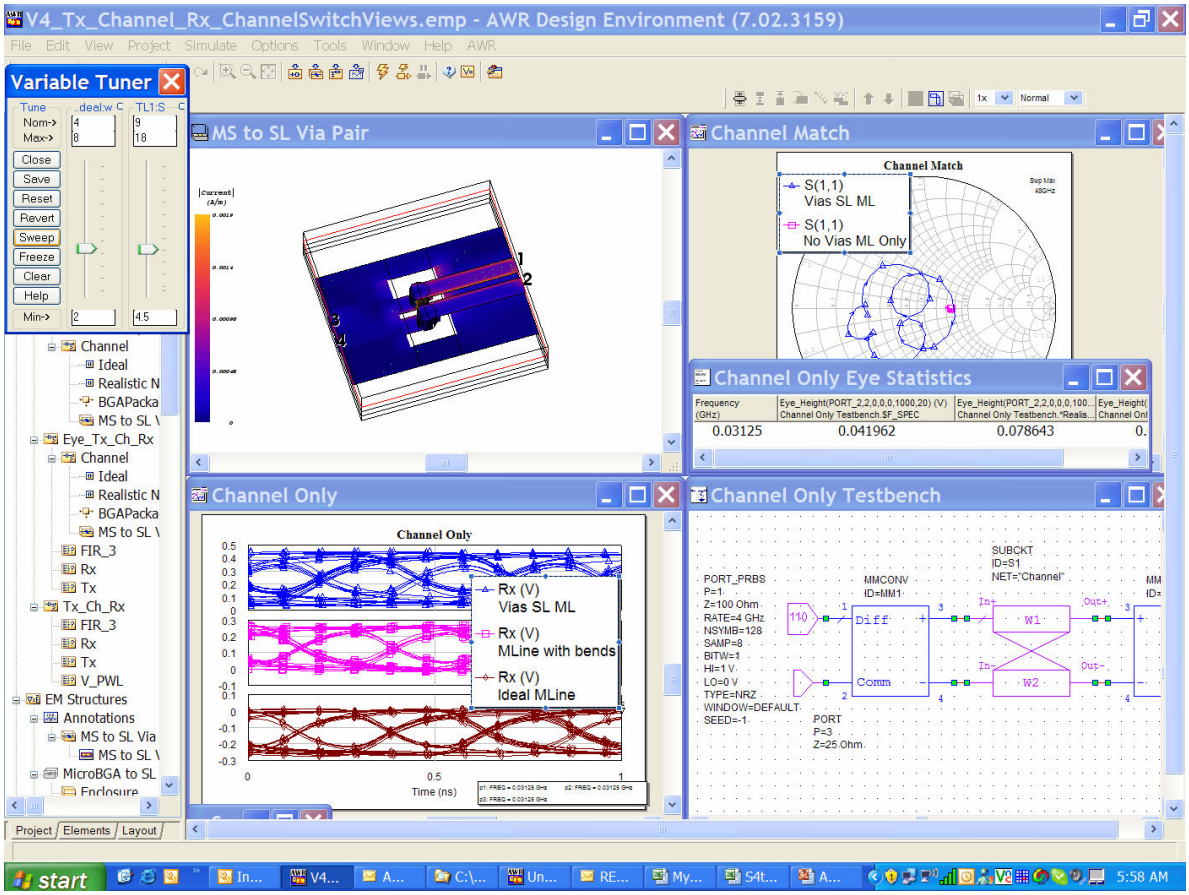

Figure 6: Via Design and Modelling

For the majority of cases the built-in Via model found in microwave EDA tools meets the needs of the high speed analogue designer. Nevertheless there will be occasions when a specific Via structure does not have such a model and it is necessary to make use of an EM solver. Two classes of solver are available to the board designer; 3D planar Method of Moments or 3D FEM/FDTD. For simple tasks the former is the most efficient, but for more complex feed through designs the latter class of solver is better suited as it makes fewer approximations. Each has its own place in the designer's tool box. Most importantly the integration of these solvers into the circuit design environment is of paramount interest to the designer. The flow of data (mechanical OUT, S parameters IN) needs to be entirely automatic with the minimum of user interaction. Tools such as Applied Wave Research's Microwave Office have tight links between the circuit solver and the EM solver using the EMSocket™ technology. With this design environment and data flow it is simple to affect a small change in the dimensions of the feed through connections and see the effect upon the eye diagram (figure 6, figure 7).

The internal design of the package equally can make use of either a combination of advanced bond wire model and EM data for the package leads or adopt an entirely EM based approach. The latter method whilst having the appearance of providing a definitive model suffers from being too rigid and not allowing for design trade offs with chip IO design, leads and package design.

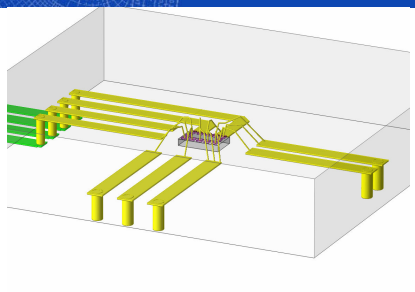

Figure 7: Chip and package

Coupling between adjacent tracks can be modelled by using general purpose simulation elements that make use of quasi-static 2D solvers. These models are less restrictive compared to the closed form analytical models and in the majority of cases yield more accurate results. In this example (Figure 8) a balanced system of tracks (green) runs close to a track that may carry an interfering signal (gold). Advanced models such as these are readily available with RF/Microwave design tools.

Figure 8: Multiple Coupled Lines

Transient and Harmonic Balance Simulation

During the discussion of modelling high speed traces no mention has been made of the type of simulation tools needed to create eye diagrams. Many PCB designers assume that a transient time domain "Spice like" circuit solver must be used for this type of simulation. This is not actually the case, as many Harmonic Balance (HB) solvers support eye diagram simulations and more importantly are able to calculate eye diagram statistics, such as eye jitter, eye height and eye width.

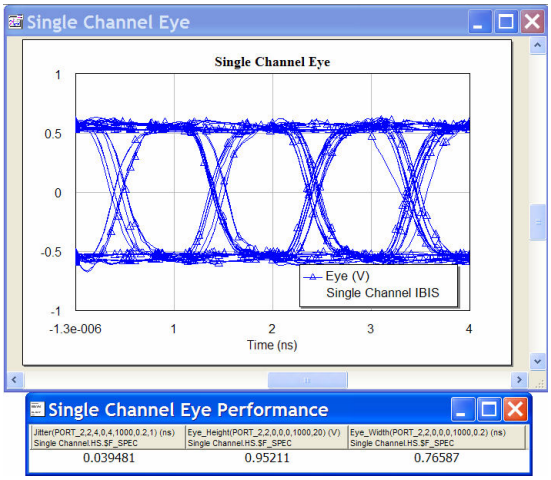

Figure 8: Built in Eye Diagram Statistics

For eye diagram simulations the HB circuit solvers have circuit elements for injecting Pseudo Random Bit Stream (PRBS). The main parameters that the designer defines for this element are

number of bits in the stream, the Hi and Low voltages and the signal format, Non-return to Zero (NRZ) and Return to Zero (RZ). For simulation, the PRBS waveform is converted from it's time domain representation to a frequency domain representation and it this calculated spectrum that is used by the HB solver. Using such techniques the designer is able to use the speed and efficiency of the HB solver. This speed permits fast tuning and optimisation of the circuit interconnect design. Thus very rapid design tradeoffs can be accomplished whilst varying track and board parameters.

To get a handle on track to track isolation and the injection of interfering signals, a simple provisional track layout can be created and viewed. Again, the multiple coupled line models can be exploited for their simulation speed. Extra PRBS sources can be added to the schematic and by using new seeds for the random numbers needed to generate a fresh bit sequence plus the addition of extra track lengths; one can ensure that the signal transition of the unwanted signal can be brought into the wanted signal clock sampling time. As is well known, the coupled energy is a maximum during the signal transition. By adjusting the distance between the wanted tracks and the interfering track (Figure 9) the degradation in signal shape is seen.

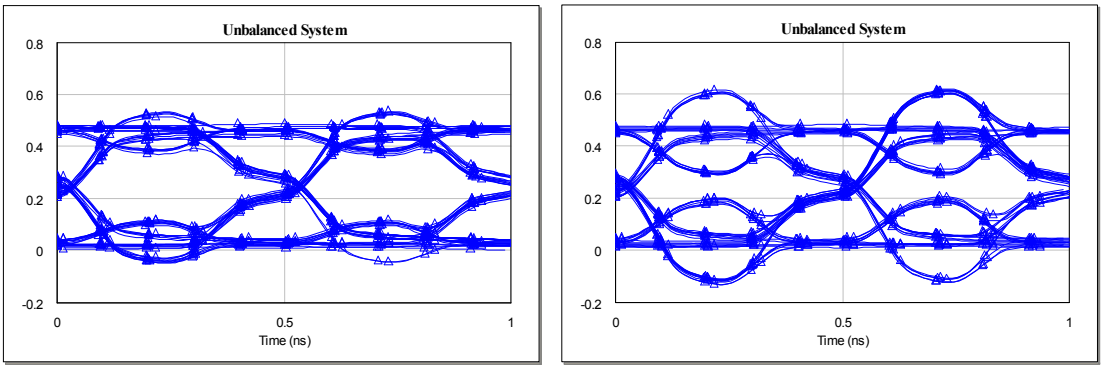

Figure 9: Cross talk … onset of interference (left) degraded isolation (right)

IBIS and Encrypted HSpice models

Often the chip/package model is available in the form of an **Input/Output Buffer Information Specification** (IBIS) model. The IBIS model is a combination of linear and non-linear model. The linear model defined by an RLC network defines the behaviour of the package leads. The nonlinear model in the form of IV tables captures the relationship between the device terminal voltage and current. Many tables include fast, typical and slow devices so the spreads in chip performance can be accounted for.

voltage	I(typ)	I(min)	I(max)
-0.6000	-42.7914mA	-24.7000mA	-59.9030mA
-0.5000	-35.9585mA	-21.5310mA	-51.2445mA
-0.4000	-28.9090mA	-17.1951mA	-41.6658mA
-0.3000	-21.7700mA	-12.8171mA	-31.6078mA
-0.2000	-14.5500mA	-8.4669mA	-21.2999mA
-0.1000	-7.2860mA	-4.1830mA	-10.7600mA
0.0000	37.0000fA	0.7000pA	1.2700pA

Table 1: Section from an IBIS file. (Voltage and Current table)

When an IBIS or encrypted HSpice model is used for a packaged component such as a high speed FPGA, a transient time domain solver is required for circuit simulation. Both IBIS and encrypted HSpice models protect the chip manufacturers IP. If this is this case; models for passive structures (perhaps EM modelled interconnections) and dispersive transmission lines need to be converted into a form suitable for transient simulation. The EM modelled interconnections and dispersive transmission line models are frequency domain models, these models can be directly used in a HB simulation.

When two tracks of different width are connected together a field discontinuity is created. This discontinuity does not cause problems at low data rates, but at high data rates, that is at high frequencies, this may not be the case. Located at the junction of these two tracks we find stored energy in the form of an evanescent mode. Classical models of these discontinuities often use negative circuit elements which in the context of Harmonic Balance simulation do not pose a problem. For transient simulation negative element values can give rise to convergence problems. Driving circuits with a few volts may result in the simulator predicting kilovolt outputs!

The AWR Design Environment is able to translate passive structures represented by S-parameter data sets into equivalent models and avoid the need for dynamic convolution. Dispersive transmission line models such as the MLIN element (Microstrip) are converted into the HSpice W-Model, which uses a generalized modelling capability for lossy coupled transmission lines. The HSPICE "W-element" models transmission lines based on RLGC matrices. This is a very general approach, applicable for any transmission line system. The RLGC values can have frequency dependence, allowing the modelling of higher frequency loss effects (such as skin effect and dielectric loss) and for modelling dispersion (frequency dependent propagation factors).

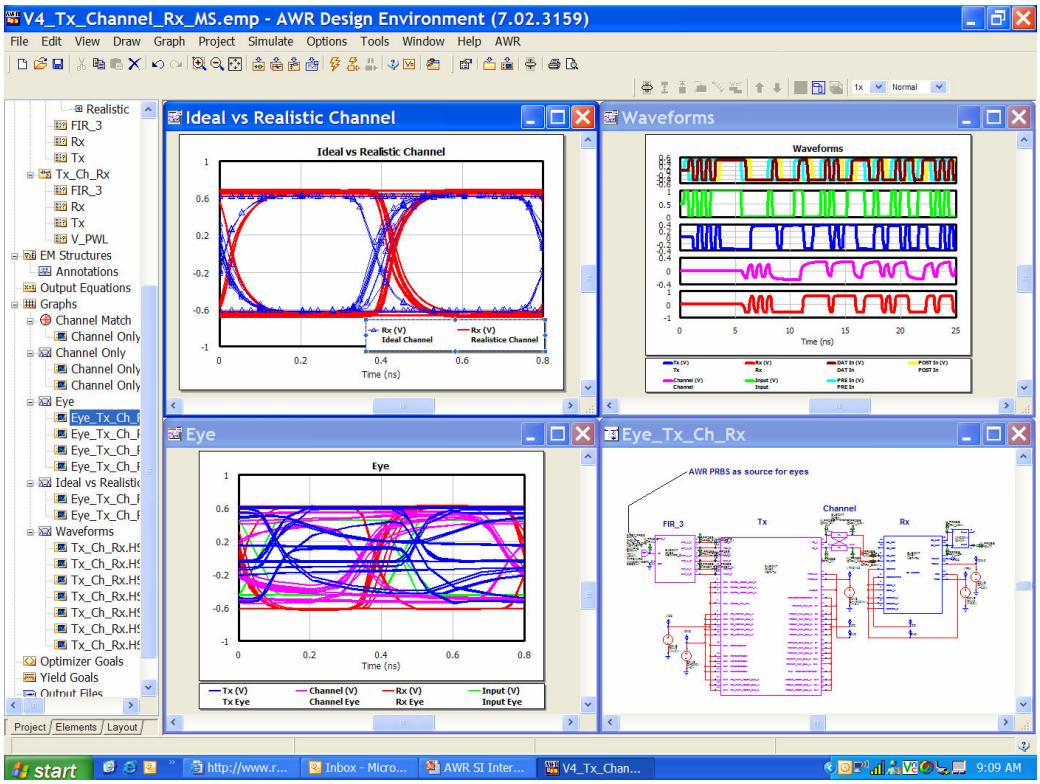

Figure10: The AWR Design Environment using HSpice for circuit simulation

Links to PCB tools

Whilst the final layout of the design will be conducted using a PCB design tool, the accurate models for complex high speed analogue circuits are to be found in RF/Microwave tools. It is important that the links between these tool sets is efficient and simple to use. With common file formats and the use of an advanced and comprehensive application programming interface (API) such links can be built. Ideally the links must support a bi-directional flow of information.

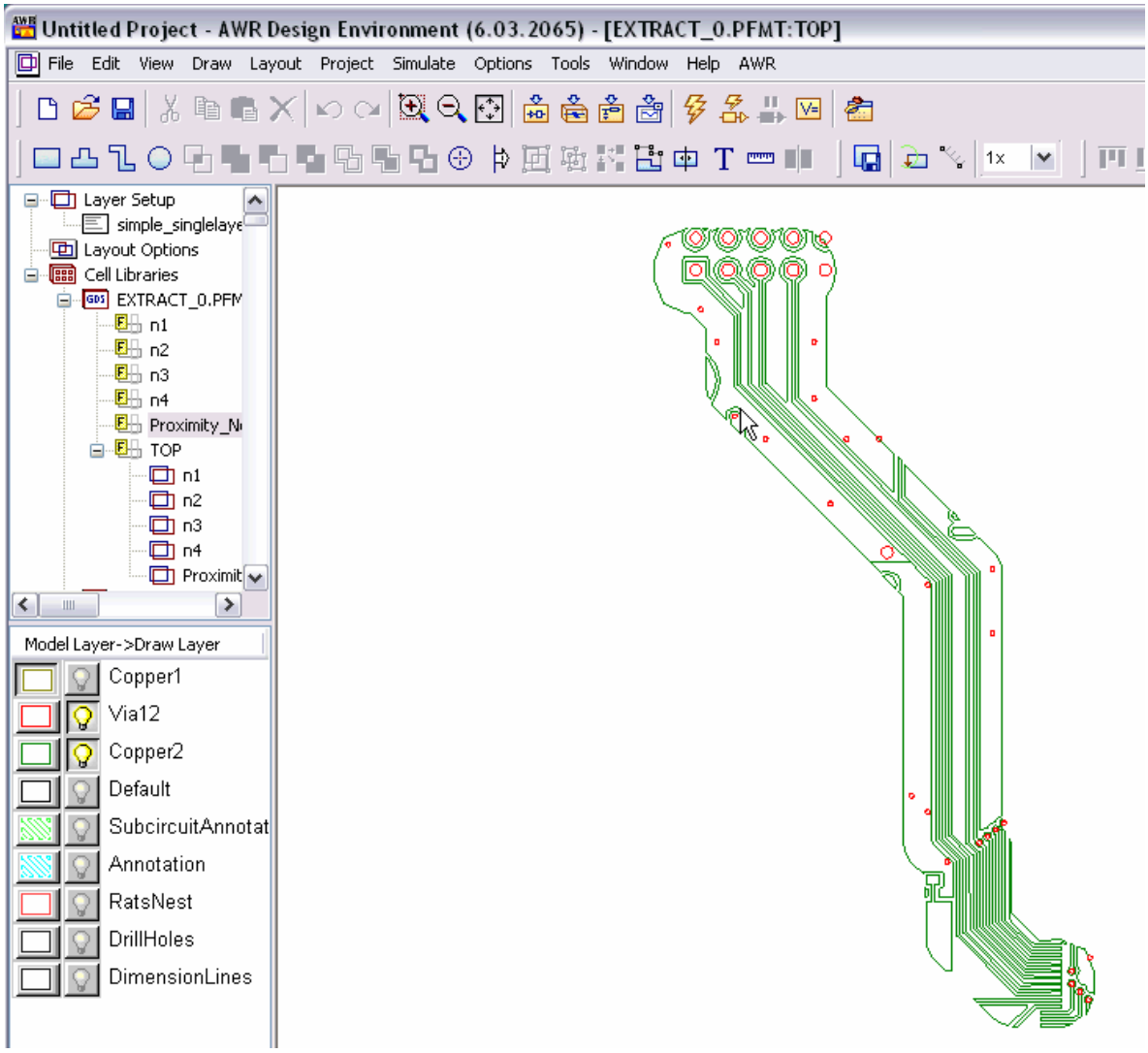

Figure11: Imported track data

In some cases the design may proceed to the point of board layout, and the generation of Gerber data for mask manufacture. It may be necessary to extract the critical track data and subject this to some EM analysis. By selecting the specific tracks for examination considerable time can be saved by not submitting the entire design to the EM solver (Figure 11).

Conclusion:

The emphasis of this paper has been on the need to have accurate high frequency models for use during SI design. By using high frequency simulation tools at the earliest opportunity in the design cycle, an approach which is known as SI Design, the designers can avoid costly mistakes. SI Analysis on the other hand tends to be a post design debugging process. With a hundred components and a thousand tracks this approach is most often less appealing. In such situations EM and circuit analysis become over burdened with data and sifting through simulation results is a challenge. If post design EM analysis is unavoidable, then a mechanism for data culling is highly desirable. Understanding the behaviour of the tracks, Vias, the tradeoffs between single ended and balanced system, maintaining characteristic impedance are all critical to a successful design process.