VNA Calibration Modifications and Hybridizations for Simplified High Frequency Multiport/Differential Measurements

J. Martens, D. Judge, and J. Bigelow Anritsu Company 490 Jarvis Drive, Morgan Hill, CA 95037 US

<u>Abstract</u>

As multiport and differential VNA measurement needs move beyond 50 GHz, measurement complications increase. Solid state switch insertion losses and costs increase enough that incomplete switching fabrics are often mandatory. In addition, system requirements may preclude optimal reference coupler placement. These issues lead to some complications with the traditional switch correction techniques used with the LRL/LRM class of calibrations. An approach based on a two-tier load match correction has been implemented to help handle the pathology of this situation. An additional problem that appears is the increasingly imperfect behavior of available thru lines, particularly in wafer probing applications. One approach to solving this problem is a hybridization of SOLR techniques with SOLT or LRL/LRM methods depending on the test port configuration. Single-ended and differential measurements to 65 GHz illustrating both of these principles are presented and compared against traditional methodologies in asymptotic cases.

I. Introduction

The need for differential and multiport S-parameter measurements continues to move up in frequency, whether the application involves communications components, gigabit Ethernet backplanes, or other devices. A common cost-sensitive approach for performing such measurements consists of placing a switch fabric (for multiplexing) in front of a receiver and source matrix (usually part of a 2 port VNA). In some cases, all of the couplers are behind the switch matrix such that standard 2-port VNAs can be used directly (see Fig. 1, e.g., [1]-[3]). In this case, a series of 2 port calibrations are renormalized against the off-state impedances of the various switches before combining.

For measurement repeatability and system longevity, solid-state switches are often preferred but above 40 or 50 GHz, the insertion loss (per unit isolation) of such switches usually becomes quite large (often > 10-15 dB at 60 GHz for 100 dB of isolation). The insertion loss of a reasonably modern 60+ GHz PIN diode switch is shown in Fig. 2. At these higher frequencies the losses in front of the test coupler can become unacceptable from the point of view of raw directivity and hence measurement stability. For this reason, this paper will focus solely on systems in which at least the test couplers are in front of the switch matrix.

Such a switch fabric (that allows at least all two port combinations) would be a possibility then with test couplers moved out to the test ports (e.g., [4]-[5]). While this does remove some stability issues, the insertion loss is large enough at higher frequencies to severely impact dynamic range (even before considering the loss in the coupled arm multiplexing that is not shown in Fig. 1). In addition, the classical placement of reference couplers may not be practical for system integration reasons (e.g., source locking). Besides the above, the cost of a more classical fabric may become prohibitive at these frequencies. For these reasons, a simplified test set (not a full switching fabric) such as that shown in Fig. 3 may be desirable.



Each gray box represents an SPDT terminating switch

Figure 1. One approach in which the internal VNA couplers are used with an external switch matrix is shown here. At higher frequencies, the switch insertion losses affect raw directivity and measurement stability.



Figure 2. Insertion loss of a 100 dB-isolation, 65 GHz SPDT switch is shown here. The 7+ dB insertion loss at high frequencies can impact architecture choices.

While simple, less costly, and providing of maximum dynamic range; such a structure does have disadvantages. The previously discussed technique of combining two port calibrations with renormalization is not possible due to the limited fabric, but a direct four port calibration is possible (due to the test coupler positioning). The fully referenced approach of [4] is also no longer possible. When attempting a direct four port calibration in the test set of Fig. 3, one must address the question of consistent terminations of non-driven ports. If four S-parameters are measured at a time in this configuration (using the VNA's internal transfer switch termination as the measurement termination); then when the driving port changes, so does the load match. One option is to ignore differences between load match and source match but this approach increases measurement uncertainty and will not be used here.



Each gray box represents an SPDT terminating switch

Figure 3. A simplified test set addressing some of the high frequency issues of Fig. 1 is shown here. The reference coupling has been moved to back before the demultiplexing switches and the switch fabric has been reduced. There is somewhat less flexibility on the driving port selection and all combinations of 2 port calibrations are not possible.

II. Four port calibrations and the relationship to the test set

Much has been written about multiport calibrations (e.g., [1]-[5], [11], [12]) and the intent of this document is not to revisit all of the algorithmic choices possible. Rather, there are a few points that have a direct impact of test set structure that will be discussed.

All of the commonly known 2-port VNA calibration algorithms have multiport analogs [5]. Thus one can select an approach that fits the application needs in terms of standards realizability, robustness, absolute accuracy, etc.. There are several ways to realize the multiport calibration from these basic concepts but one useful approach is as follows:

- a) extract reflectometer parameters (directivity, source match, transmission tracking) one or two ports at a time using a conventional 2 port algorithm.
- b) During the steps of part a), also obtain some of the transmission tracking (and perhaps isolation) terms
- c) Through a combination of additional line connections, get all of the remaining transmission tracking terms

So far, no statement has been made that affects the test set directly except to ensure that all 16 Sparameters can be measured. Using SOLT, one would connect an open, short and load to each port in turn followed by line connections between at least 3 port pairs [5]. Using TRL, one may perform a pair of conventional TRL calibrations (lines and reflects only) between two disjoint port pairs to complete steps a) and b) followed by at least one additional line connect to complete the transmission tracking terms. Where the complications arise is how the ports are terminated when the various lines (and the DUT) are connected. If one followed step c) naively, one may setup the test set to terminate both ports of the line at the VNA in every case. This presents a problem when measuring the real 4 port DUT in that only 2 of the 4 ports are VNA-terminated thus the other two ports would be terminated in a load match not present during the cal. While there are renormalization ways around this problem [1], they do not apply to the simpler test sets like Fig. 3. Here we must make sure during the calibration that every line measurement is terminated at the test set. This causes issues with certain calibration algorithms as is discussed in the next section.

A second issue revolves around the practical lines that can be used during a four port calibration. Depending on the hardware orientation, some paths may allow higher quality lines (in terms of return loss and insertion loss) than other paths. Since there is some redundancy in many calibrations, we may want to weight some paths over others. Additionally, it may invite the use of algorithms less dependent on the reflective nature of the lines such as SOLR which will be discussed in the fourth section. The limits discussed above on how the lines are terminated affect this algorithm as well.

III. TRL/LRL/TRM/LRM complications

In the TRL/LRL/TRM/LRM family of calibrations (e.g., [6]-[8]), a switch correction is normally used to account for the changing state of the transfer switch. A measurement at the non-driving reference coupler is typically used (with convenient ratioing) to get a measure of the reflection coefficient of the off-state of the transfer switch (e.g., [9]). In more complicated systems, this approach has other issues in that the load match becomes less a function of the transfer switch itself and more a function of other intervening hardware. As long as this hardware does not change state, this is not much of an issue.

The configuration of Fig. 3 does, however, present a structure that changes state and hence the simple switch correction approach must be modified. The object of this section is to present a simple two-tier algorithm to properly handle the various load match presentations that are involved.

A. Modified TRL, etc. algorithm

Treat the problem initially as a pair of disjoint two port calibrations, arbitrarily between ports 1 and 3 and between ports 2 and 4 (see Fig. 4). Perform a conventional LRL/LRM calibration (using the usual switch correction). This allows one to directly compute many of the calibration terms: directivity, source match, reflection tracking, and some transmission tracking (those between ports 1 and 3 and those between ports 2 and 4).

Next, sequentially terminate the outboard switches and measure raw reflections (S_{ii}) with lines (usually the line used in LRM or the shorter line used in LRL) still connected between 1 and 3 and between 2 and 4. These need not be thru lines as a subsequent de-embedding step will take care of the line behavior.

- Measure S_{11} with the outboard port 3 switch in the terminated position
- Measure S_{33} with the outboard port 1 switch in the terminated position
- Measure S_{22} with the outboard port 4 switch in the terminated position
- Measure S_{44} with the outboard port 2 switch in the terminated position



Figure 4. The test set of Fig. 3 is shown with two lines connected for completing the load match analysis.

Next perform one port corrections of each of these raw measurements based on the reflectometer error coefficients already derived. These corrected measurements are now S_{11} ' through S_{44} '. Finally de-embed the behavior of the line (in Fig. 4) which may either be known *a priori* or determined from a γl (propagation constant) extraction as part of the LRM/LRL calibration [10]. These created values now define the load match of the outboard-terminated ports. The tracking terms mentioned above must be recalculated based on these load match terms and outboard-terminated transmission measurements. Here the raw transmission measurements have the line characteristics de-embedded as above.

There are eight remaining transmission tracking terms that can be obtained in a number of ways. In many differential wafer calibration scenarios, two probes on each side may be close together (say 1-2 and 3-4) making a well-defined measurement more difficult. Consider first the other paths 1-4 and 2-3. One additional line measurement (per pair) is all that is needed to complete another LRM set; two additional for LRL. If this is inconvenient and a line is well-known, a single transmission measurement per pair can be used to get the tracking terms between ports 1 and 4 and between 2 and 3. The last four tracking terms can be found similarly if the lines between those ports are sufficiently well-behaved. If not, redundancy can be used to compute them [11].

A complete set of error coefficients using a consistent termination state is now available. To emphasize, this approach does require that non-driving ports must be terminated within the test set (not at the VNA's transfer switch) for consistent loading.

B. TRL, etc. measurements

As a first test of this technique, a full four port LRM calibration from 40 MHz to 65 GHz was performed in coax using a standard V calibration kit. A delay line of 2.4 cm was measured using this consistent termination state and the multi-tier LRM process just described. The results were then compared with those from an ordinary 2 port LRM calibration where the load state was

determined by the VNA's transfer switch. Because the 2-port approach can determine the load match conventionally, this allows for some validation of the present technique. The insertion behavior with these calibration techniques are shown in Fig. 5.

The insertion loss differences are within the expected uncertainties and the phase deviations show the same form. There is some difference in the jitter distribution. It is believed this is due to averaging differences during the two calibrations and differences in the amount of cable flex required between measurement and calibration.



Figure 5. A comparison of transmission measurements of the delay line is shown here ('ts'- the present method, '2p'- conventional LRM in a 2 port context)). The phase measurement is a deviation from linear phase and is represented by the left axis.

A differential delay line was measured next and some of its transmission and mode conversion parameters are shown in Fig. 6. For comparison, the results will be compared to a 4 port SOLT measurement on the same hardware. Only one level of load match correction is required in SOLT since a switch correction is not used as part of that algorithm thus it also allows for a reasonable comparison.

Aside from some additional scatter and small insertion loss variations (20-30 GHz and near 50 GHz) in the SOLT results, the measurements compare well. It is believed that the SOLT deviations are due to the fairly coarse characterization of the standards used for this calibration. A larger set of standards with a statistical calibration approach may provide a better basis for comparison.

IV. Thru line complications

Whether in the TRL family as in the last section or in a defined standards family, another issue to address is that of the transmission line standards used. While common to most media, one issue becomes obvious in wafer probing applications and this is illustrated in Fig. 7.



Figure 6. The measurement of a differential delay line is illustrated in these two plots. The first was performed using the modified LRM calibration of this paper while the second was performed using a 4 port SOLT calibration. The left axis is for S_{c2d1} while the right axis is for S_{d2d1} and S_{c2c1} .

Assuming the probes are positioned as shown, lines from 1-3 and 2-4 can be constructed with good electromagnetic behavior to 65 GHz. The cross-over lines (1-4 and 2-3) and loop-back lines (1-2 and 3-4) may have issues. At these frequencies, avoiding reflections, radiative loss/sensitivity and other problems becomes difficult. These distortions will most severely affect the TRL family but SOLT will be impacted as well.

One could conceivably use something like SOLR throughout [13]-[15] but this has its own issues. One may want to stick with the TRL family to handle most of the terms for reasons of standards availability and one may want to avoid the load match degradation inherent in pure SOLR [15]. These arguments do, however, suggest a hybridization approach.



Figure 7. A collection of lines that might be used in a 4 port calibration (layout typical of balanced wafer probing) is shown here. While the 1-3 and 2-4 lines are often not an issue, the match and electromagnetic quality of the others raise questions at higher frequencies.

A. Algorithm

Start off by performing a classical (TRL family or SOLT family) calibration between ports 1-3 and 2-4. As discussed earlier, these initial calibration steps determine directivity, source match, reflection tracking, and transmission tracking (two port pairs). Using the techniques of the last section, load match can be determined.

Since the integrity of the cross-over and loop-back is in question, a logical step might be to apply SOLR (e.g., [13]-[15]) on one of these paths. As discussed in the references, SOLR uses an undefined network (albeit reciprocal) instead of a defined transmission line between ports. Unfortunately, SOLR also requires switch correction terms much like the TRL family in the previous section. On the other hand, since SOLR is being used in a secondary role in this case, all of the load match terms have already been determined. We can thus proceed with a slightly modified SOLR algorithm using pre-determined load match terms in lieu of the traditional switch correction. As discussed in [15], there are practical limits on the match and insertion loss that this network can have but the cross-over lines of Fig. 10 should not usually infringe those limits.

If we assume, without loss of generality, that SOLR is applied to the 1-4 and 2-3 lines, then the last four tracking terms (related to paths between ports 1 and 2 or between 3 and 4) can either be found with another SOLR application or via redundancy as in Section III.

B. Measurements

To see if this approach is viable, an experiment was run in a 4 port 65 GHz system in coax so that good lines can be used in the suspect paths for comparison. A series of calibrations were made and the same DUT, a balance delay line, was measured in each case. Since the match of this low loss device is the most sensitive parameter, it will be used as the basis for comparison. The

comparison will be made to a calibration performed with a good line in the suspect path (which would not be available in a practical application of this problem).

The following three calibrations will be judged relative to the 'good line' result. The good line in this case had a match better than -30 dB over the range and an insertion loss < 0.1 dB. The poor line in the following cases had a match ranging from -25 to -15 dB and an insertion loss sloping from 0.1 dB at the low end to 0.7 dB at 65 GHz.

Case 1: A poor line was used to define transmission tracking and load match for the port pair using SOLT.

Case 2: The load match from the 1-3 and 2-4 calibrations was used but transmission tracking was derived from the poor line connection and SOLT.

Case 3: Same as case 2 but the transmission tracking was derived from the poor line connection and SOLR.

The DUT match was evaluated in linear terms for all three cases and differences from a measurement based on the 'good line' calibration was computed. These differences are plotted in Fig. 8 and the averages (over the .1-65 GHz range) were 0.02 for Cases 1 and 2 and 0.004 for Case 3.

Cases 1 and 2 are very similar, in part because the traditional transmission tracking extraction is very dependent on having a well-matched line. Since a poor thru was used here, the transmission tracking calculation would be impacted even if a relatively accurate load match term was used. Although cases 1 and 2 were based on SOLT, the same measurements based on LRM had even worse agreement, presumably because of the stringent 'well-matched line' assumption in that calibration family. The transmission tracking in case 3 (using SOLR) is not dependent on that match assumption.



Figure 8. The delay line matches for a balanced delay line obtained with several calibration schemes (all relative to a 'good line' cal) are shown here. The best one, case 3, uses load match obtained from previous calibration steps and transmission tracking obtained from SOLR on a questionable line.

V. Conclusions

Some of the complications, and some solutions, related to high frequency multiport measurements have been discussed. The practicalities of test set construction above 50 GHz tend to force architectures where modifications to calibration algorithms, such as TRL, are necessary. The practicalities of the calibration structures for these measurements also tend to suggest algorithmic changes, this time hybridizing certain algorithms to work around line quality and load match issues.

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