A Low Cost, Plastic Packaged, 0.5W, 6-18GHz Amplifier MMIC

Stuart Glynn and Liam Devlin

Plextek Ltd, London Road, Great Chesterford, Essex, CB10 1NY, UK; (lmd@plextek.co.uk)

Abstract

This article describes the design, fabrication and evaluation of a low cost, SMT packaged, 6 to 18GHz amplifier MMIC. It was designed to occupy a small die area on a high volume, optically defined process and to be packaged in a low cost standard QFN plastic package. The resulting part provides >10dB of gain across the 6 to 18GHz band and has an output P-1dB of +27dBm.

1. Introduction

The aim of the development described in this paper was to produce a low cost, SMT packaged amplifier covering 6 to 18GHz and able to deliver a reasonable level of output power. Obviously power capability and cost are strongly linked and this trade-off is discussed in more detail below. An adequate level of gain is also important and it was determined that the minimum gain requirement should be 10dB.

2. Process Selection

In selecting the most appropriate process the following requirements were identified:

- Optically defined gate structures (for cost reasons)
- Acceptable die area cost (ideally 6" diameter wafers to help reduce cost per unit area)
- Adequate gain across the 6 to 18GHz frequency range
- Adequate RF output power capability

The PP25-12 process of WIN semiconductor was selected. This is a PHEMT process with 0.25µm optically defined gates. Wafer diameter is 300mm (≈ 6"). It is has a typical breakdown drain-gate voltage of 14V and is suitable for operation from a 6V supply. The wafers are coated with BCB (benzocyclobutene), which is a low loss, low dielectric constant passivation layer that helps to mitigate the effects of plastic packaging.

3. Design and Simulation

High power amplifier MMICs normally combine multiple output transistors to provide the required power levels. With the emphasis on low cost the approach taken with this design was to use a single output transistor. One of the first stages of the design process was therefore to select the size of the output device.

As the physical size of a transistor increases (more fingers or wider unit gate width) the available gain at microwave frequencies decreases [1]. It was necessary to choose a large transistor, in order to provide useful levels of output power. However, it was also important to select a transistor that could still provide adequate gain across the 6 to 18GHz band. The device selection process that was adopted is described in more detail in [1].

After initial simulations to determine the most appropriate device size, a transistor with 1.4mm total gate width biased at 36% Idss (approximately 200mA) at 6V Vds was selected for the output stage. Figure 1 shows the maximum available gain (Gmax) versus frequency for the selected output device. A two stage design would be required to achieve the target gain for the complete amplifier.

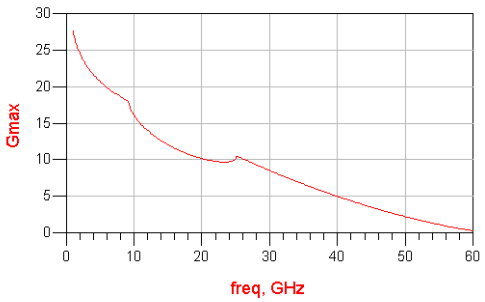

Figure 1: Gmax versus Frequency, 1.4mm device biased at 36% Idss, 6V Vds

The Gmax curve of Figure 1 exhibits a kink at 9GHz and another at 25GHz. At frequencies below the first kink and above the second kink the device is only conditionally stable. In these regions Maximum Stable Gain (MSG) is actually plotted rather than Gmax. Between the two kinks the device is unconditionally

stable. The extent of these regions of conditional and unconditional stability are influenced by the transistor size and grounding inductance in the device's source.

If a transistor is unconditionally stable with a Gmax of, say, 10dB then the gain of a reactively matched amplifier implemented using it would be less than 10dB due to the matching network losses and the gain sacrificed to flatten the gain versus frequency response. For a conditionally stable transistor with an MSG of 10dB, it is likely that additional gain would need to be sacrificed to stabilise the transistor. It is important to bear this consideration in mind when selecting the preferred transistor topology.

Having selected the output transistor the design of the output stage could commence. Figure 2 shows the schematic of the amplifier output stage. Fourth order low-pass matching networks were used to achieve the required bandwidth with a compact layout. A lossy matching component (R1) was required in the input match. This stabilises the transistor in the lower part of the band and also helps to flatten the gain response.

The inclusion of lossy matching at the output was avoided so as to preserve output power. The inductors L1 to L6 were implemented as micro-strip lines which were meandered in layout to achieve a compact design. The lengths of these meandered lines were optimised using an EM simulator. C9 and C4 provide in band supply decoupling, C1 and C8 provide DC blocking and C10 provides low frequency de-coupling of the drain supply. R2, R3 and C5 allow for low frequency stability and filtering of the gate supply.

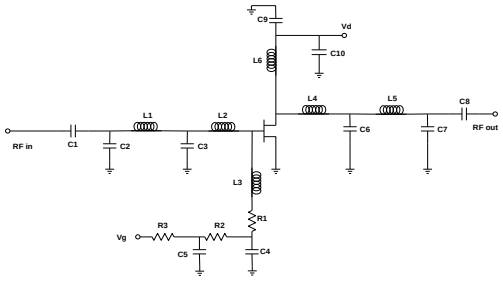

Figure 2: Schematic of the amplifier output stage

Figure 3 shows the schematic of the amplifier input stage. This has a similar topology to the output stage. The main differences are that the device has a total gate width of approximately half that of the output stage at 0.72mm and is biased at a quiescent current of around 100mA. Some output loss can be afforded for stability and is provided by R4. Series resistive filtering of the drain supply can be implemented as the slight drop in drain supply voltage due to R5 can be tolerated. Source degeneration (L7) is employed to achieve a good input match.

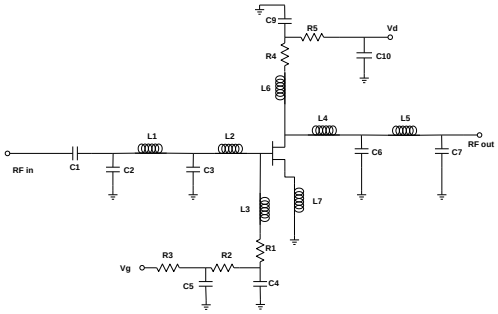

Figure 3: Schematic of the amplifier input stage

Figure 4 shows the simulated s-parameters of the 2 stage amplifier MMIC (bare die). The gain is 15dB ±2dB across the band. The input and output return losses are better than 10dB across the band.

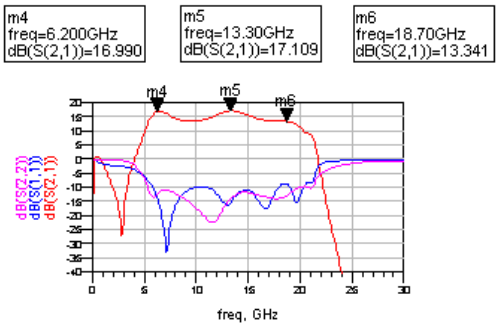

Figure 4: Simulated S-parameters of 2 Stage Amplifier MMIC

Figure 5 shows simulated P-1dB. This is over 27dBm across the full 6 to 18GHz band.

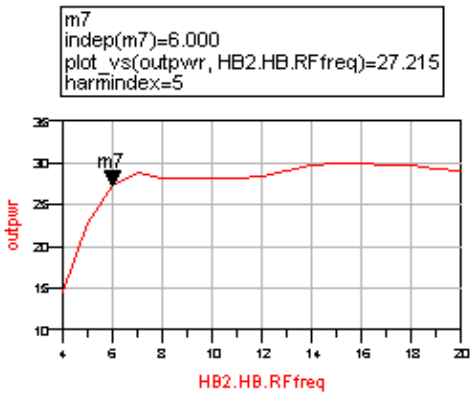

Figure 5: Simulated P-1dB of 2 Stage Amplifier MMIC

Figure 6 is a stability analysis showing that the amplifier is unconditionally stable from 10MHz to 60GHz. Detailed analysis of the

stability of each individual stage was also undertaken as part of the design process.

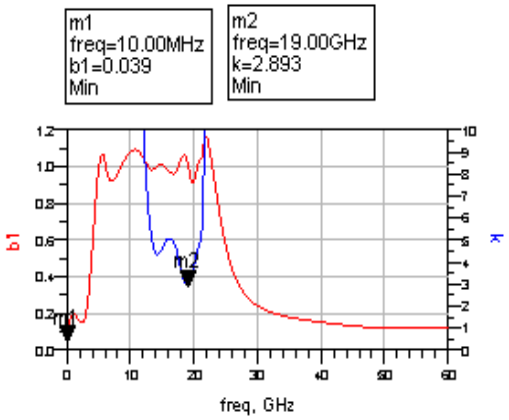

Figure 6: Simulated Stability of 2 Stage Amplifier MMIC

4. Realisation and RFOW Performance

A photograph of one of the amplifier MMICs is shown in Figure 7. The die area is 2.75mm^2, allowing over 5000 working amplifiers to be realised on a single 6" diameter wafer.

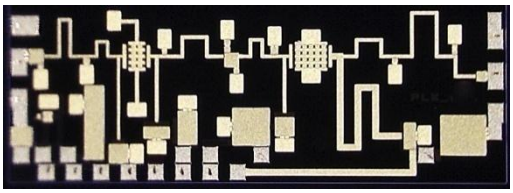

Figure 7: Photograph of the mixer MMIC

RF On Wafer (RFOW) small signal measurement was performed on the amplifier die. The measured s-parameters of 6 samples are plotted in Figure 8 to Figure 10.

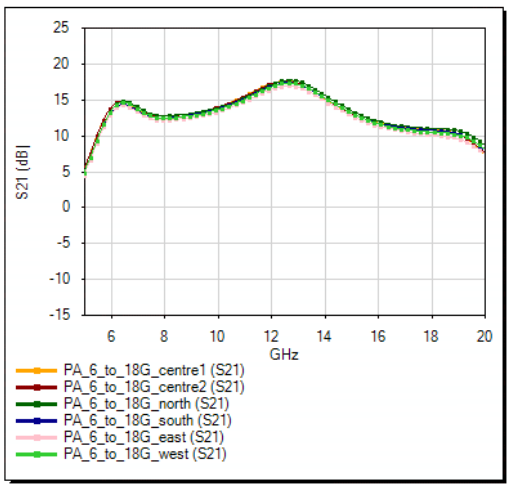

Figure 8: RFOW measured S21 of 6 devices versus frequency

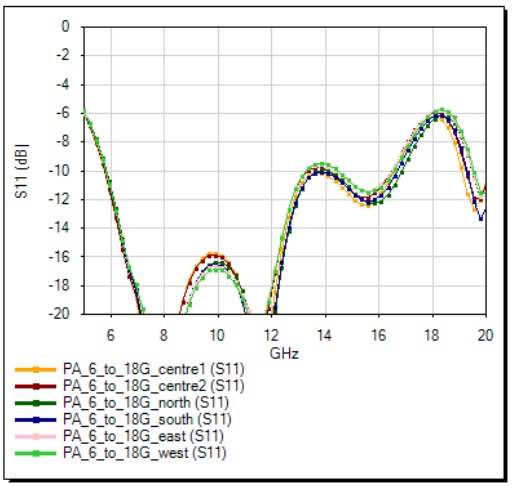

Figure 9: RFOW measured S11 of 6 devices versus frequency

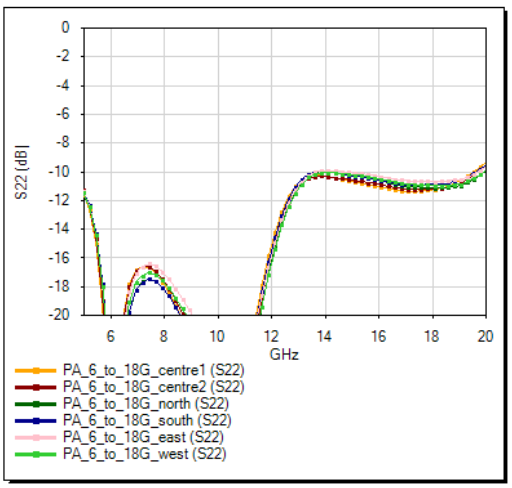

Figure 10: RFOW measured S22 of 6 devices versus frequency

5. Measured Performance of Packaged Parts

The ICs were assembled into standard QFN-20 plastic packages and assembled on to PCBs for evaluation. A photograph of one of the assembled PCBs is shown in Figure 11. The substrate material was Rogers 4003. All measurements presented below are referenced to the package pins.

The devices were biased at 6V and took a quiescent supply current of 277mA. The negative gate voltage is generated by an on-chip active bias network that takes 4mA from a -5V supply.

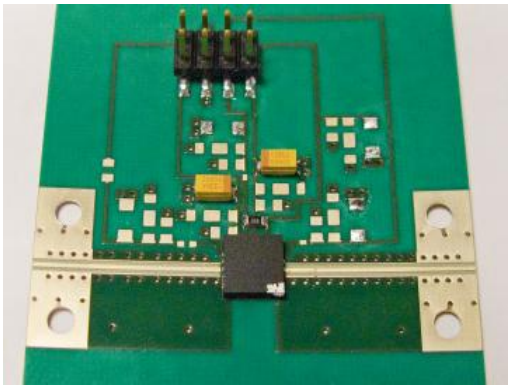

Figure 11: Photograph of packaged amplifier on evaluation PCB

The measured s-parameters of 3 packaged devices are shown in Figure 12 to Figure 14. Typical gain is 16dB ± 2.2dB from 6 to 15.5GHz dropping to 10.2dB at 18GHz. The input return loss is > 10dB below 17GHz and output return loss is > 9dB.

Examination of X-ray images of the packaged parts revealed that the die was actually sitting a little low on the lead-frame resulting in a slight increase in RF bondwire length. It is expected that correct alignment of the die with the RF input and output pins will result in improved return losses at the top of the band and a slight increase in gain at 18GHz.

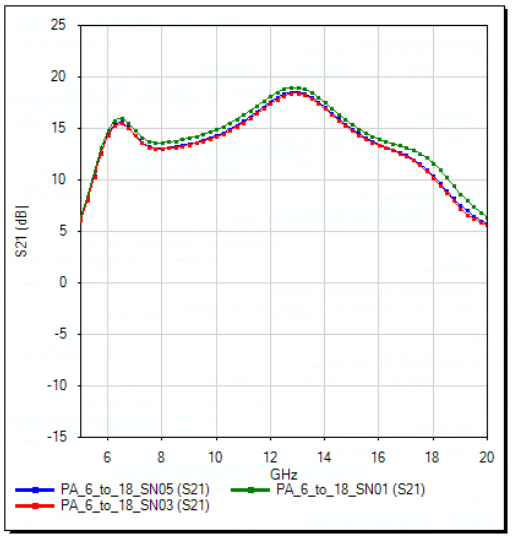

Figure 12: Measured S21 of 3 devices versus frequency

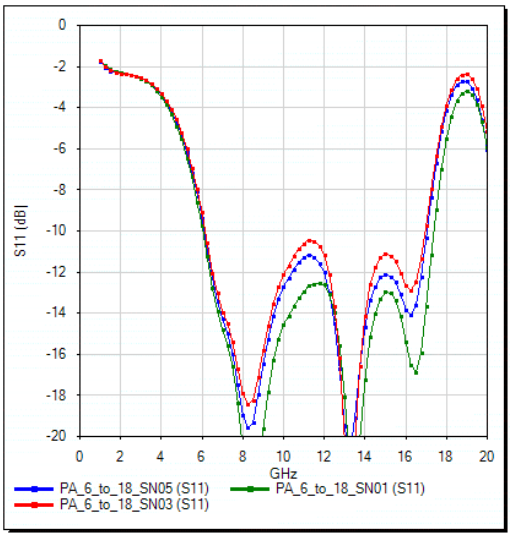

Figure 13: Measured S11 of 3 devices versus frequency

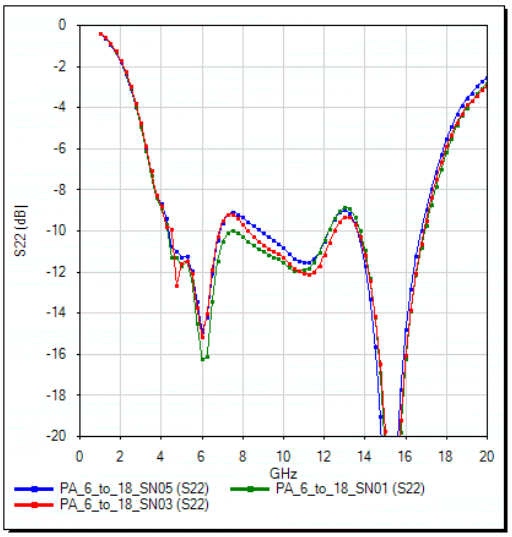

Figure 14: Measured S22 of 3 devices versus frequency

The 1dB gain compressed output power of a typical device is plotted against frequency in Figure 15. The typical P-1dB is around 27dBm, although it drops slightly below at the top and bottom of the band and peaks significantly above this in the 12 to 14GHz region.

Figure 16 shows the measured output referred 3rd order intercept point (IP3) versus frequency of 3 devices. Across the majority of the band the IP3 is around 35 to 36dBm.

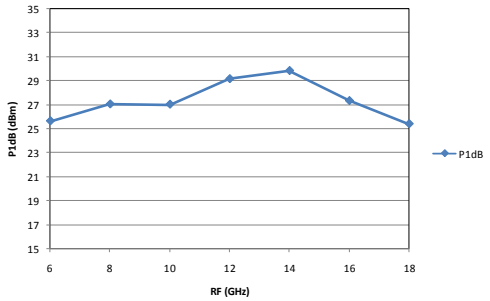

Figure 15: Measured output P-1dB versus frequency

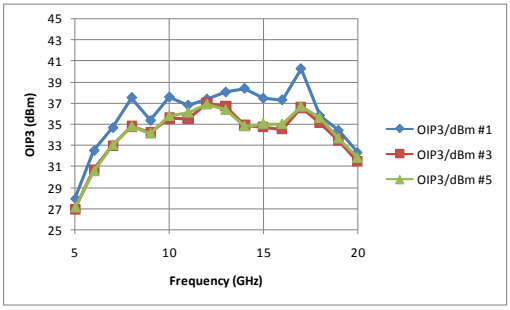

Figure 16: Measured output referred IP3 versus frequency

6. Summary and Conclusions

This paper has presented the design and measured performance of a low cost, SMT packaged, 6 to 18GHz amplifier MMIC. It exhibits a gain of over 10dB and a typical 1dB gain compressed output power of 0.5W.

7. References

[1] Devlin, L.M. et al "The Design of E-band MMIC Amplifiers" ARMMS RF & Microwave Conference, April 2010