

Ballasting HBTs For Wireless Power Amplifier Operation

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Abstract — This paper describes ongoing work to evaluate conditions for bias stability in large power devices, with particular emphasis on the interplay between thermal stability and electrical performance. We show that base ballast generally provides good thermal stability in HBTs, but only if appropriate levels of ballast resistance are used. Those values are surprisingly high. Base ballast may also affect saturation characteristics and thus linearity of power amplifier devices.

Index Terms — Power Amplifiers, Ballast, Thermal Effects, HBT.

I. INTRODUCTION

Thermal effects in both bipolar and FET devices have been a subject of major interest to power-amplifier designers since the beginning of solid-state power-amplifier technology [1, 2]. The initial interest was for thermal stability, as it was clear that silicon BJTs could be destroyed by thermal runaway. It rapidly became clear, however, that the uniformity of dc currents and drive levels in the individual cells of large power devices were extremely important as well, not only to prevent individual cells from failing, but also to prevent current collapse, a phenomenon particularly evident in HBTs [3].

Nonuniform cell currents can cause other problems in HBTs. For example, if the cell currents are not uniform, certain cells are driven more strongly than others. Then, the cells carrying higher RF power generate disproportionately high distortion. Such effects could be responsible for high IM or ACPR levels in power amplifiers. Such devices could also show a higher degree of memory effects. Similarly, base or emitter ballasting, methods to make the cell currents uniform, affect the saturation characteristics of the device in different ways, and thus affect large-signal distortion differently. This is especially important in amplifying signals having a high peak-to-average ratio. Finally, the method of ballasting can have implications for analysis, introducing ill conditioning and multiple solutions in the simulation of such devices.

II. THERMAL STABILITY AND BALLAST

The type and amount of ballast has always been a dilemma. Much of it, however, is based on simplifying assumptions that are not relevant to HBTs, such as neglecting the temperature dependence of static current gain (β). Some of the most important papers are those of Winkler [1], Liu et al. [3-5], and Gao et al. [6-7]. Later papers [8-10] provide further insight. Winkler is one of the earlier treatments on the subject of thermal stability. The papers by Gao focus on emitter ballast and those by Liu make the point that base ballast is most appropriate for HBTs, while emitter ballast is best for silicon BJTs.

A. Thermal Stability of Multicell Devices

A fundamental concern is to prevent classical “current hogging,” in which one cell in a power device conducts while the others are turned off. This phenomenon leads, in the most extreme case, to current collapse in power transistors. [1]. It occurs because self-heating causes the base-to-emitter voltage (V_{be}) of a cell eventually to decrease as collector current increases. If a second cell, connected in parallel, runs slightly cooler, the value of V_{be} necessary to cause the fold-back will not occur. Then, as V_{be} of the first device decreases, as its current increases, the current of the second device must decrease.

This phenomenon is illustrated by the simulations shown in Figure 1. The HBT is a foundry InGaP device, 1.6 x 30 μm , characterized by a VBIC95 model. The thermal resistances have been offset by approximately 10% from the specified value of 600C/W. Although this phenomenon depends primarily on V_{be} , we shall show that the behavior of β with temperature also has an important effect.

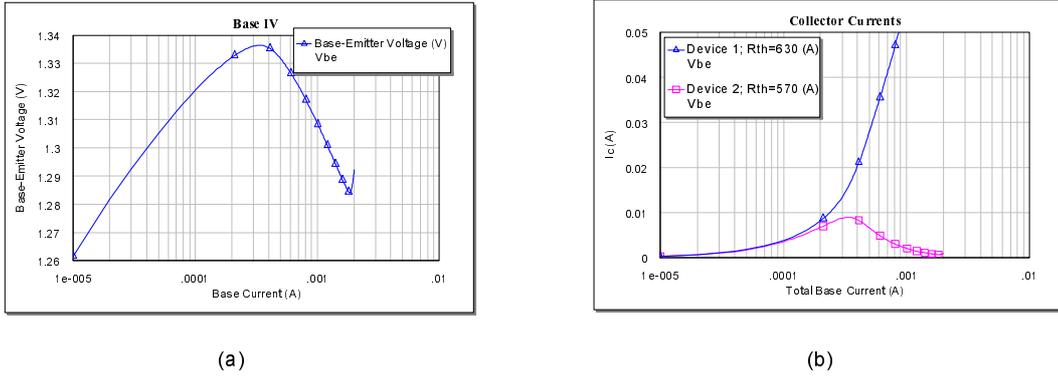


Fig. 1. V_{be} (a) and collector currents (b) in two HBTs connected in parallel as a function of base current. The base is driven from a current source. No external ballast is used.

Adding ballast prevents current collapse and makes the individual cell currents more nearly equal. Either base or emitter ballast can be used, although there are clear trade-offs between them. In the rest of this paper, we examine the effects of ballast not only on thermal stability but also on RF performance.

B. Base Ballast

Liu [5] makes a strong case that emitter ballast is optimum for silicon homojunction devices, in which the current gain (β) increases with temperature, while in HBTs, where β decreases with temperature, base ballast is preferred. We confirm this conclusion, but more needs to be said. We consider the circuit in Figure 2, which is simply DC biased. The temperature increase, ΔT , of a transistor is given by

$$\Delta T = \theta_{jc} P_d = \theta_{jc} I_c V_{ce} \quad (1)$$

where θ_{jc} is the thermal resistance, P_d is the power dissipation, and the other variables are defined in the figure. The thermal resistance is a function of both temperature and device geometry; for now, we shall view it as independent of temperature. The device temperature, T , is

$$T = T_0 + \Delta T \quad (2)$$

where T_0 is the baseplate temperature.

The collector current, I_c , is given by

$$\begin{aligned} I_c &= \beta(T_0 + \Delta T) I_b(T_0 + \Delta T) \\ &= \frac{\beta(T_0 + \Delta T)(V_{bb} - V_{be}(T_0 + \Delta T))}{R_{bb}} \end{aligned} \quad (3)$$

where β and V_{be} are explicitly functions of temperature. Substituting (3) into (1) gives

$$\begin{aligned} \Delta T &= \frac{\theta_{jc} V_{ce}}{R_{bb}} \beta(T_0 + \Delta T)(V_{bb} - V_{be}(T_0 + \Delta T)) \\ &= C_{tb} f_b(\Delta T) \end{aligned} \quad (4)$$

where C_{tb} is a coefficient and $f_b(\Delta T)$ is a function of temperature, which, in this case, is simply β times the voltage dropped across R_{bb} . V_{be} decreases monotonically with ΔT . In silicon devices, β increases with ΔT , so $f_b(\Delta T)$ increases with ΔT . In HBTs, β decreases with ΔT , so $f_b(\Delta T)$ may increase or decrease, depending upon the magnitude of the individual terms in (4).

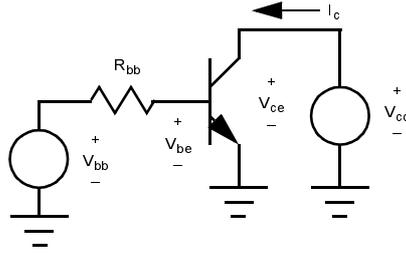


Fig. 2. Base-ballasted bipolar transistor (BJT or HBT).

Eq. (4) must be solved numerically or graphically. Graphing the terms provides good insight into the characteristics of various types of ballast. A graph of the terms in (4) is shown in Figure 3, where we have plotted the curves $\Delta T' = \Delta T$ and $\Delta T' = C_{tb} f_b(\Delta T)$. The intersection of these curves is the operating temperature increase. Figure 3(a) shows the case for silicon homojunction devices, where β increases with temperature. Figure 3(b) shows the case for HBTs, where β decreases with temperature. For most silicon homojunction BJTs, the dependence of β and V_{be} on T does not vary much between devices. C_{tb} , however, is under the designer's control, depending most strongly on thermal resistance, collector voltage, and especially R_{bb} , the ballast resistance. The designer can decrease this quantity arbitrarily by appropriate selection of R_{bb} .

Figure 3(a) shows the dependence of the operating point on C_{tb} in a silicon device. When C_{tb} is small, the bias point is unique and the device temperature remains low. As C_{tb} increases, however, a second solution to (4) becomes possible. Finally, when C_{tb} is large enough, no solution is possible, and thermal runaway occurs.

The curves also show, indirectly, the dynamic behavior of temperature after the device is turned on. At turn on, the device temperature is T_0 , so $\Delta T = 0$. Invariably, at this point, $C_{tb} f_b(\Delta T) > \Delta T$, so the device heats up until a stable thermal operating point is reached. In some cases, more than one operating point exists, the second at a higher temperature. This case is illustrated in Figure 3, the "Large C_{tb} " case. Unless the higher-temperature operating point is unusually close to the low-temperature one, the device does not reach the second operating point, and it is thermally stable. It is not unusual, however, for a circuit simulator to find the higher-temperature operating point and to present it to the user as the sole solution. The existence of multiple operating points is a reality that must be taken seriously in the design of models that include self-heating effects and in the design of circuit simulators that use them.

Figure 3(b) illustrates the behavior of HBTs. In HBTs, β decreases with ΔT , but the $V_{bb} - V_{be}$ term increases. Generally, $C_{tb} f_b(\Delta T)$ decreases with ΔT , especially when R_{bb} and, hence, V_{bb} are large. In this case, even with relatively modest base ballast, (4) has a single solution and thermal instability should not occur, even if C_{tb} is fairly large.

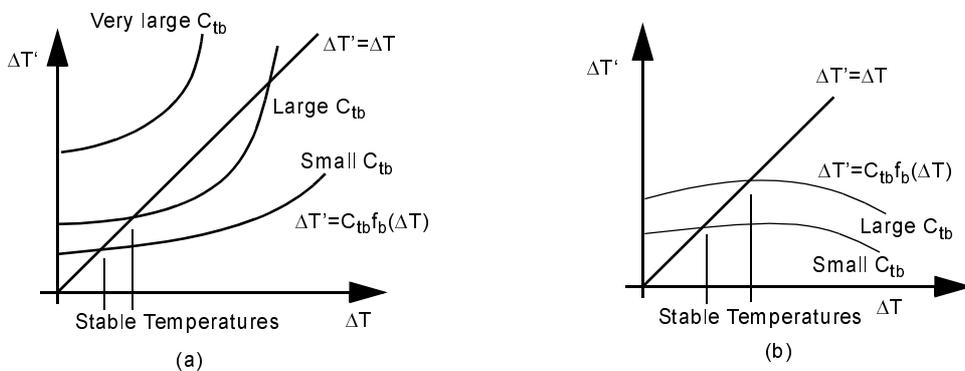


Fig. 3. Graphical solution of (4): (a) silicon homojunction BJT, where β increases with temperature; (b) HBT, where β decreases. V_{bb} is the same for both cases, so the stable operating temperatures represent different values of collector current.

Current hogging in the base can still occur, however, if the bases are connected in parallel. Thus, separate base resistors, R_{bb} , must be used for the individual cells. High values of R_{bb} require high V_{bb} , so V_{be} becomes small relative to V_{bb} , decreasing the effect of thermal variation of V_{be} . This improves the thermal stability substantially and equalizes the currents in the individual cells. This is the case even if current bias is used or the cell thermal resistances vary significantly. As a base-ballasting standard, we have used resistances great enough to assure cell currents within 5% at current densities up to 50 kA/cm², based on simulation with well validated models. This standard has completely solved earlier problems in obtaining high efficiency, which were believed to be caused by unequal cell currents.

From simple inspection of Figure 3(a), we can derive a condition for thermal stability at a single temperature:

$$C_{ib} \frac{d}{d\Delta T} f_b(\Delta T) < 1.0 \quad (5)$$

over the entire range of ΔT . This guarantees that only a single solution of (4) is possible, and that at least one will exist. Eq. (5) is a relatively strict requirement, as the higher-temperature solution of (4) is unlikely to be reached in practice. A weaker, but more practical criterion, is to satisfy (5) in the vicinity of the operating point. If

$$C_{ib} \frac{d}{d\Delta T} f_b(\Delta T) \sim 1.0 \quad (6)$$

near the operating point, the solution is indistinct and the problem of determining the operating temperature is ill-conditioned. In many such cases, (4) has no solution, indicating thermal runaway.

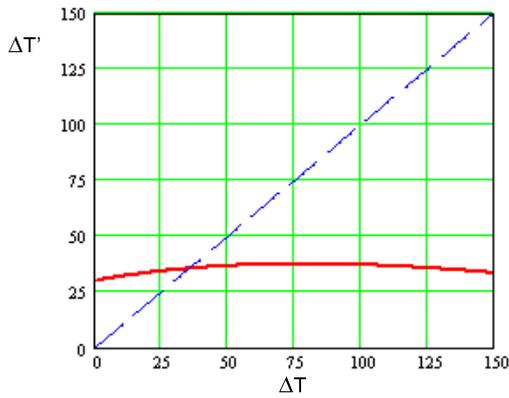
By substituting $f_b(\Delta T)$ into (5) and differentiating, we obtain

$$C_{ib} \left(\beta(T_0 + \Delta T) \left(-\frac{dV_{be}}{d\Delta T} \right) + (V_{bb} - V_{be}(T_0 + \Delta T)) \frac{d\beta}{d\Delta T} \right) < 1.0 \quad (7)$$

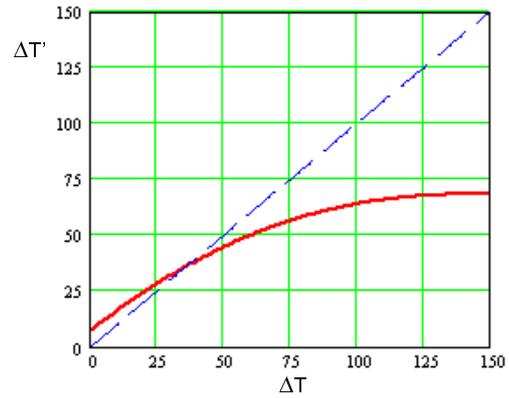
For silicon BJTs, both terms within the parentheses are positive, so (7) may be relatively difficult to satisfy. In that case, the designer's only degree of freedom for satisfying (7) is to adjust C_{ib} . For HBTs, however, the first term is positive, but the second is negative. In this case, (7) can be satisfied by making the second term large relative to the first; this requires, in turn, making the voltage drop across R_{bb} , $V_{bb} - V_{be}$, large enough. This must be done by increasing V_{bb} , which requires increasing R_{bb} , simultaneously decreasing C_{ib} .

III. BIAS-POINT NORMALIZATION

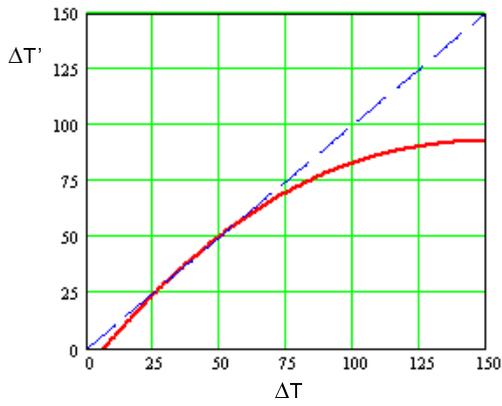
The thermal operating points in the curves of Figure 3 represent different values of collector current (I_c); in effect, they represent constant V_{bb} . It is useful to show the results when normalized for constant I_c instead of constant V_{bb} . Figure 4(a) shows results similar to Figure 3(b), but we have used the expressions for $\beta(T)$ and $V_{be}(I_c, T)$ given in [5]. Device parameters (particularly $\theta_{jc} = 600$ C/W, energy gap $E_g = 1.62$ eV, and low-temperature $\beta = 80$) are those of a common 1.6 x 30 μm foundry device and are similar to those of the 2 x 50 μm device described in [5]. With $R_{bb} = 1000\Omega$ and $V_{ce} = 5.0\text{V}$, the figure shows a unique, well conditioned operating point. Figure 4(b) shows the case when R_{bb} is reduced to 300 Ω and V_{bb} is adjusted to provide the same thermal operating point, thus the same I_c . The operating point is now considerably less well conditioned, indicating high sensitivity to thermal resistance, which implies significantly nonuniform currents in cells and difficulty in numerical analysis. Reducing R_{bb} to 200 Ω , Figure 4(c), shows severe ill conditioning, high sensitivity to V_{bb} and θ_{jc} , and, in fact, inability to achieve the desired bias point. Paradoxically, the operating point can be achieved only by making the $V_{bb} < V_{be}$, which prevents turn-on at $\Delta T = 0$. Operation at this bias point would, in fact, require heating the device! Thus, we conclude that, *while base ballast generally provides a stable thermal operating point in HBTs, the use of inadequate resistance can result in ill conditioning as severe as in silicon homojunction devices*. The result is poor thermal stability, nonuniform cell currents, and inability to find the operating point in circuit simulation.



(a)



(b)



(c)

Fig. 4. Calculations of thermal operating point, normalized to 10 mA I_c (~ 20 kA/cm²). Device parameters are given in the text. (a) $R_{bb} = 1000\Omega$; (b) $R_{bb} = 300\Omega$; (c) $R_{bb} = 200\Omega$.

IV. ANALYTICAL IMPLICATIONS

We noted earlier that, in the real circuit, ΔT at turn-on is initially zero and increases until the stable thermal operating point is reached. A circuit simulator, however, starts with an initial estimate of ΔT that may be above or below the operating point. Even if it is below, the iterative solution process may occasionally set ΔT to a value that is closer to the higher, spurious operating point than to the correct one. Then, the solution may converge to the higher-temperature point.

Interestingly, Figure 4(c) shows that it is possible for a circuit simulator to find a nonzero operating point, even if $V_{bb} < V_{be}$. However, in view of the severe ill-conditioning of the problem, it seems more likely that no solution at all will be found.

If a solution is indistinct or nonexistent, a circuit simulator may not be able to find a solution. In a harmonic-balance simulation, this is manifest as nonconvergence of the harmonic-balance process; in time-domain analysis, the simulator is unable to find the dc operating point. When nonconvergence is encountered, the user may have difficulty determining whether it is caused by some limitation of the simulator or by the ill-conditioned nature of the problem itself.

V. CURRENT UNIFORMITY IN BASE-BALLASTED CELLS

Figures 3(b) and 4(a) show that the HBT is inherently thermally stable as long as an appropriate value of R_{bb} is used. Thus, the purpose of ballast is primarily to equalize currents in the individual cells. In any case, equalizing currents is a more severe requirement than simple thermal stability, so the former guarantees the latter.

In any large power device, the cells near the center of the structure are not cooled by conduction as well as the cells near the edge, so they run hotter. In effect, θ_{jc} is larger for the center cells, so C_{tb} is also

larger. Large base-ballast resistance compensates for this difference by reducing the dependence of cell current on V_{be} , and thus its temperature sensitivity. The decrease in β with temperature also helps to equalize cell currents when the ballast resistance is high; this represents a kind of negative thermal feedback.

VI. OTHER EFFECTS OF BASE BALLAST

At this point, it seems that the greatest possible base ballast resistance should be used in HBTs, and perhaps even current-source base biasing should be considered. There are, however, good reasons not to do this. We examine several considerations in this section.

A. Gain Reduction

Base resistance decreases the amplifier's gain, increasing the required size and power of the driver device and decreasing the power-added efficiency of the power stage itself. After all, one of the main reasons for using HBTs is their lower base resistance relative to silicon BJTs. It makes no sense to discard this advantage.

Fortunately, it is usually possible to bypass the ballast resistor at each cell. The inclusion of bypass capacitors increases the chip size, but the use of relatively large individual cells, which reduces the interconnection overhead in the chip, minimizes the size increase. However, if multifinger cells are used, the designer must take care to insure that current-hogging does not occur.

B. Size

A high value of base ballast resistance requires a physically large resistor at each cell, as well as a bypass capacitor. This is a distinct disadvantage when one must minimize the size of the chip to minimize its cost.

C. Changes in Bias With Drive Level

As RF excitation to the power stage increases, the rectified current in the base—the dc base current—also increases. This increases the dc voltage drop across R_{bb} , decreasing V_{be} . Thus, as drive is increased, the dc bias on the base-to-emitter junction drops. This has a number of important effects:

- 1) Saturation of the amplifier gain occurs at lower drive levels and is “harder”; i.e., the difference in input level between 1-dB compression and full saturation is less.
- 2) In Class-A amplifiers, the onset of clipping occurs at lower input power, so distortion, beyond the 1-dB compression point, is worse.
- 3) Similarly, in Class-AB amplifiers, adjusting V_{bb} to provide an optimum value under full drive results in high idling current when drive is removed. In effect, the device must be biased in Class A in quiescent conditions and driven into class AB, or some sort of drive-sensing regulator must be used.
- 4) Envelope frequencies are not bypassed by the ballast-resistor bypass capacitors, so envelope peaks increase the base current, decreasing V_{be} , and causing peak clipping. Distortion in amplifiers intended for signals having high peak-to-average ratios is thus increased. For this reason, base ballast probably should be avoided in CDMA or WCDMA amplifiers.

Of course, many of these problems can be eliminated by the use of a properly designed bias-control chip. However, the problem with high peak-to-average signals is probably not solvable with such a regulator.

D. Stability

HBTs have high low-frequency gain, which can lead to oscillation. The oscillation often occurs at a few tens of MHz and is nonsinusoidal. It usually begins at relatively low current levels as the device is turned on. Operating-frequency oscillation at high bias current is also possible but is relatively easily avoided.

Base ballast can be helpful in preventing low-frequency oscillation. Often a resistor in series with the base is adequate, so the base-ballast resistor can serve this purpose. The bypass capacitor can be selected to bypass the ballast resistor at the operating frequency but not at the expected frequency of oscillation.

In CDMA amplifiers, where base ballast probably should not be used, other means must be found to provide low-frequency stability. Often resistive loading in the bias circuit is sufficient.

E. Low-Frequency Phenomena

Many phenomena in HBT circuits depend strongly on the device's low-frequency terminations. These include the effect of low-frequency noise on oscillator phase noise, memory effects in power amplifiers, intermodulation distortion, and related phenomena such as adjacent-channel interference in cellular systems. Since the ballast method and resistor values affect the device's low-frequency terminations, they also affect these phenomena.

VII. EMITTER BALLAST

Emitter ballast is a bit more complicated. We begin by examining the general case of emitter and base ballast, shown in Figure 5. We assume that β is large (say, greater than 20). We also assume that the bal-

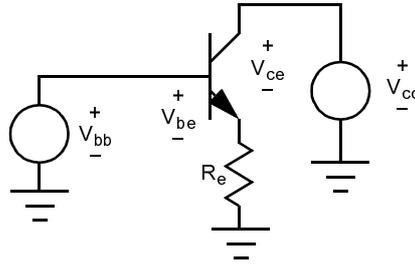


Fig. 5. Emitter ballast.

last resistor, R_e , is located close to the cell, so power dissipated in the ballast resistance heats the cell. Since R_e is invariably an integral part of the cell, its power heats the cell in the same way as collector dissipation.

Our approach is similar to that of the base-ballast case. From a similar derivation, we obtain

$$\begin{aligned} \Delta T &= \frac{\theta_{jc} V_{cc} \beta (T_0 + \Delta T) (V_{bb} - V_{be}(T_0 + \Delta T))}{1 + (\beta(T_0 + \Delta T) + 1) R_e} \\ &\approx \frac{\theta_{jc} V_{cc}}{R_e} (V_{bb} - V_{be}(T_0 + \Delta T)) \\ &= C_{te} f_e(\Delta T) \end{aligned} \quad (8)$$

where C_{te} is the coefficient before the terms in parentheses. The β term is no longer in the equation, showing that, in this case, β does not affect the thermal stability of the device.

Figure 6 shows the plot of $\Delta T'$ using the same device as in Figure 4, but with emitter ballast instead of base ballast. Because V_{be} varies approximately linearly with temperature, the curve is nearly a straight line. The criterion

$$C_{te} \frac{d}{d\Delta T} f_e(\Delta T) < 1.0 \quad (9)$$

must be met not only for stability, but also for a solution to exist. We find that no solution is possible for $R_e < 3.5$, and a well conditioned solution requires $R_e \sim 8$ or greater.

It is worthwhile to consider the effect of high emitter ballast on output power and efficiency. The ballast resistor decreases output power by a factor of approximately $R_L / (R_L + R_e)$, where R_L is the load resistance. For the device used in Figure 6, optimum class-A load resistance, with 3.5V collector bias, is approximately 300 Ω per cell, giving a power reduction of 2.5%. Decrease in power-added efficiency

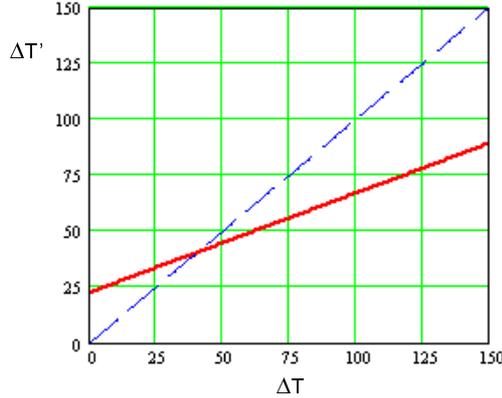


Fig. 6. Plot of $\Delta T'$ for emitter ballast, same device parameters as in Figure 4. $R_e = 8\Omega$.

depends on the ballast resistor's effect on gain, but should be similar. Thus, reasonable values of emitter ballast cause only modest decreases in power and efficiency.

Although emitter ballast is not optimum, as [5] points out, adequate stability still should be obtainable. In any case, emitter ballast avoids the problem of hard saturation and clipping of envelope peaks that exists with base ballast. In particular, it should be used in amplifiers for signals having a high peak-to-average ratio.

Emitter resistance generally has a deleterious effect on stability in HBTs. For this reason, values of emitter resistance above a few ohms per $100\ \mu\text{m}^2$ of emitter area should be used with caution. This situation contrasts that of base ballast, which can improve low-frequency stability. In general, it is not practically possible to bypass emitter resistors with capacitors. Because of the low value of emitter-ballast resistance, the required capacitance would be too great.

It is worth noting that the emitter resistance of an HBT is somewhat temperature sensitive, increasing with temperature. This tends to improve thermal stability as well, although the emitter resistance usually is not great enough to insure thermal stability by itself. External base or emitter ballast is usually necessary.

Values of emitter ballast resistance that provide good thermal stability also provide acceptable levels of cell-current uniformity. The same devices and conditions as in Figures 1 and 4 were used to test current uniformity. (Device internal base and emitter resistances were set to zero, however.) The device showed thermal instability and difficult convergence in the dc analysis with $R_e < 3\Omega$ and $R_{bb} = 0$. Cell currents of parallel devices, again with $R_{bb} = 0$, differed by approximately 20% at $R_e = 3\Omega$ when the thermal resistances were 10% apart. Increasing R_e to 8Ω reduced the difference to 5%. It is worth noting that, even at $R_e = 3\Omega$, no current-hogging was evident.

VIII. WHAT VALUE OF BALLAST RESISTANCE SHOULD BE USED?

This is, of course, the most important question and simultaneously the most difficult to answer. Some generalizations, however, are possible. Our goal in this work is to achieve uniform current in the cells of a power amplifier, and that goal can be met with straightforward simulations using well conceived models. However, often the total collector current is controlled by a feedback system or by other means. It is possible that this may change the ballasting requirements. This possibility has not been considered in this work, but it is a subject for future investigation.

Another important consideration is the effect of ballast on the RF performance of the amplifier. Specifically, if the dc-to-RF efficiency is high, less power is dissipated in the device, and less ballast is needed. Conversely, poorer efficiency requires higher ballast. In the foregoing, we have made the most conservative assumption, that the full dc power is dissipated in the device. While this assumption may seem to conservative, most power devices must, under some conditions, survive full dc bias without RF drive. Thus, dc stability and cell-current uniformity represent a reasonable, conservative criterion for design.

The results shown above indicate that the usual cell size employed in wireless and cellular handset power amplifiers requires base ballast on the order of 500-1000 ohms. Emitter ballast should be at least 8

ohms for good stability in a typical cell of $50 \mu\text{m}^2$ emitter area. These values can be scaled for larger or smaller cells.

In this work, we did not examine the possibility of combined emitter and base ballast. It is possible that the use of some base ballast in conjunction with emitter ballast may result in more uniform cell currents with minimal emitter ballast and base ballast resistance values low enough to avoid its drawbacks. This possibility also is a subject for continuing investigation.

IX. CONCLUSIONS

We have shown that, while base ballast provides high thermal stability and cell-current uniformity, it has deleterious effects on many aspects of RF amplifier performance. At the same time, emitter ballast, which initially appears inferior, avoids many of those disadvantages, and can provide stability if adequate values of emitter resistance are used. The choice of a ballasting method should therefore be based on the effects on RF performance with values of ballast that provide adequate thermal stability and cell-current uniformity. In particular, it should not be based on a perceived inherent advantage of one method.

X. ACKNOWLEDGEMENTS

This work was supported by the Science Foundation, Ireland while the author was a Walton Fellow at University College, Dublin. The author also wishes to acknowledge the support of RF Integrated Corporation and helpful discussions with the staff.

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