"MOSFETs with vertical and horizontal channels – potential advantages for RF"

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Abstract

This paper will address some methods of manufacturing high performance but low cost transistors and integrated circuits (ICs). The paper will focus on RF-CMOS ICs.

Conventional Transistor and IC fabrication is heavily dependent on very many sequential precision manufacturing steps which consequentially lead to long manufacturing cycle times. Additionally equipment and infrastructure costs make IC manufacture very expensive.

New ICs are developed from original circuit designs. From the circuit design to a working product requires a number of iterative manufacture steps during which prototype circuits are manufactured and tested. Failure of a prototype followed by identification of the failure mode leads to an improved circuit design and the requirement for the manufacture of further prototypes. This whole reiterative process for prototype manufacture can frequently take more than one year, which can make the original design out dated. Methods will be discussed which drastically decrease this fabrication time, and thus cost, particularly for prototype production.

Introduction

In order to extend CMOS scaling to its physical limits while maintaining performance improvements, devices with structure different from the single gate MOSFET will have to be introduced. One of the most promising concepts in this direction are double and surround gate MOSFETs (Figure 1), which can be grouped in three classes:

- Planar Double Gate and Gate All Around (GAA) MOSFETs. In planar double gate devices both the current-carrying plane and the current flow are parallel to the wafer surface. In GAA MOSFETs the current can flow on planes perpendicular to the wafer surface as well.
- FinFETs. In these devices the current-carrying plane is perpendicular and the current flow parallel to the wafer surface.
- Double and Surround Gate Vertical MOSFETs. In these devices both the current-carrying planes and the current flow are perpendicular to the wafer surface.

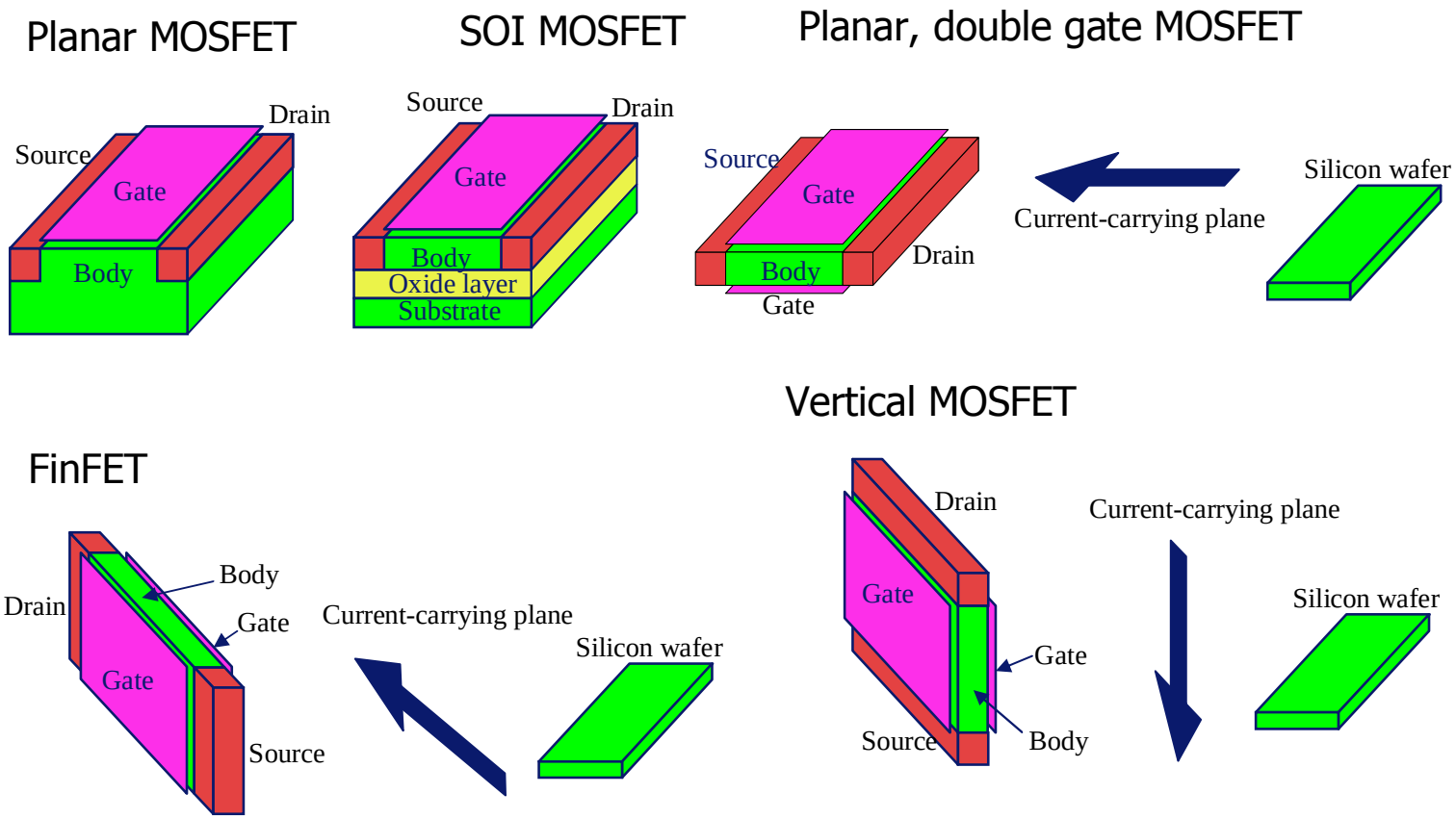
Both planar double gate and GAA MOSFETs in general require a very complex fabrication process. This fact limits their integration in a standard CMOS process. In particular, the realisation of planar double gate MOSFETs is difficult because, to obtain good performance, top and bottom gates must be aligned. As for FinFET, its main advantage consists in its high CMOS compatibility. This device

requires SOI substrates that are increasingly being used. One drawback is that a very thin fin needs to be etched, thus involving advanced lithographic techniques.

Surround gate vertical MOS transistors built on the sidewalls of vertical pillars have been developed for four main reasons:

- the gate length is controlled by non-lithographic methods; this allows the realisation of shorter channel lengths without using advanced photolithography and thus allows sub-100 nm vertical MOSFETs to be integrated in a mature CMOS technology with relaxed lithography rules (Figure 2);
- surround gate or double gate structures allow more channel width per unit of silicon area; this leads to an increase of the drive current per unit area (Figure 3);
- the better control of the substrate depletion region in thin, fully depleted pillars reduces the short channel effects and improves channel mobility;
- the gate length is decoupled from the packing density; for RAM applications, long channel transistors (with lower off currents) can be produced without decreasing the number of devices per unit area.

Fig 1. Single and double gate MOSFETs



Advantages of vertical MOSFETs

- The gate length is controlled by non-lithographic methods; this allows the fabrication of sub-100nm channel length devices with relaxed photolithography rules, reducing costs.
- Surround gate or double gate structures allow more channel width per unit of silicon area; this leads to an increase of the drive current per unit area.
- Better control of the substrates depletion region in thin, fully depleted pillars reduces the short channel effects and the parasitic capacitances.

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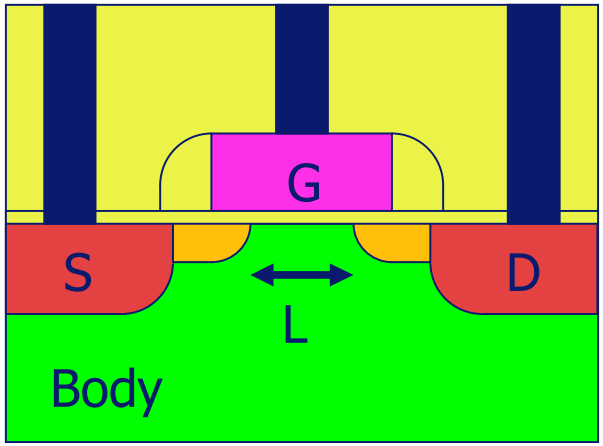
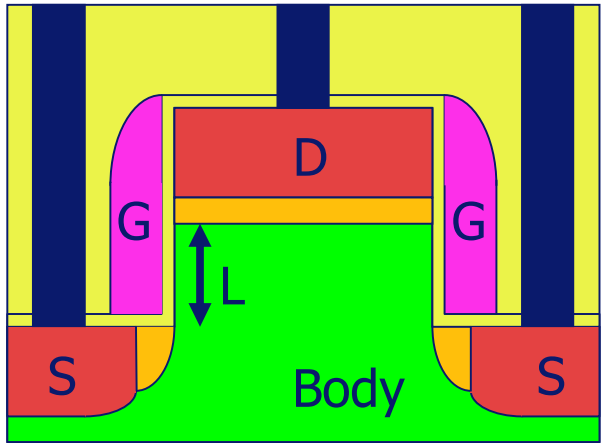
Fig 2. Short Channel Length Devices

- Planar MOSFET: the minimum channel length (L) depends on the minimum feature length achievable with photolithography

- Vertical MOSFET: the minimum channel length is controlled by non-lithographic methods (ion implantation or expitaxial growth)





S = Source
D = Drain
G = Gate

p-doped silicon

n+-doped silicon

SiO_2

n-doped silicon

n+-doped polysilicon

Metal

Fig 3. Increased drive current per unit of silicon area

Device integration:
The double gate or surround gate
Layouts allow to obtain:

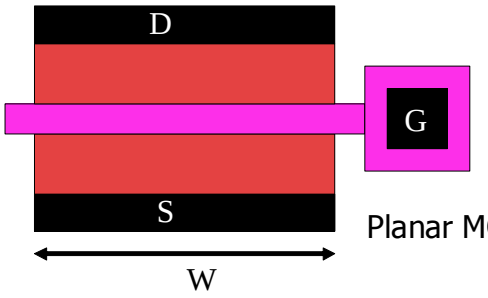
- More channel with (W) per unit of silicon area;
- More drive current per unit of silicon area

S = Source
D = Drain
G = Gate

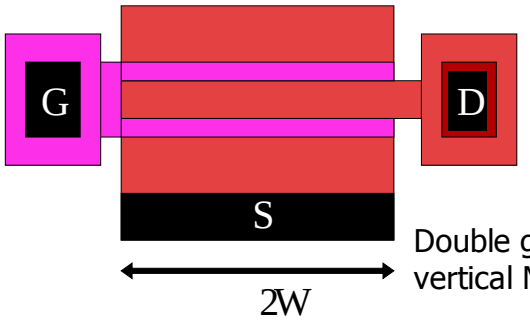
Metal

n+-doped silicon

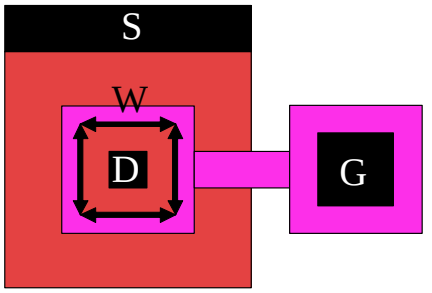
n+-doped polysilicon



Planar MOSFET

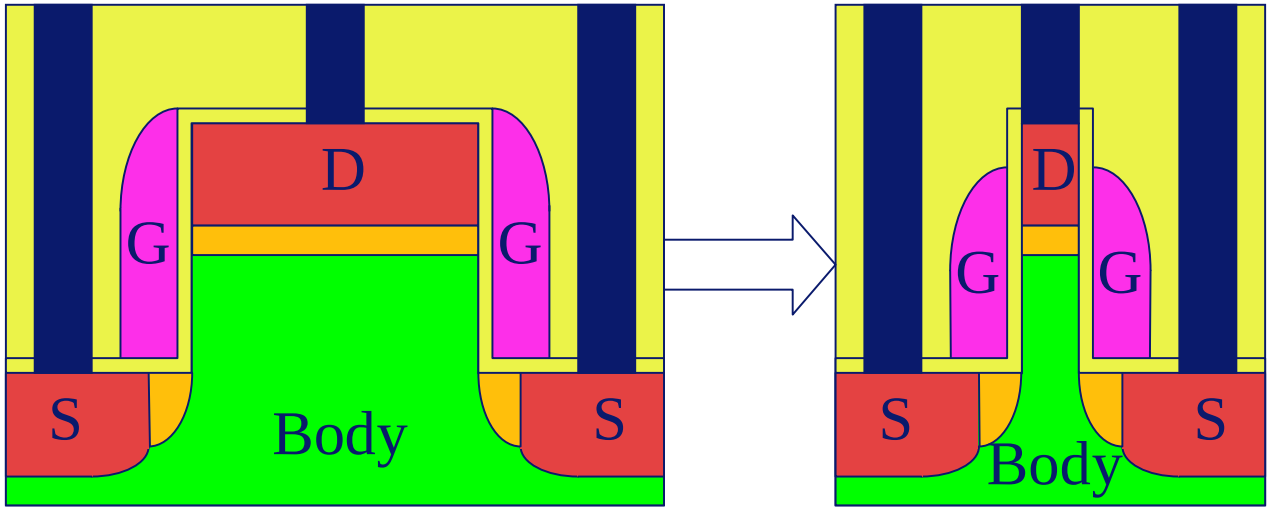


Double gate
vertical MOSFET



Surround gate
vertical MOSFET

Thin pillar, fully depleted vertical MOSFETs



- Physical reason: the coupled effect of the gates allows better control of the body depletion region
- If the body is thin enough (30-50nm wide), it is fully depleted, as in an SOI device
- The body doping concentration an be reduced without degrading the short channel effects and this allows:
    - Subthreshold slope reduction
    - Channel mobility increase

Conclusions:

RF Advantages

- Sub-100nm channel length – GHz transistors - length easily controlled.
- More (RF) drive current per unit area of silicon.
- Reduced short channel effects – linear behaviour.