A very high efficiency high power Schottky diode frequency doubler operating at 180-190 GHz

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***Abstract*—This paper presents simulation and test results for a fixed-tuned ultra-high efficiency high power Schottky diode 180-190 GHz frequency doubler. The doubler was designed for an input power of 100-200 mW and tested producing flange-to-flange peak efficiency greater than 40% and output power greater than 70 mW in 185-195 GHz band. The 3 dB bandwidth was measured at more than 13%. In terms of output power and total efficiency these results exceed the current state of the art at the given frequency and input power.**

***Index Terms*—Schottky diodes, high power, doubler, high efficiency.**

I. INTRODUCTION

There is a significant demand for high power high frequency signal sources in millimeter-wave and submillimeter wave applications. Schottky varactor diodes are still preferred choice devices when it comes to low order mutlipliers (doublers and triplers) that are to be employed in local oscillators in heterodyne receivers/radiometers for remote sensing, imaging, atmospheric physics, test instrumentation and radar systems at very high frequencies (>110 GHz). High power and high efficiency frequency doublers are frequently employed in higher order multiplier chains, where low order multipliers are cascaded together with microwave local oscillator to form a sub-millimeter wave frequency source. The output power of such sources, in most cases, is sufficiently high to drive subharmonic mixers in sub-millimetre receiver systems. When considered on their own, such source/multiplier chains can be used as signal sources for test and measurement or communication applications. The high power high efficiency doublers also facilitate radar solutions for applications above 100 GHz, for which up until now there were no means of generating sufficient power levels in a cost effective way. These radar systems could fulfill market needs for safety and security focused applications such as: foreign object detection, perimeter detection, traffic monitoring, collision avoidance, aircraft landing systems, security imaging and many others. High order multiplier chains rely on solid state MMIC devices for early stage multiplication and power generation. The recent advent of high power GaN technology allows for relatively simple realization of amplifiers operating up to 110 GHz that can be used as drivers for these efficient Schottky multipliers, allowing to achieve very compact and cost effective high frequency multiplier chains.

For many years the attraction of various industry and academia organizations towards high power generating devices has been very high. Large number of these organisations have been heavily involved in development of high power and high efficiency Schottky devices and multipliers. Their prime interest has been in low order multipliers such as doublers and triplers. The triplers are deemed particularly useful as final stage multipliers for applications were the final frequency leap to the desired frequency is required. In such case a solid state electronics is used to provide pumping power in lower end of mm-wave spectrum (<100 GHz) to the tripler that allows for reaching 300 GHz range. In those cases however where a much higher frequency signals must be produced additional stage of a single or chained multipliers must be used. It is predominantly in these applications where the high efficiency and power of Schottky doublers are used best to produce compact and efficient multiplied frequency sources. Such devices offer sufficient efficiency and output power for driving the last stage triplers or operate as a LO sub-system for sub-terahertz subharmonic receivers. Advanced design techniques and powerful 3-D and system design tools allow for very accurate and efficient modelling and synthesis of Schottky multipliers. These design tools allow for taking into account all physical and electrical properties of all circuit components, their analysis and optimization. With high precision machining and accurate printed circuit techniques a physical realization of multipliers based on discrete Schottky devices yields very repeatable results, the components are mechanically robust and relatively easy to assemble.

The device presented here is based on a circuit topology presented originally by Erickson [1], [2] and further modified by Porterfield [3], [4]. In this configuration the Schottky diodes are placed in anti-series configuration at the junction between the balanced and unbalanced sections of the circuit. In such arrangement the diodes respond only to odd harmonics at the input and even harmonics at the output. The EM mode orthogonality ensures very good input and output signal isolation without the need for additional filtering elements, their additional complexity and impact on the conversion efficiency. An E-plane split block metalwork design and photolithographic techniques are used to produce circuit interfaces, cavity and matching networks.

II. Design

The circuit relies on the inherent mode and frequency isolation between the input and output port. The incident wave is coupled onto the varactors in a balanced TE_{10} mode and must not be allowed to propagate into the circuit channel. This is achieved by creating the effective input frequency backshort and narrowing down the circuit channel width. The output frequency is generated by the varactors in a TEM mode and is free to propagate down the circuit channel, onto the output transition and into the output WR-05 waveguide. It must be noted that without reducing the height of the input waveguide the diodes would produce the output signal also in other field modes - namely TM_{11}. The reduced height input waveguide section and the input backshort position are the elements responsible for input matching and spurious mode suppression, while the on-substrate microstrip sections and output transition ensure good power transfer to the output waveguide. The doubler circuit from a conceptual point of view is shown in Fig. 1.

Due to their high frequency and high power operation the Schottky doubler circuits call for advanced modelling techniques to ensure their efficient operation and ability to interface with other devices in the cascaded chain without significant miss-matching issues. Extensive electromagnetic modeling with High Frequency Software Simulator (HFSS) from Ansys was used for passive circuit analysis. The whole doubler circuit was separated into sections for waveguide cavities, Schottky diodes and substrates. The simulation results were extracted and used as input files to a harmonic balance analysis in Advanced Design System (ADS) from Keysight to determine optimum diode matching at all the relevant frequency points and allowed for simulating the doubler circuit as a whole with its non-linear as well as linear effects.

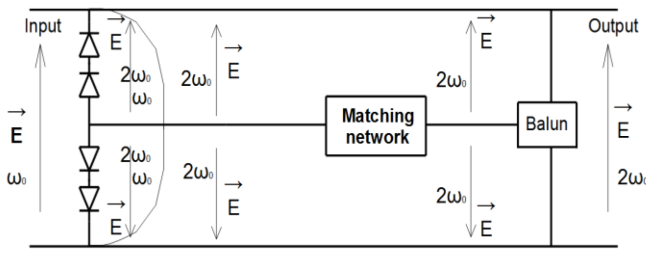

Fig. 1. Doubler circuit - diagram.

The HFSS model of input circuit containing the varactor diodes and waveguide-suspended stripline interface is shown in Fig. 2:

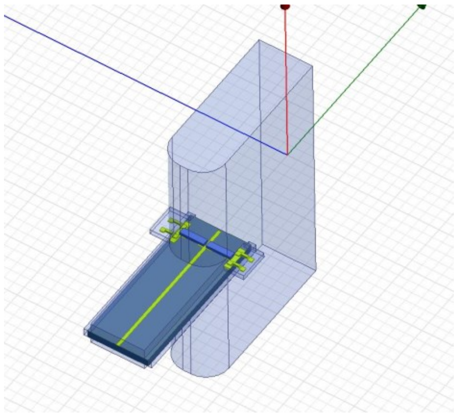

Fig. 2. HFSS model of input circuit.

III. Simulations and Measurements

A comparison of the simulated and measured performance of the complete doubler driven with 200 mW of input power is shown in Fig. 3 and Fig. 4:

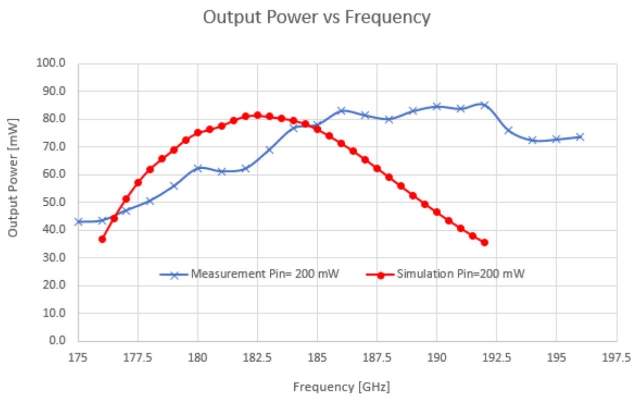

Fig. 3. Predicted and measured output power vs output frequency.

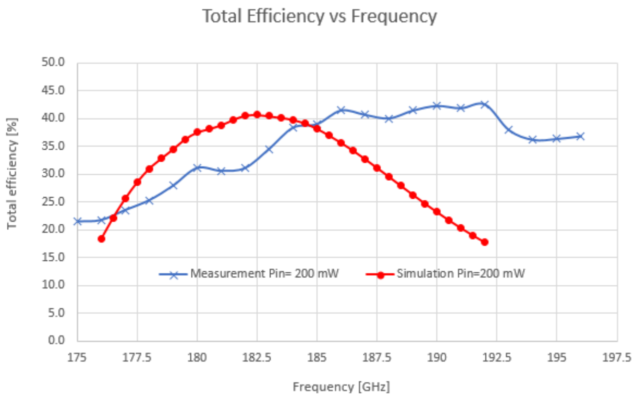

Fig. 4. Predicted and measured total efficiency vs output frequency.

The initial measurements were performed using Farran Technology's own multiplier/amplifier chain in a setup shown schematically in Fig. 5:

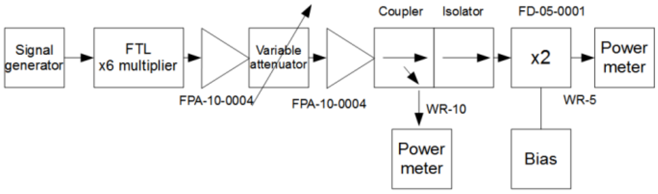

Fig. 5. Output power measurement setup.

The RF signal was provided by a signal generator feeding o the active x6 multiplier/amplifier chain. The incident power to the doubler was controlled by a variable attenuator positioned between two GaN 88-96 GHz power amplifiers. The power level was continuously monitored and controlled at every frequency point. The full set of results for output power and flange-to-flange efficiency for 5 different input power levels is shown in Fig. 6 and Fig. 7, respectively. The calculated error in the input power measurement was ± 0.4 dB which contributes to a maximum total efficiency error of ± 3%. Output power measurement accuracy was ± 0.1 mW. The test results were corrected by 0.25 dB for the WR-05-to-WR-10 transition in front of the calorimeter sensor. The bias voltage ranging from -7 to -13V was adjusted at each frequency point at each input power level to achieve optimum total efficiency and output power.

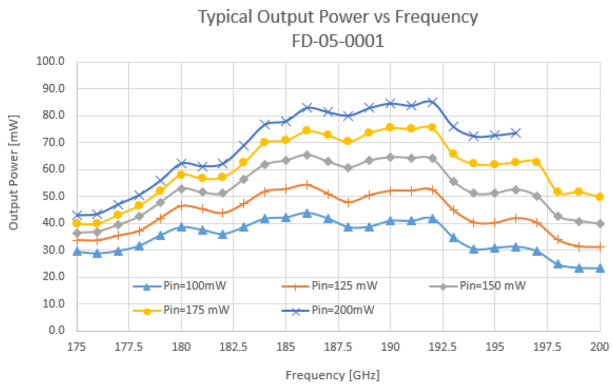

Fig. 6. Measured output power at various input power levels.

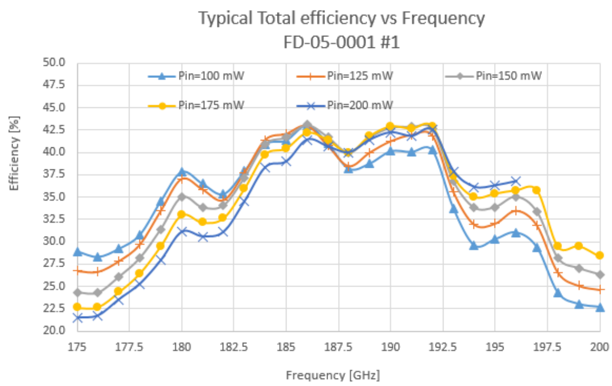

Fig. 7. Measured total efficiency at various input power levels.

Overall three devices of the same type have been built and characterized. All three exceeded 40 % of peak efficiency. Their results were within a 3% window between all units.

There is a significant shift in frequency for which the doubler achieves its optimum performance. The peak power and efficiency are achieved 7 GHz higher in the spectrum than expected. The reason for this effect is not fully understood as it is most likely an effect of electrical accuracy in the input matching network as well as estimated values for junction and parasitic capacitance. At the time of submitting this work no viable reasons and results were available to the authors to present. The investigation will continue in an effort to understand better the reason for the discrepancy.

The fully assembled device is shown in Fig. 8.

Fig. 8. Assembled doubler.

It worth noting that the doubler achieves efficiency greater than 40% at from 185-192.5 GHz. More importantly however it achieves very broad range of 20 GHz where the conversion efficiency is greater than 30%. At the maximum drive level of 200 mW it produces output power exceeding 70 mW over 10 GHz of bandwidth with a peak of 85 mW at 192 GHz. A comparison of published results and results measured in this work is given in Table I:

TABLE I. PERFORMANCE COMPARISON

Ref	Frequency [GHz]	Input Power [mW]	Output Power [mW]	Total Efficiency [%]	Obtained results:
[2]	174	200	48	24	Measured
[4]	200	200	36	18	Measured
[5]	188	200	55	27.5	Measured
[6]	188	80	7.2	9	Measured
[7]	190	200	52	26	Simulated
This work	192	200	85	42.5	Measured

As it can be seen from the above table the results achieved by the doubler presented here significantly exceed those presented in [2], [4]-[7].

IV. Conclusion

A high power high efficiency frequency doubler has been designed and tested. Its performance with very high conversion efficiency makes it an ideal candidate for high frequency multiplier chains and for integration in safety and security radar front-ends. Its optimum input power level range of 100-200 mW combined with high efficiency ensures that it can be driven by very compact and relatively inexpensive solid state amplifiers making it more cost effective as well as easier to handle from a thermal management point of view.

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