APPLICATIONS OF WAVEFORM ENGINEERING FOR ANALYSING NEW DEVICE TECHNOLOGIES

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Abstract

With increasing system demands calling for higher performance RF components there is a continual push towards new material systems and device topologies. As each new technology evolves new challenges are presented that must be faced in order to fabricate successful products. Most recently, GaN HFETs (Heterojunction Field Effect Transistors) have been in development as an enabler for solid state RF power amplifier (PA) applications at higher frequencies and power levels than afforded by incumbent technologies. In the course of the development of these devices, RF waveform measurement and active load-pull have been utilized at Cardiff University and QinetiQ Ltd. to explore device performance limitations and to help analyse and model the physically underlying mechanisms. This paper presents an overview of this effort, demonstrating how advanced RF measurements can help device technologists and circuit designers alike maximise the performance of developing technologies.

Introduction

GaN HFETs have received a large amount of interest for RF PA applications due to their potential for simultaneous high power and high frequency operation. However, during early device development the performance has not consistently matched this potential. Many groups worldwide have been investigating why RF output power levels are not as high as predicted from basic DC measurements and why device performance alters over time. Common tools used for quantifying problems with RF PA performance include DC measurements, pulsed-IV measurements, small signal RF measurements and power or large signal RF measurements which are often made under varying impedance conditions (load pull).

It is also possible to capture RF time domain waveforms which provide direct information on the RF behaviour of the device under operating conditions representative of final circuit applications. Here results are presented from a program of interaction between QinetiQ and Cardiff University aimed at monitoring and improving RF performance of GaN HFETs through analysis of RF waveform measurements. The measurement system used in this work has been developed at Cardiff University and is

based upon sub-sampling a time repetitive RF signal to allow the calibrated measurement of RF terminal voltage and current waveforms [1]. The device-under-test (DUT) can also be presented with a range of load impedances using active load pull loops for a number of harmonics, resulting in an extremely versatile characterisation setup.

This paper presents a number of example RF waveform measurements which demonstrate the value of this technique when looking at device level issues. As a conclusion the measurement system's application for design is also demonstrated with a high efficiency class F tuning experiment.

Basic waveform analysis of GaN HFET performance

Figure 1 shows the output voltage and current waveforms of a 200µm periphery GaN device measured on-wafer at 900MHz. It is possible to see that the output voltage waveform is approximately sinusoidal but the output current waveform is strongly compressed as the RF signal interacts with the device boundary conditions. This is typical of overdriven PA operating modes, which are the modes of operation that should deliver maximum output power for a given device.

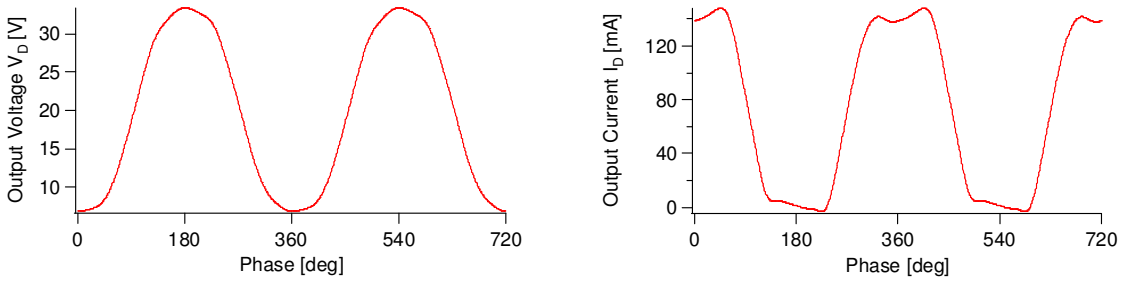

Figure 1 – Output RF voltage and current waveforms for a 200µm GaN device driven into strong compression. Measurements made on-wafer at f_0 = 900Mhz with class A bias conditions at V_D = 20V.

These waveforms can be analysed in relation to the device boundary conditions by plotting the output current vs. the output voltage as a dynamic load-line and overlaying this load-line on the device DC-IVs. Such a plot is shown in Figure 2 for the same measurement shown in Figure 1. This figure demonstrates why the maximum achieved RF output power is lower than expected given the device DC-IVs. The measured waveforms highlight the premature compression of the RF current swing compared to the DC limits as the load-line tries to move into the knee region. This phenomena has been called "knee-walkout," "DC-RF dispersion" and "current collapse" in the literature and can be observed and tracked very effectively using measured RF waveforms.

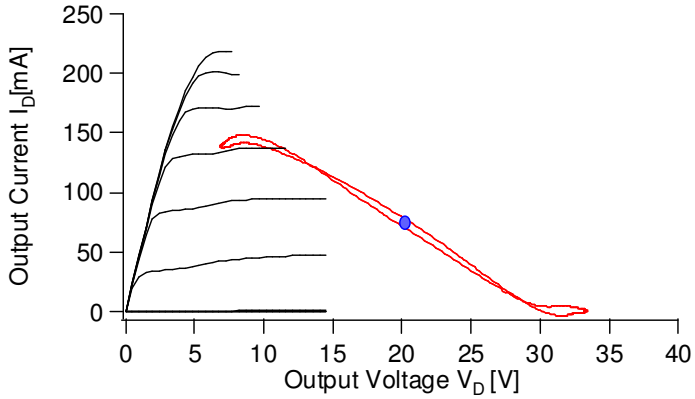

Figure 2 – Dynamic load-line measured for a 200µm GaN device driven into strong compression. Measurements made on-wafer at f_0 = 900Mhz with class A bias conditions at V_D = 20V.

Detailed load-line analysis

By measuring suitably compressed load-lines for a range of fundamental load impedances it is possible to trace the boundary regions of an RF power device that limit output power and efficiency in most typical applications [2]. This can be useful when diagnosing device level issues. Figure 3 shows a range of dynamic load-lines measured at a range of fundamental load impedances and at four different drain biases (10V, 20V, 30V and 40V) for two different devices. This level of detail allows analysis of the RF boundary conditions over the entire IV plane for an operating PA.

Short channel effects

It is possible to see that device (a) is not pinching off sufficiently resulting in the dynamic load-lines rising up at high drain voltages. This is believed to be caused by a parasitic current flow under the main channel which reduces output power and efficiency and is extremely undesirable for PA applications. The root cause of this behaviour is due to the geometry of the device depletion region being overcome by high voltages on the drain terminal. The pinch-off problems can be controlled by doping the buffer region of the device to reduce leakage and effectively create a back-gating effect – the result of which can be seen in device (b).

Dispersive effects at the knee

GaN HFETs are known to suffer from strong dispersive effects linked mainly to the sensitivity of the structure to surface defects and also due to the developing quality of the bulk semiconductor material. Both devices in Figure 3 show signs of strong dispersion. The current collapse is a function of the DC drain bias. It can be seen that increasing the drain bias results in increasing amounts of dispersion. Time domain waveform measurements provide a useful way to examine dispersive effects.

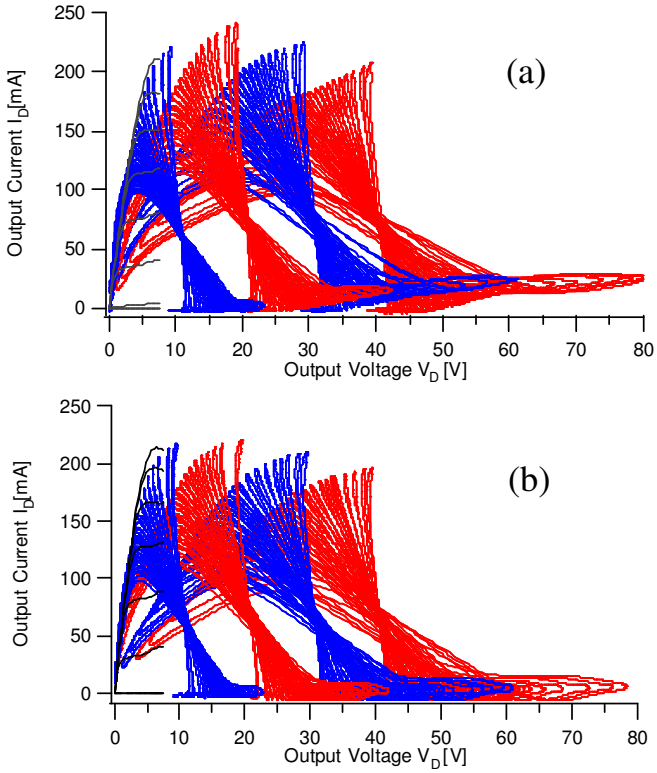

Figure 3 – Dynamic load-lines measured for a 200µm GaN device driven into strong compression for a range of drain biases and fundamental load impedances. It is possible to see that device (a) is suffering from short channel effects as well as knee walkout whilst device (b) has negligible short channel effects.

Degradation Tracking

Another device issue which can be analysed using RF waveforms is the degradation of device performance over time. The majority of semiconductor devices experience a rapid "burn-in" period where their performance changes rapidly during a short initial period of multiple hours. This is commonly followed by a much slower change over the course of the component's lifetime - often multiple years of use. Investigations of reliability in RF transistors employ a fairly standard characterisation procedure whereby RF output power reduction, gain reduction, DC bias drift and leakage levels are measured before, during and after various RF and DC stress tests. Elevated temperatures may also be employed to facilitate accelerated life testing, where added thermal energy speeds up the degradation processes in order to condense the duration of test needed to demonstrate a given product lifetime.

Measuring the RF waveforms of GaN HFETs over time can help in understanding these processes by providing additional information unavailable in standard measurement techniques. As an example experiment, a batch of 2x100µm GaN HFET devices with rapid degradation issues were characterised for standard degradation measures whilst simultaneously collecting measured waveforms. The transistors were biased in a Class A configuration at a drain voltage of 20V and stressed using a 1.8GHz CW signal. The devices were driven approximately 3dB into gain compression with a fundamental load

tuned for optimum output power (R_L = 140Ω at f_0) with all higher harmonics terminated into 50Ω. Each device was then stressed for a period of 1.5 hours whilst the input and output current and voltage waveforms were periodically sampled 100 times, resulting in a measurement similar to an RF "burn in" test, but with the addition of waveform data. The standard RF and DC results from one such test are shown in Figures 4 and 5 respectively. It can be seen that output power is rapidly decreasing, whilst quiescent drain current is dropping and gate leakage is increasing.

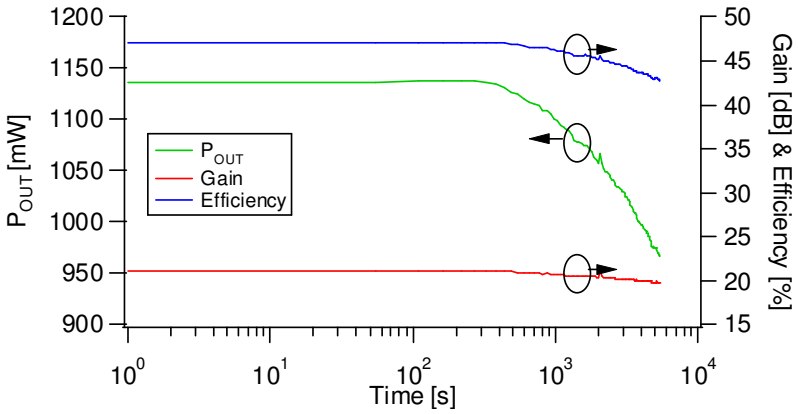

Figure 4 – Standard RF measures of degradation for a 1.5hour burn-in period measured for Class A bias at V_D = 20Vusing 1.8GHz CW.

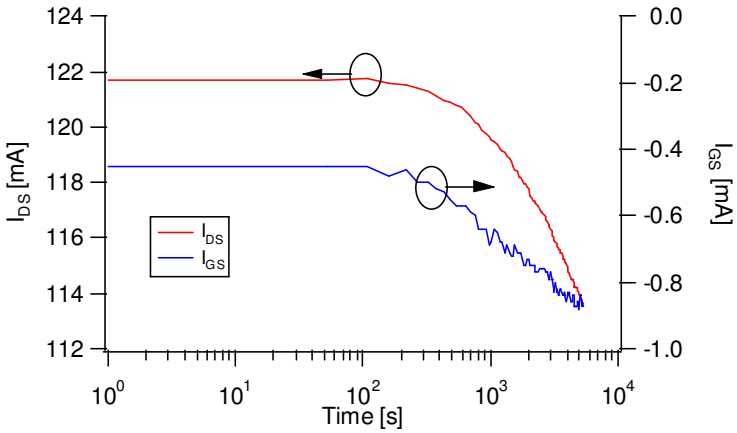

Figure 5 – Standard DC measures of degradation for a 1.5hour burn-in period measured for Class A bias at V_D = 20Vusing 1.8GHz CW.

These standard results can be enhanced by analyzing the simultaneously measured RF waveforms, sampled periodically over the stress period. It can be seen in the load-lines of Figure 6 that the level of localized dispersion at the knee region has changed during the stress period, since the difference between initial load-line and initial DC knee is smaller than the post stress difference. Looking at the dynamic transfer characteristics shown in Figure 7 (output RF current vs. input RF voltage) can highlight other interesting observations. For instance it can be seen that the reduced current is mainly occurring

whilst the gate voltage is swinging to values above -3V. Additionally there is a lack of degradation occurring around the threshold voltage ($V_T \approx$ -6V), suggesting that the semiconductor material directly under the gate is not changing during the stress period [3].

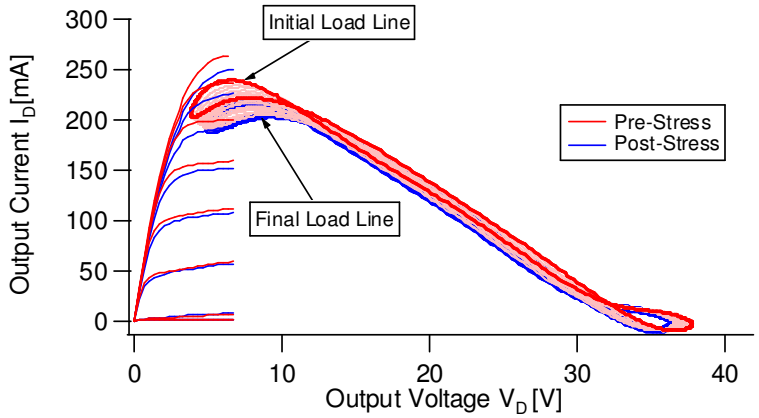

Figure 6 – Dynamic load-lines measured periodically during 1.5 hour stress period and DC-IVs measured before and after stressing (V_G =0V to -8V in 1V steps)

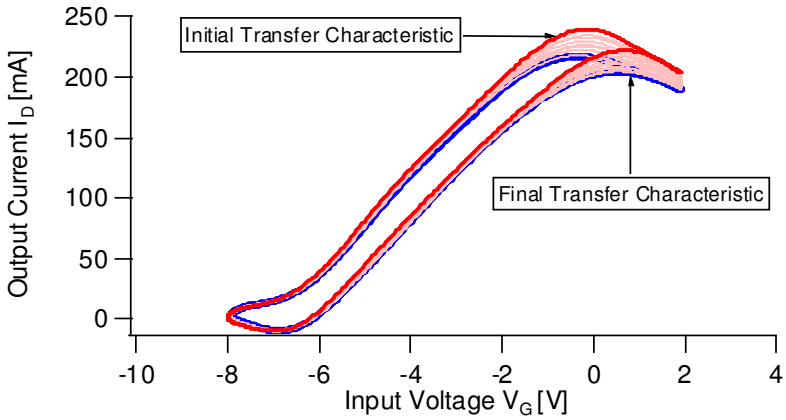

Figure 7 – Dynamic transfer characteristics measured periodically during 1.5 hour stress period

Application to Design

As technologies develop and mature it is often necessary to utilize the components in systems before all device issues have been fully resolved. Successful designs using developing technologies must take into account non-optimal characteristics of the devices involved, and can therefore benefit from advanced characterization. The class F mode of PA operation is desirable for its simultaneously high output power and efficiency and is achieved by engineering the output voltage and current waveforms to specific shapes (square wave voltage and half rectified current). A class F design is greatly benefited if the designer has access to measured waveforms and is able to manipulate circuit

parameters such as bias and impedance environment whilst observing the effect on the device waveforms and associated RF performance.

A class F GaN implementation must avoid operating in regions where the performance will be reduced by non-ideal features of the device technology, such as knee walk-out at high current densities. A fundamental load-pull sweep can reveal the trade-off between power density and drain efficiency as a function of effective current density [4]. The results of a simulation are plotted in Figure 8. This graph allows the designer to select an effective working current density by altering the fundamental match to balance output power and efficiency for a specific class F condition.

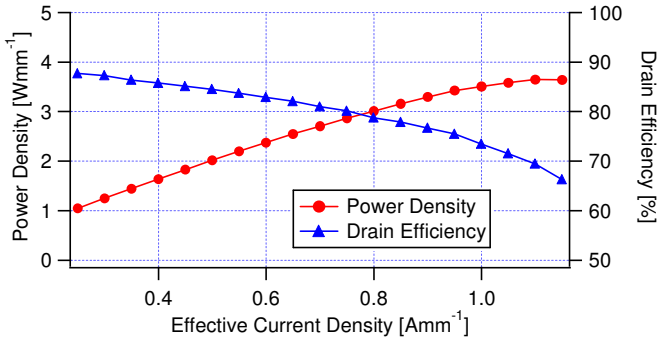

Figure 8 –Predicted maximum achievable power density and drain efficiency as a function of the effective current density for the 15V drain bias condition.

Based on the predicted performance of Figure 8 it was possible to emulate a three harmonic class F matching network using active load-pull loops at each harmonic frequency to achieve 3W/mm and 80% efficiency. The predicted trade-off point could be achieved by careful optimisation. The resulting output waveforms and dynamic load-line are shown in Figures 9 and 10 respectively.

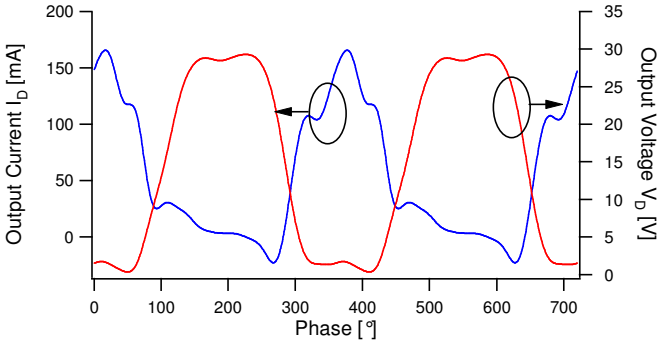

Figure 9 –Measured RF current and voltage waveforms for class F operation of a GaN device.

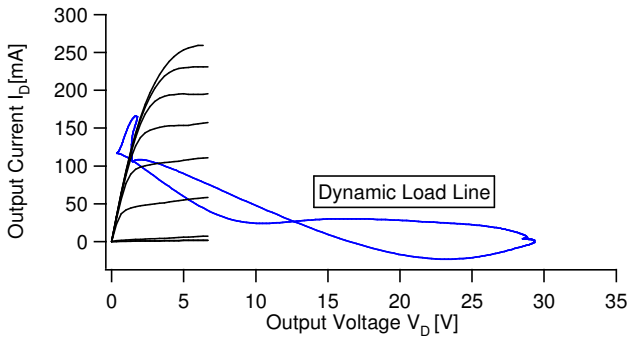

Figure 10 – RF dynamic load-line for same class F case, overlaid on the device DC-IV.

Conclusions

It has been shown that waveform measurements and engineering can be a useful tool for analysing developing technologies as well as moving these technologies into initial designs. Early problems with GaN HFETs such as short channel effects and current-collapse have been observed. In addition device reliability can be monitored by measuring waveforms of an active device over time. As devices near commercialisation prototype designs can be expedited by using measured waveforms, demonstrated here by a class F tuning experiment.

References

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[2] C. Roff, P. McGovern, J. Benedikt, P.J. Tasker, R.S. Balmer, D.J. Wallis, K.P. Hilton, J.O. Maclean, D.G. Hayes, M.J. Uren & T. Martin, "Detailed Analysis of DC-RF Dispersion in AlGan/GaN HFETs using Waveform Measurements," *Proceedings of the 1st European Microwave Integrated Circuits Conference, Sept. 2006, Manchester, U.K., Pages 43-45.*

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