Analysis of the VSWR Withstand Capability of a Balanced Amplifier

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***Abstract*—An analytic calculation is made of the VSWR withstand capability of a balanced amplifier and the results are verified by computer simulation. It is shown that in the presence of a mismatch at the output that one transistor in the balanced amplifier sees an improved VSWR whereas the other sees a larger mismatch and a very simple equation is derived that enables the VSWR that the transistors see to be calculated The paper highlights deficiencies in previous works addressing this topic.**

***Index Terms*—Power amplifiers, Balanced Amplifiers, RF & Microwave Amplifiers, GaN**

I. Introduction

One of the key parameters in an RF or microwave transistor's data sheet is the VSWR mismatch that the transistor can withstand without failing. A typical value for an LDMOS transistor is 20:1, but some LDMOS devices can withstand a VSWR mismatch as large as 65:1 [1]. The failure mechanism is always excess thermal dissipation. GaN transistors, however, have a much higher thermal resistance per RF Watt than LDMOS and so a typical VSWR withstand value for a GaN high-power transistor is 5:1 with many very high power GaN transistors having a value as low as 3:1. High power amplifiers require multiple transistors to be combined and the designer can use either in-phase combining with Wilkinson or Gysel combiners, anti-phase combining (push-pull) with baluns, or quadrature combining (balanced amplifier) with quadrature couplers. A key decision in the choice of which combiner structure to use is which topology offers the best VSWR withstand capability, particularly for GaN amplifiers. It is readily shown that in-phase combining provides the same VSWR withstand capability as the transistors have. The ideal push-pull amplifier uses a pair of center-tapped transformers but these cannot be realized at microwave frequencies and so baluns are used instead. However, a balun does not have the same circuit properties or *S* parameters as a center-tapped transformer, and there are numerous different balun types such as Guanella, rat-race coupler, Wilkinson coupler with a 180^0 phase shifter in one arm etc, all of which have different circuit properties and *S* parameters to each other. It is beyond the scope of this paper to consider all the various different baluns with respect to VSWR withstand and so instead this paper will focus exclusively on balanced amplifiers.

Balanced amplifiers have many advantages and their properties are well known [2]. One of their key advantages is that a balanced amplifier provides an excellent VSWR at its external terminals even if the two internal amplifiers have very poor terminal VSWR. This paper is concerned with the converse problem, namely what VSWR do the two internal amplifiers see when a mismatch is present at the external port. This problem has previously been considered by Walker [3] and, more recently, by Jung *et al* [4], but both these analyses have serious deficiencies. Walker assumed that the each of the internal amplifiers presented a perfect match to the coupler; this is invariably untrue and so his analysis is of limited value. Jung *et al* calculated the value of the physical load that each internal amplifier sees and not the value of the electronic load and so their analysis is invalid. The significance of the problem is illustrated in Figure 1. Each current generator sees a physical load of 1Ω but the voltage across the resistor is 2V and hence each current generator sees an electronic load of 2Ω rather than 1Ω. In the case of the balanced amplifier shown in Figure 2, it is essential to calculate the load seen by each amplifier while both current generators are simultaneously injecting current into the coupler i.e. the electronic load.

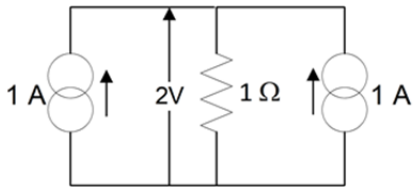

Figure 1. Illustration of the difference between physical load and electronic load.

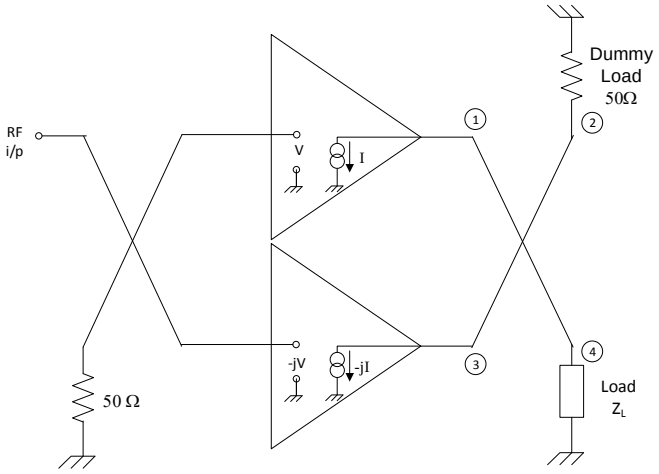

Figure 2. Balanced Amplifier Schematic.

This paper will first outline how VSWR withstand capability is defined and measured, and then a valid analytic calculation of the electronic load seen by each internal amplifier will be presented. The results will be shown to be in complete agreement with computer simulation.

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II. VSWR Withstand capability Definition and measurement

The traditional method of measuring VSWR withstand capability is to insert a transistor into a test fixture and adjust the RF input power until the RF output power reaches its full rated value. The load is then removed and replaced with an attenuator terminated in a short-circuit and proceeded by a trombone line stretcher as shown in Figure 3. The line stretcher is adjusted such that the phase of the load is swept through 360^0. The value of attenuation is then reduced in stages and the process repeated until the transistor fails. Strictly speaking, this method measures the VSWR withstand capability of the transistor embedded in its test fixture, but provided the test fixture does not have any intentional attenuation in the RF output matching network then this method measures the VSWR withstand capability of the transistor. The VSWR withstand capability is quoted with reference to a 50Ω load and not the load impedance that the transistor sees.

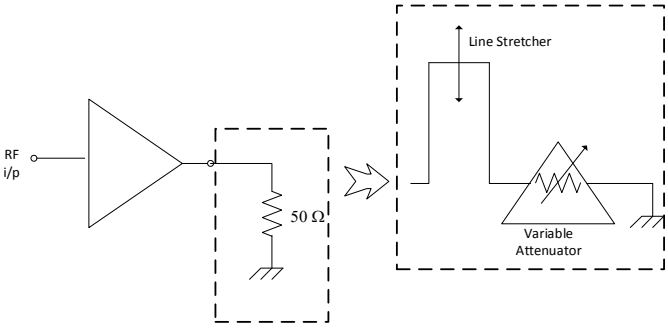

Figure 3. Measurement of VSWR Withstand Capability Set-up.

III. ANALYSIS OF VSWR WITHSTAND CAPABILITY OF A BALANCED AMPLIFIER

The scattering matrix of an ideal quadrature coupler at band center is given by

$$(S) = \frac{1}{\sqrt{2}}\begin{pmatrix} 0 & 1 & 0 & -j \\ 1 & 0 & -j & 0 \\ 0 & -j & 0 & 1 \\ -j & 0 & 1 & 0 \end{pmatrix} \quad (1)$$

where the port numbers are as defined in Figure 2. For a balanced amplifier with a mismatched load then the two transistors see a two-port network formed by the directional coupler with port 2 terminated in a reflection coefficient of $\Gamma = 0$ and port 4 terminated in a reflection coefficient of $\Gamma = \Gamma_L$. Straightforward calculation shows that the resulting two-port network has a scattering matrix given by

$$(S) = \frac{\Gamma_L}{2}\begin{pmatrix} -1 & -j \\ -j & 1 \end{pmatrix}. \quad (2)$$

The scattering matrix given by equation (2) can be converted to a Z matrix given by

$$(Z) = Z_0\begin{pmatrix} 1-\Gamma_L & -j\Gamma_L \\ -j\Gamma_L & 1+\Gamma_L \end{pmatrix}. \quad (3)$$

Thus at band center the two transistors see the simple equivalent two-port network shown in Figure 4 where the element values are given by

$$Z_A = Z_0(1 - \Gamma_L + j\,\Gamma_L)$$

$$Z_B = -jZ_0\,\Gamma_L$$

$$Z_C = Z_0(1 + \Gamma_L + j\,\Gamma_L) \quad (4)$$

Hence the *electronic* load seen by the two transistors is given by

$$Z_{electronic\ load} = Z_0(1 \pm 2\Gamma_L) \quad (5)$$

which when expressed as a reflection coefficient is given by

$$\Gamma_{electronic} = \frac{\pm\Gamma_L}{1\pm\Gamma_L}. \quad (6)$$

Hence one transistor sees an improved VSWR mismatch whilst the other one sees a worse VSWR mismatch. Equation (6) is a new result in the field of balanced amplifier theory.

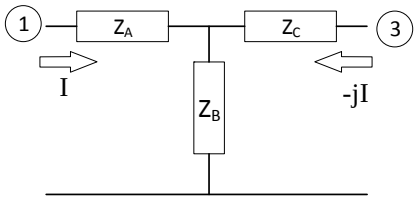

Figure 4. Equivalent network seen by the two transistors.

As an example of the application of equation (6), if the VSWR withstand capability of each transistor is 5:1 then the maximum VSWR withstand capability of the balanced amplifier is only 2.3:1. It should also be noted from equation (5) that if the external mismatch exceeds 3:1 ($\Gamma_L = 0.5$) then one transistor will see a negative resistance. While this a mathematically correct deduction, this situation won't arise in practice unless the transistor can survive an infinite VSWR mismatch as the transistor will already have failed at a lower value of external VSWR mismatch. However, one of the transistors may see a negative resistance under small-signal conditions in the presence of an external mismatch which might cause instability.

Finally, it should be noted that in the presence of a mismatch that there will always be some phase of the external load which causes one of the transistors to see a higher load

resistance than the designed value for maximum power output. The circuit in Figure 2 upon which this analysis is based assumes an ideal constant current generator which generates a constant current regardless of the voltage across it. For a real transistor this is only true provided the drain-source voltage is greater than the knee voltage and below the breakdown voltage. In a mismatch situation the increased load resistance will cause the voltage to enter the breakdown region with the result that the current through the transistor will rapidly increase and the device will fail through excess thermal dissipation.

IV. COMPUTER SIMULATION

Figure 5 shows the simulation file while Figure 6 shows the reflection coefficient seen by the two transistors. The magnitude of the reflection coefficient of the load was swept from 0 to 0.5 while the phase was varied from -180^0 to $+180^0$ in 7.5^0 increments. It can be seen that the simulated results are in complete agreement with Equation (6).

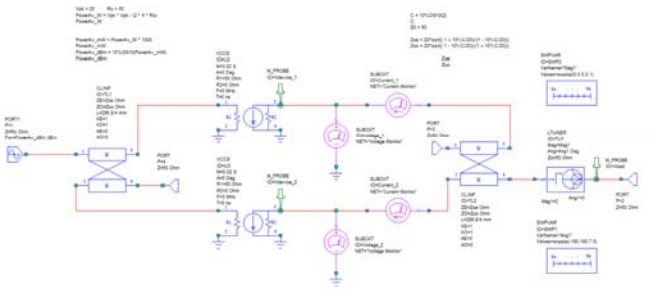

Figure 5. Simulation file of the balanced amplifier.

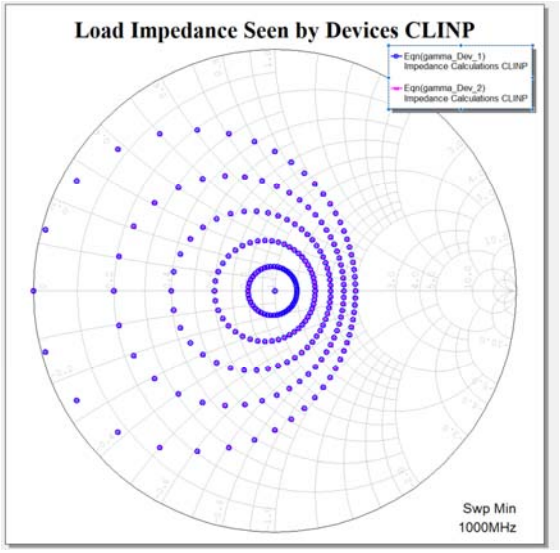

Figure 6.Reflection coefficient seen by the two transistors.

Finally, the simulation was re-run but with the simplified ideal transistor model replaced with the Statz model and with RF matching incorporated between the transistor and the quadrature coupler to provide a more realistic model for a transistor and the amplifier. The Statz model incorporates finite knee and breakdown voltages, non-linear capacitances and current generator etc. Figure 7 shows the reflection coefficient seen by the transistor under the same sweep conditions as previously. While the magnitude of the reflection coefficient seen by the transistor is now not as large, it is still larger than that of the external load.

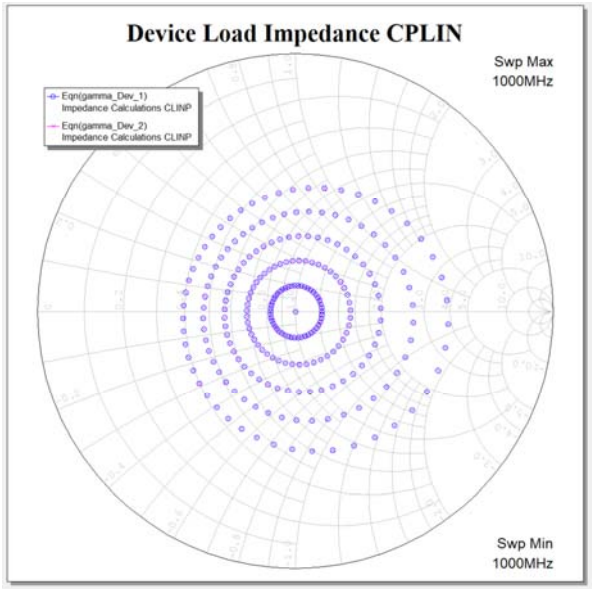

Figure 7. Reflection coefficient seen by the individual amplifiers.with the transistors represented by a Statz model and with RF matching incorporated between the transistor and the quadrature coupler. The sweep conditions are identical to those in Figures 6

V. CONCLUSION

This paper has shown both theoretically and by computer simulation that a balanced amplifier has a reduced VSWR withstand capability than that of the transistors that are used in its construction.

REFERENCES

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