A New Approach to Frequency Synthesis

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Abstract

A new approach to frequency synthesis permits the achievement of excellent spectral purity, high agility, very fine resolution, low power consumption and low cost. The principle of the proposed Phase Digital Synthesizer (PDS) is that the control signal of the PLL is formed by a multi frequency-phase comparator with phase splitting of the reference and VCO signals into a large group of signals which are compared in the partial detectors. The outputs of these partial detectors are then summed to develop the VCO control voltage. The main advantage of the method is that there is no division ratio in the loop and thus there is no multiplication of noise and spurs normalized to the phase comparator. The synthesizer of PDS type can be used instead of complicated multi-loop systems which are too expensive, bulky and with high power consumption.

1. Introduction

The most important characteristics of the frequency synthesizer are the agility, spectral purity and frequency resolution of its signal. It is indispensable that they be of high enough level to obtain high quality telecommunication and measuring equipments. There is no necessity to review all possible variants of synthesizer structures because there is detailed description of them in [1-3]. In brief, in the most cases, it is Direct Digital Synthesizers (DDSs) and phase-lock loop (PLL) frequency synthesizers or, as well, the different combinations of such structures.

As it is known, the DDS synthesizers while being very fast switching and having fine resolution do not provide good enough spectral purity on high output frequencies because of the spurious signals (spurs), and cannot always be used in the direct way in telecommunication and measuring equipments. As a rule, they are used as the parts in complicated synthesizer structures which include addition means for transferring low-frequency and narrow-band DDS output (where the level of the spurs is good enough) to the high-frequency and broad-band output of the complete synthesizer. In general, the means are the integer-N PLL frequency structures with high enough reference frequency, having thus a good spectrum purity and agility, but big step size which is to be filled up with the DDS band in a summing PLL.
That is why in order to provide simultaneously high specs of agility, spectral purity and frequency resolution they resort to multi-loop structures which are bulky, expensive, and with greatly increased power consumption.

So here, only the different variants of single-loop synthesizers will be considered because they are closest to the structure of the PDS synthesizer to be described.

The synthesizer based on a single-PLL with divider of integer variable ratio in the loop [4-5] is the simplest structure, but because of its well known disadvantages, is used by itself only in the systems where there is no need to have simultaneously very high specifications of frequency resolution, agility and spectral purity, or used in the multi-loop structures as it was already mentioned above.

The most significant improvement of the single-loop synthesizer is disclosed by J.N.Wells [6]. This structure named as Frac-N, DSM is a loop with a fractional divider in which for compensation of fractional components the author used an idea of Delta-Sigma Modulation (DSM) that was known considerably earlier, in 1960s, being used in Digital-to-Analog and Analog-to-Digital converters.

The chips based on such an idea are designed and manufactured by ADI [7], Skyworks Solutions, Inc. [8], Hittite Microwave Corp. [9] and many others. They have low power consumption and low cost but have as well, low spectral purity (because of spurs). They have poor agility too because PLL bandwidth must be narrowed enough (as a rule, some tens of kHz) to suppress quantization noise due to delta-sigma modulation which increases steeply with increasing offsets from carrier. It seems the most significant achievement in developing the Fractional-N-DSM method has been obtained by the designers of Hittite Microwave Corp. with the raising of comparison frequency over 100MHz and enlarging PLL bandwidth to few hundreds kHz. The prospects for further enlarging PLL bandwidth in order to heighten agility, having the same good enough spectral purity, are rather moderate.

The goal of this work is to show that not all possibilities in developing of single-loop synthesizers are exhausted, and that there are such variants of schematic composition which could realize simultaneously the advantages of the all synthesizer types existing on the world market today. It is agility of DDS, low cost and low power consumption of Frac-N-DSM synthesizer, and high spectral purity of multi-loop system.

Further, for short, the new type of synthesizer is named as PDS - Phase Digital Synthesizer.

2. Description of the new type of frequency synthesizer

The idea of PDS synthesizer can be explained with one of its version shown in Figure 1.
There is a reference accumulator (R-accumulator), clocked by reference frequency f_r and having, for example, n=32 binary bits in sum: blocks of most significant and least significant bits (MSBs and LSBs respectively), coupled to each other by a carry network. The number of bits in the blocks can be, for example, k=5 and n-k=27 bits respectively. Data inputs D of MSBs and LSBs blocks (for codes R1 and R2) are connected to a HOST unit (user input) which generates the frequency tuning word R=R1+R2 determining the synthesizer carrier and provides direct FSK and PSK modes.

A Phase Splitter generates on its $K=2^k$ outputs the pulse sequences of frequency $F_r=Rf_r/q$, on the average, where $q=2^n$. Each of the sequences is an exact copy of full accumulator overflow, and the sequences are shifted in time respectively to each other by T/K, where $T=q/f_r$. In fact, all the sequences are the result of dividing the reference frequency f_r by a fractional value q/R. In other words, there are as if formed K, for example K=32, overflow outputs of the accumulator, and these outputs are shifted in time.

Thus, the phase splitter forms the K reference sequences for the PLL. The latter contains, in consecutive order, a voltage controlled oscillator (VCO), divider i.e. prescaler (:N, if it is necessary), pulse distributor, phase comparator, digital-to-analog converter (as example it is the simplest R-ladder), and a low pass filter (LPF). The output of the VCO is the output of the synthesizer.

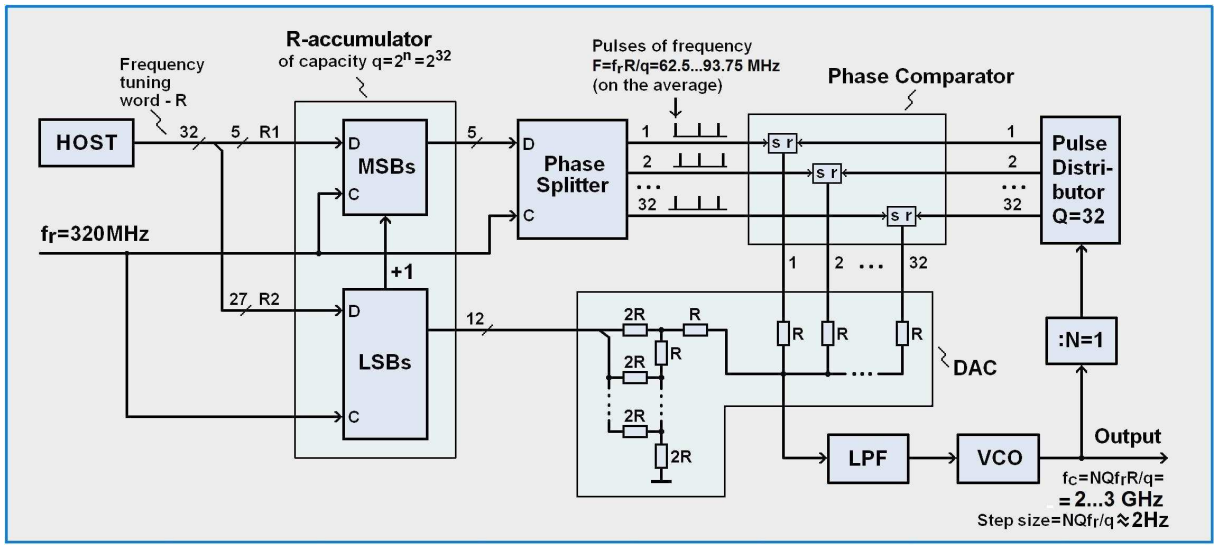

Figure 1: Block Diagram of Phase-Digital Synthesizer (PDS)

In order to be able to phase compare the signal of VCO with the reference sequences from the phase splitter, there is the need to generate, in the pulse distributor, the analogous sequences from VCO. In one of the possible versions, it is fulfilled in the same way, with phase splitter, as it was explained above, i.e. the pulse distributor contains an accumulator, the same as MSBs mentioned above, of capacity Q=K, and a phase splitter, both clocked by signal pulses f_c. The accumulator has a code C on its input which can be both constant or variable, and thus the pulse distributor forms on its Q=K outputs the K periodic or quasi-periodic pulse sequences (depends on whether numbers K is divisible by C or not) of frequency $F_c=f_cC/K$, on the average, and these sequences are shifted in time relative to each other.

The phase comparator (in fact, it is a phase detector – PD only fulfilled in a particular way) can be a set of RS flip-flops the number of which is K. The S-input of each RS flip-flop is connected to one of the K outputs of the phase splitter. The R-inputs of the RS flip-flops are connected to the Q outputs of the pulse distributor. If Q=K, as it was assumed above, then the R-input of each RS flip-flops is connected to the corresponding one of the K outputs of the pulse distributor.

In another version, if in the simplest case, the input number C of the accumulator is set to 1, then this structure is equivalent of a ring counter. Its capacity Q can be less than K, for example Q=4. The latter is a simple device which is convenient in practice. In this version all RS flip-flops should be subdivided into Q number of batches, with K/Q flip-flops in each batch. In each batch, all R inputs of the flip-flops are connected to a corresponding output of the ring counter. In example, as it is shown in Figure 1, the pulse distributer is a ring counter with Q=K=32.

The duration of pulses on the RS flip-flops outputs depends on phase differences of the pulse sequences from the outputs of phase splitter and pulse distributor. After being passed through the DAC and the LPF the pulses are transformed into the voltage for controlling the frequency

of the VCO. Thus, each of the RS flip-flops with the correspondent bit of KR-segment of the DAC operates as a partial phase detector bringing its own portion into the full scale of the control voltage.

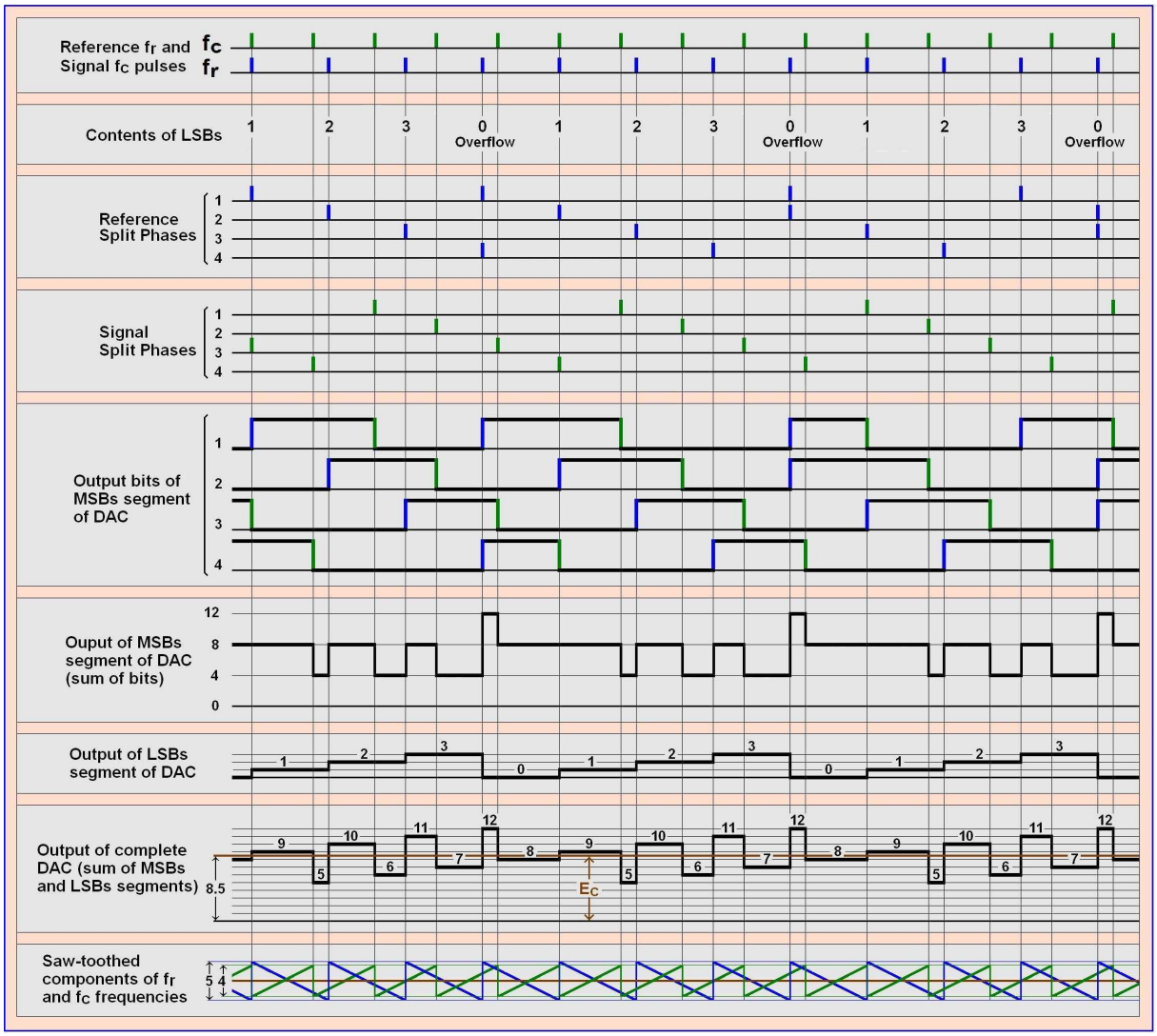

Figure 2: Functional Diagrams of PDS operation

Due to action of the PLL, there is provided an equation $f_c=NQf_rR/q$. In the example of Figure 1 there is provided a range 2...3 GHz with step size about 2 Hz if reference frequency is 320 MHz. The step size can be lessened, if it is needed, by adding corresponding bits in LSBs block.

For compensation of fractional noise there is a R2R-section of DAC, in addition to the KR-section, depicted in the Figure 1 as R2R-ladder. It transforms current contents of LSBs block into an analogue value to be summing it in complete structure of the DAC.
More detailed explanation how it is in action can be understood with the help of an example of the simplest structure of PDS. Let's assume that the full reference accumulator consists of 4 bits with 2 bits in MSBs block and 2 bits in LSBs block. The full value of its input code equals R=5, i.e. in view of weight, it is R1=1 on input of MSBs block and R2=1 on input of LSBs block. Pulse distributor for signal clocks is a ring counter of 4 bits. In such a structure, PDS operates as it is shown in diagrams of Figure 2.

As it follows from the diagrams, in the output of the DAC there are only direct component E_c and the two saw-toothed components of f_r and f_c frequencies. The E_c component is used as control voltage for VCO and the saw-toothed components are easily filtered by LPF.

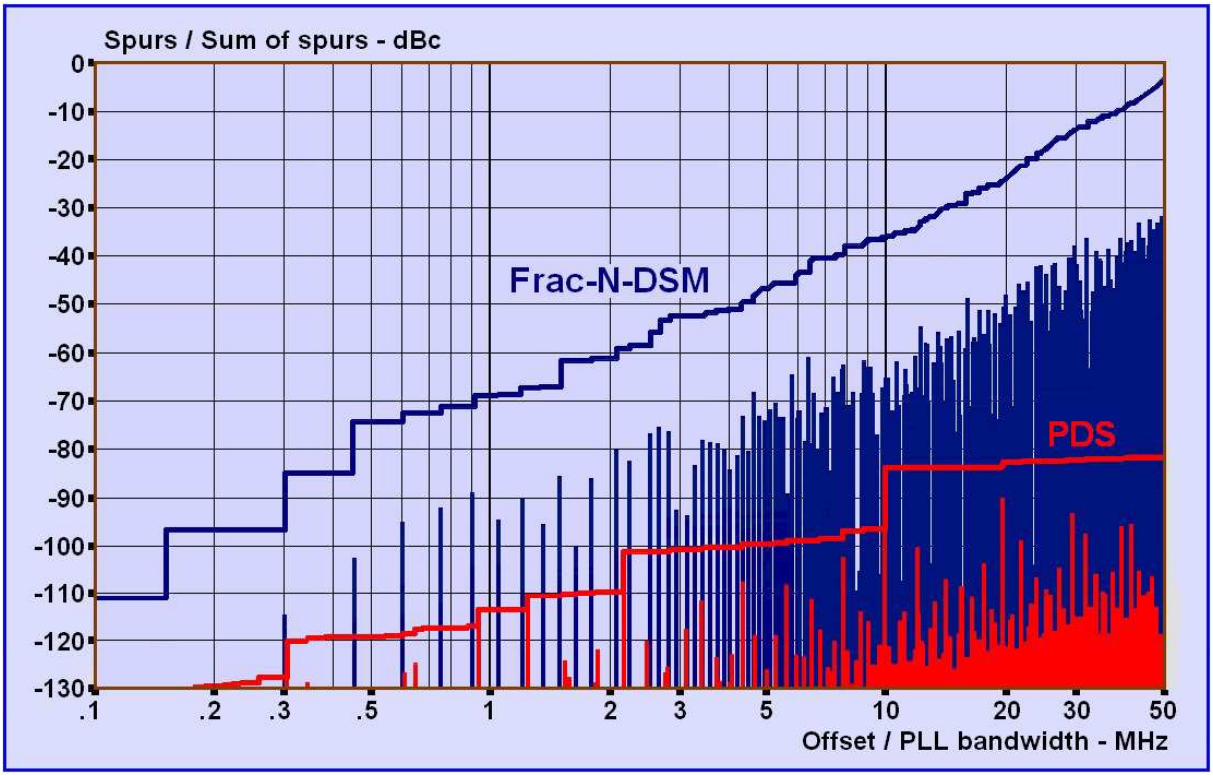

Figure 3: PDS vs. Frac-N-DSM – comparison of spurs in a typical case

It is important to note that, as it is shown in Figure 2, in PDS synthesizer each pulse of the signal frequency is phase controlled by the phase comparator, and the each pulse of reference frequency, through the phase comparator, works to phase control the signal pulses. In other words it is as if the division ratio in PLL is equal 1.

So the main advantage of PDS structure is that there is no need to have divider in the loop which is indispensable in Frac-N synthesizer and hence which lowers comparison frequency. That is why the bandwidth of PLL can be chosen to be as wide as required to suppress the noise of the VCO or/and to provide desirable fast switching speed.

The diagrams in Figure 2 are for a case of an ideal DAC, not having any inaccuracy. It is quite understandable that if there is inaccuracy, e.g. in any bit of KR-segment of DAC, then it results in a spurious spectrum, having correspondent distribution of components. As a result of a large enough number of bits in the KR-segment, the influence of each bit inaccuracy on the level of total spurious components is lowered.

Additional information about this version of synthesizer can be got from [10].

Figure 3 demonstrates the comparison of spurs and their sum in PDS (in red) against the same specs of Frac-N-DSM synthesizer (in blue) in one of typical cases when signal frequency is 2,640,312,500 Hz and reference frequency is f_r=320 MHz.

In this case there is assumed that the real amplitude inaccuracy of DAC of PDS for a bit of its KR-segment can be as small as dA=0.1% (as it is known from experience of ADI). It is also quite evident that DAC inaccuracy for the bits of R2R-segment, due to their smaller weights, exerts significantly lesser influence over the spurs. This PDS synthesizer has a reference accumulator of 15 bits (MSBs is of 5 bits and LSBs is of 10 bits). Control code on input of the R-accumulator is R=01000,0100000001.

The Frac-N-DSM synthesizer has a divider of integer ratio N=8 in the loop and a fractional unit of 10 bits including 2 DSM-accumulators of the same number of bits. Control code on input of the fractional unit is 0100000001 (the same as for LSBs of PDS). Phase detector is considered as of ideal linearity, not having inaccuracy.

From comparison of the diagrams it can be seen that even at mentioned best for Frac-N-DSM, and when the division ratio in the loop is as small as only N=8, PDS has absolute advantage over Frac-N-DSM type of synthesizer. It is especially due to broad band mode of PLL that allows the building synthesizers of ultra high agility.

3. Conclusion

The analysis presented above shows the superior possibilities of the approach to frequency synthesis proposed. Described schematic, being implemented in integrated chip, would allow to create the simple single-loop synthesizers having features of agility and spectral purity not worse than complicated multi-loop structures have, and at the same time to be by an order of magnitude or more cheaper and with significantly less power consumption.

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