Design of RF/microwave amplifiers for maximum power using harmonic balanced simulation when the only available data are the transistor's small signal *S*-parameters

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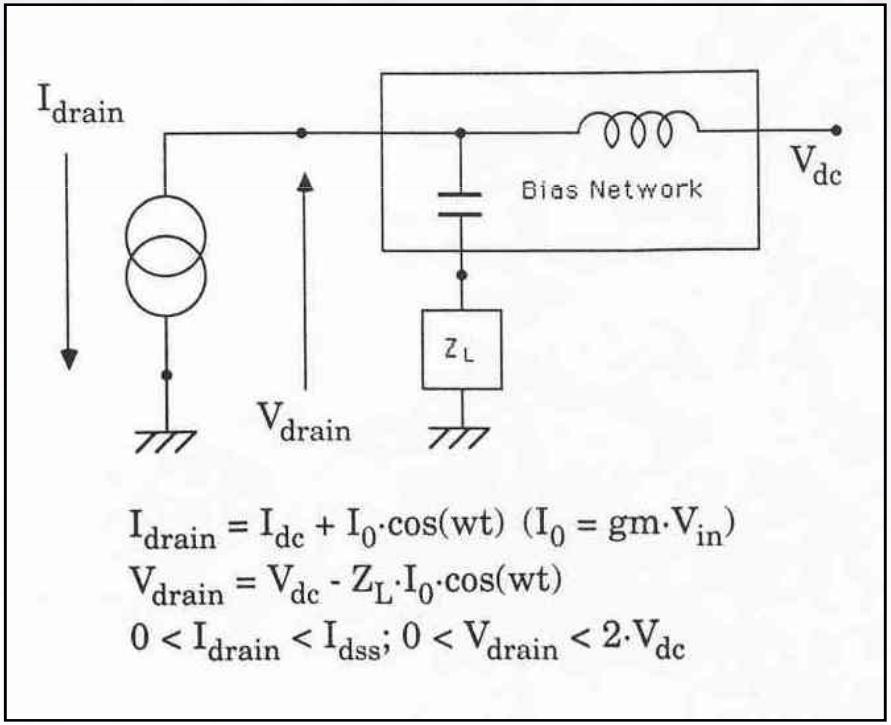
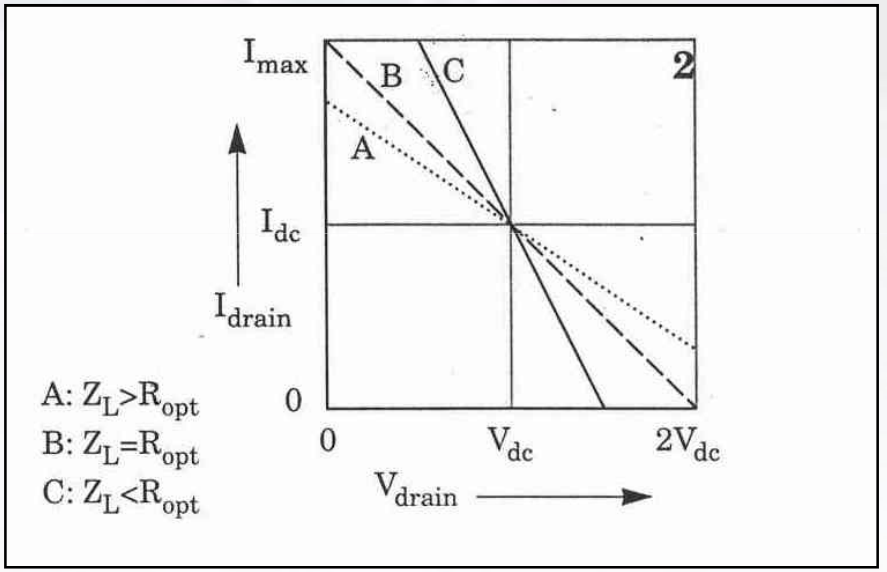
- It should be immediately obvious that there is controversy in this topic - *S*-parameters alone combined with harmonic balance cannot provide for the simulation of the power performance of the transistors.
- This topic is a sequel or an extenuation of the paper “RF and microwave solid-state power amplifiers design is a speciality” presented last year in April at the ARMMS meeting [6].
- The topic is also an extension of Steve Cripps’s Load-Line Approach, which was developed further and fully with the *power parameters* introduced by Pieter Abrie [4].

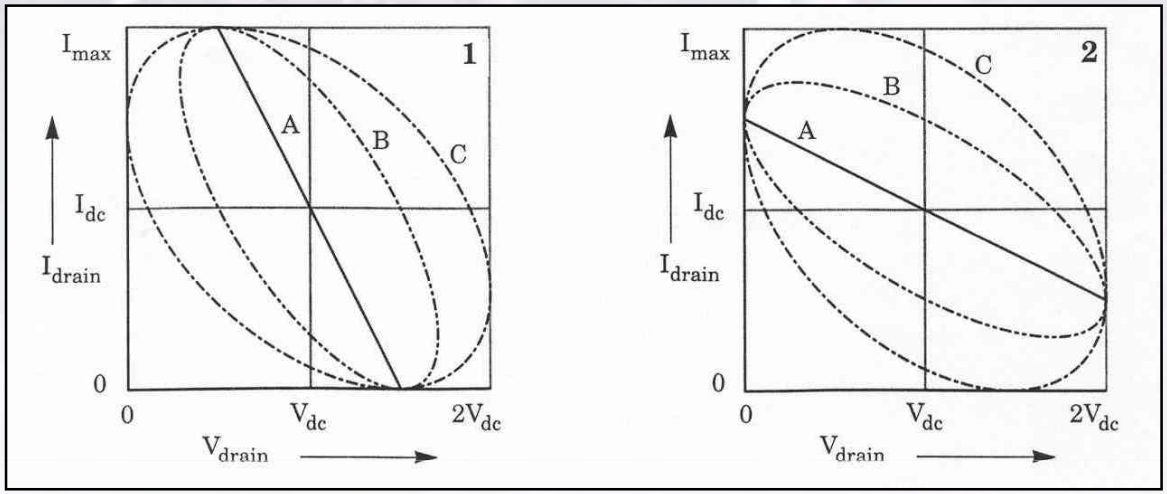
A Recap of the Steve Cripps Load-Line Approach [1]-[3]





- $R_{opt} = 2V_{dc}/I_{max} = V_{dc}/I_d$
- $P_{opt} = (1/2)V_{dc}/I_{dc}$
- $P = P_{opt} * R_{opt}/R_L$
- $P = P_{opt} * RL/R_{opt}$

Note: Graphs and math copied from [2]


I_{max}
1
A
B
C
I_{dc}
I_{drain}
0
0
V_{dc}
$2V_{dc}$
V_{drain}
I_{max}
2
C
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A
I_{dc}
I_{drain}
0
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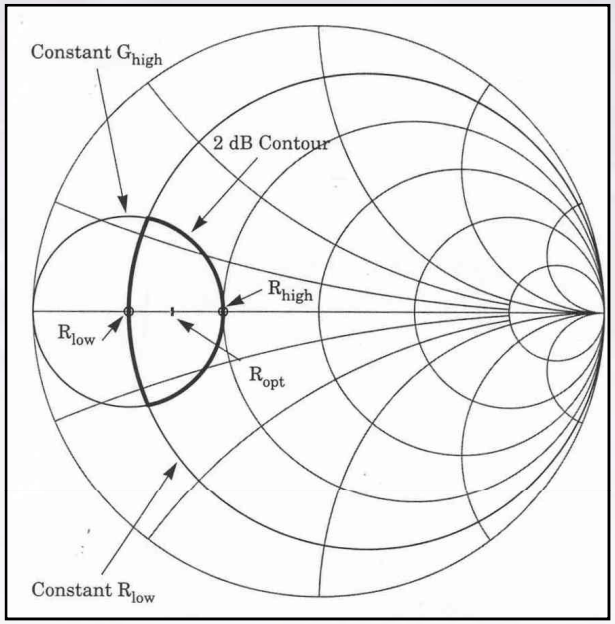
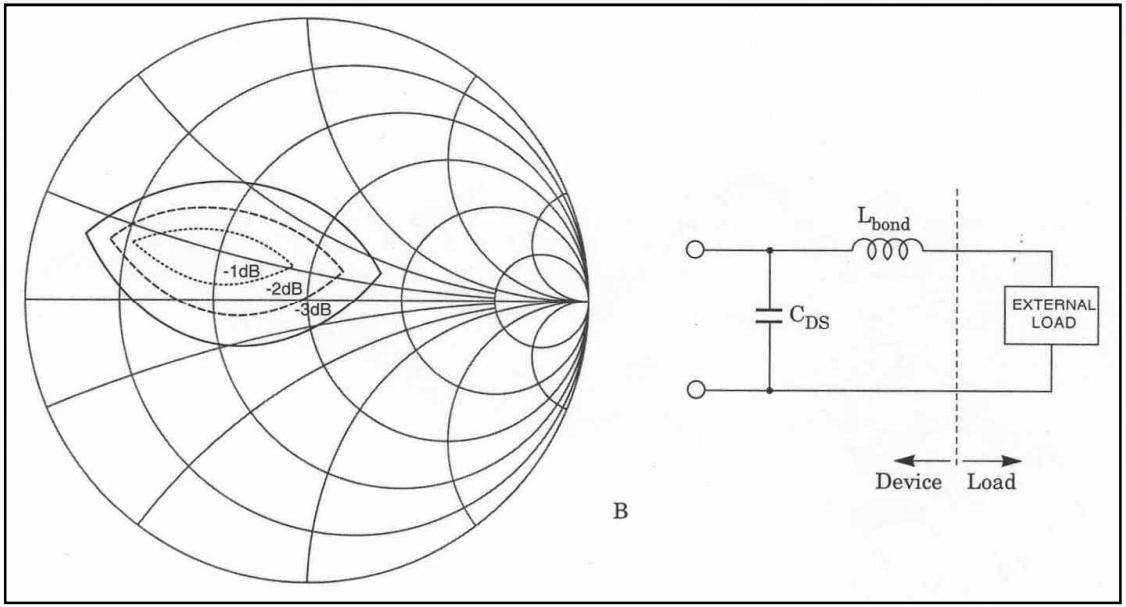
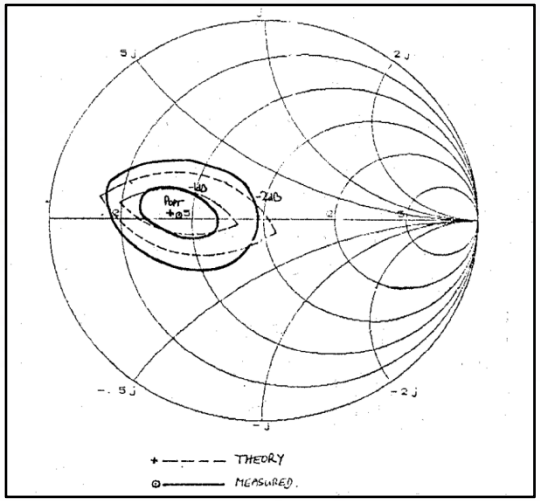
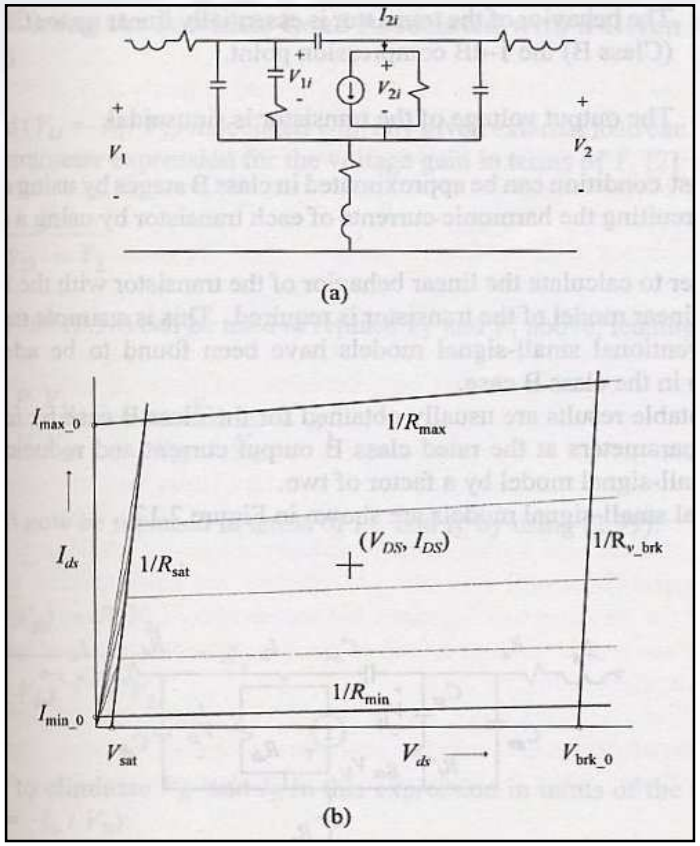

Constant G_{high}
2 dB Contour
R_{high}
R_{low}
R_{opt}
Constant R_{low}


-1dB
-2dB
-3dB
B
L_{bond}
C_{DS}
EXTERNAL LOAD
Device
Load

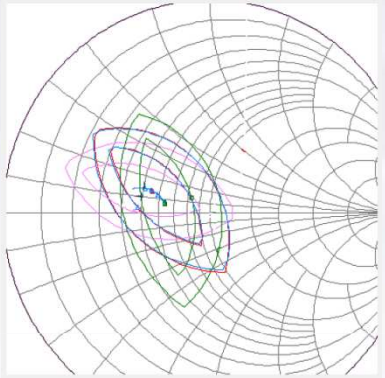

THEORY
MEASURED

- The original paper [1] was published in 1983 when harmonic balance (HB) simulation was not in use yet and Load-Pull measurements were the only option available.
- When the Technical Note [2] was published HB simulations were around but were, among other problems, very slow. The Cripps Approach, therefore, was still offering a much simple way to design for high power.
- In [2] Cripps expressed a hope that the simple math of his approach should be incorporated in the general linear simulators “in much the same way that most of the currently available packages compute noise figure”.
- He also stated that with “some slightly innovative use” the approach could be applied when there is feedback, and also for multi-stage design, etc.
- Unfortunately his approach was never implemented in any of the general simulators.
- It was, however, implemented in a more advanced form in the specialized MultiMatch Amplifier Design Wizard [5] developed by Pieter Abrie.

- Pieter Abrie presented the *power parameters* in his book [4] and implemented them in MultiMatch for the design of Class A and Class AB amplifiers.



- $V_1 = MV_{1i} + NV_{2i}$
- $V_2 = OV_{1i} + PV_{2i}$
- $I_{2i} = RV_{1i} + SV_{2i}$



- The mapping functions of the *power parameters* lifted any restrictions associated with the transistors configuration, including feedback, resistive loading, grounding node position, parallel chips/cells, reference plane issues, multistage, etc.
- There are interesting similarities with the Noise Parameters, e.g. series feedback allows for easier match for maximum power.

- Today the harmonic balanced simulations are often as fast as the linear simulations were 20 something years ago.
- While accurate non-linear transistor models have been developed, non-linear models are still not provided for many useful transistors.
- The *power parameters* approach is a fully developed approach which can easily be incorporated in any of the general simulators to speed up and enhance the design process for P1dB, Psat max, etc., especially when non-linear models are not available.

- The streamlined design process of [6] for the design of a 0.5-2.5GHz stage with a 45W GaN HEMT will be revisited here.
- In addition to the design process of [6], the results of the harmonic balanced simulations of the dynamic load-lines for each stage will be shown. This will enhance the understanding of the design process and will also show a way of extracting the desired power from a transistor stage when a non-linear model is not available.

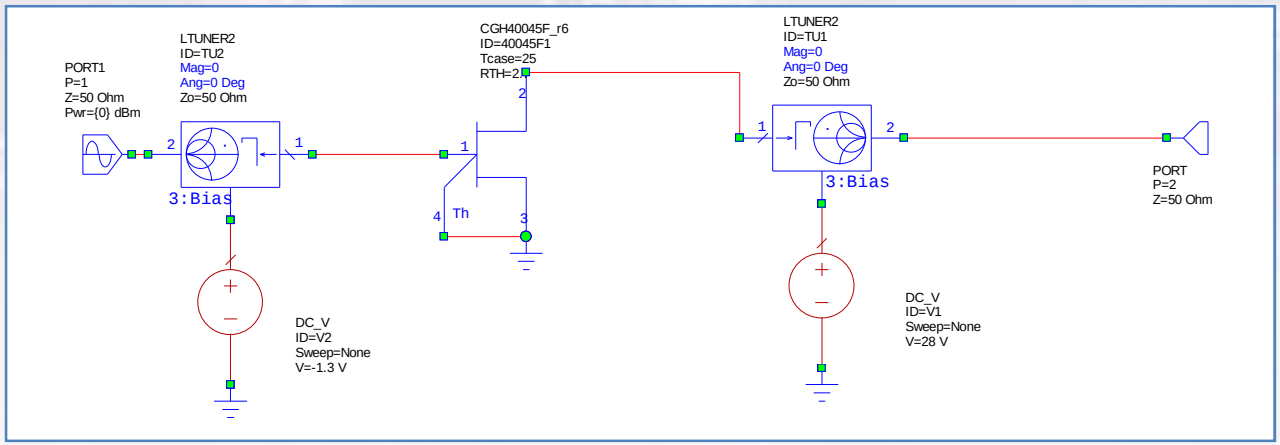


Figure1. Extraction of design data in Microwave Office

- Figure 1 shows a schematic in Microwave Office [7] simulator of AWR in which the non-linear model of the transistor and the tuners could be used to extract the impedances for the maximum power and gain over the frequency band. Instead only the *S*-parameters at transistor Imax/2 are extracted.

- The extracted *S*-parameters are then imported into MultiMatch where a linear model is fitted to them (Figure 2). After defining the maximum current and voltage areas (clipping boundaries) on the I/V-curves, the *power parameters* are used to extract the Load-Pull data (Figure 3).

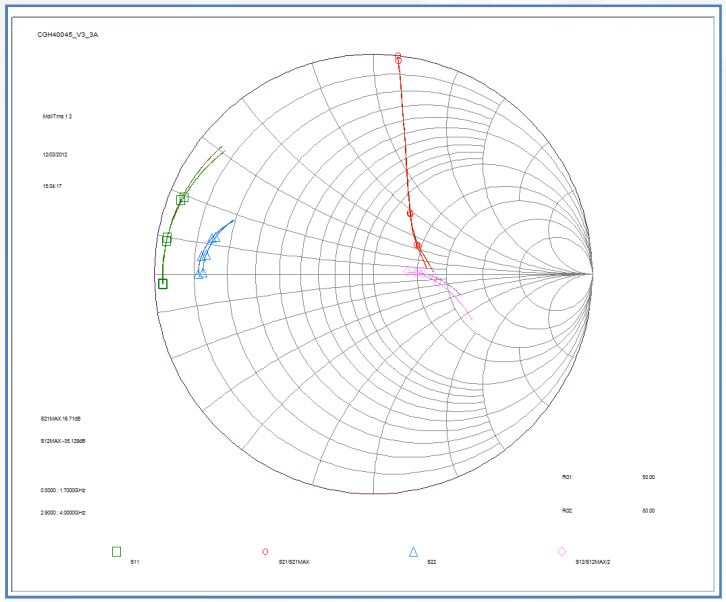


Figure 2. Fitting linear model to the S-parameters in MultiMatch

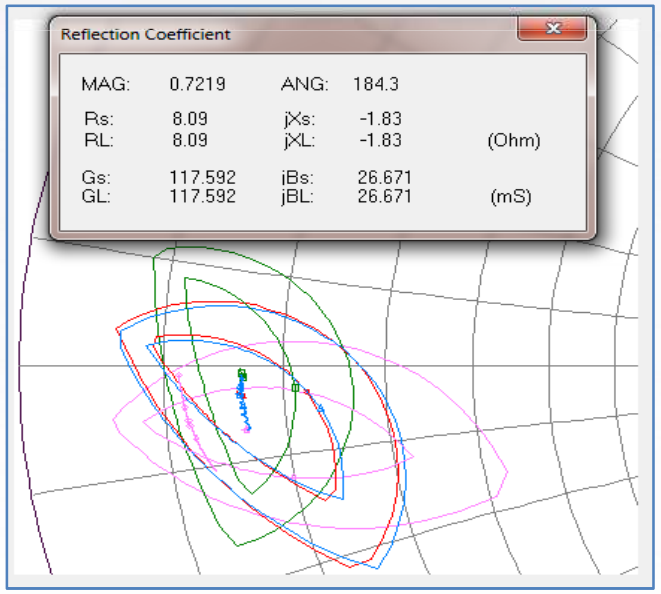


Figure 3. Load-Pull contours across the bandwidth

- The output network (on the right in Figure 4) is synthesized next to provide the load impedance associated for the maximum pre-clipped power.
- Synthesis of the input lossy and lossless matching networks (on the left in Figure 4) follows to provide maximum flat gain and stability.

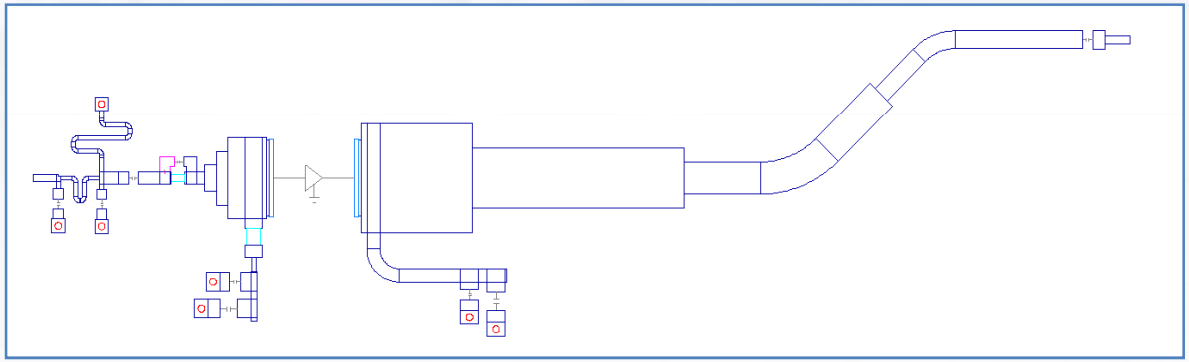


Figure 4. MultiMatch layout

- The layout is manipulated with great ease to the desired shape, and then with a few clicks of the computer mouse the schematic and the layout are exported into Microwave Office (Figure 4).

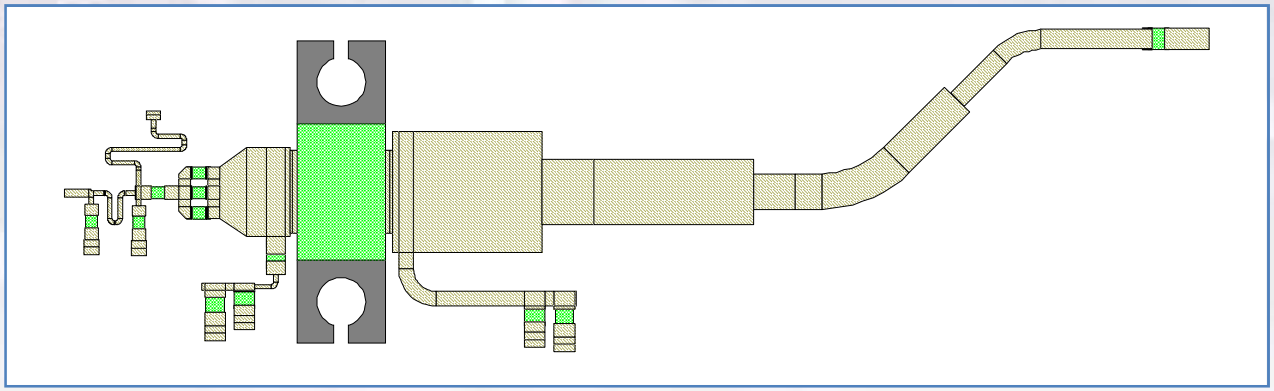


Figure 4. The layout in Microwave Office

- Back in Microwave Office the microstrip discontinuities are fully simulated, either by electromagnetic models or full electromagnetic simulation of parts of the layout.
- The non-linear model and the harmonic balance simulation are used to simulate the power levels of fundamental and harmonic signals, the associated gain and gain compression, currents and voltages, efficiency, etc.
- Using these simulations some small adjustments would usually be done to achieve the best possible performance.

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The Dynamic Load Line in harmonic balance simulator

- The technical team of the RF Cree products were very helpful and generous to provide the non-linear models with access to the voltage and current across the intrinsic generator
- The simulation of the voltage and current, and hence the dynamic load-line across the intrinsic generator provides a much higher level of visualization, understanding and design capabilities.

- In Figure 5 one can see the simulated dynamic load-lines across the bandwidth for Class A and Class AB biasing at low power levels.
- It is obvious that the Class A biasing will provide maximum swing of the voltage and current and hence maximum Psat

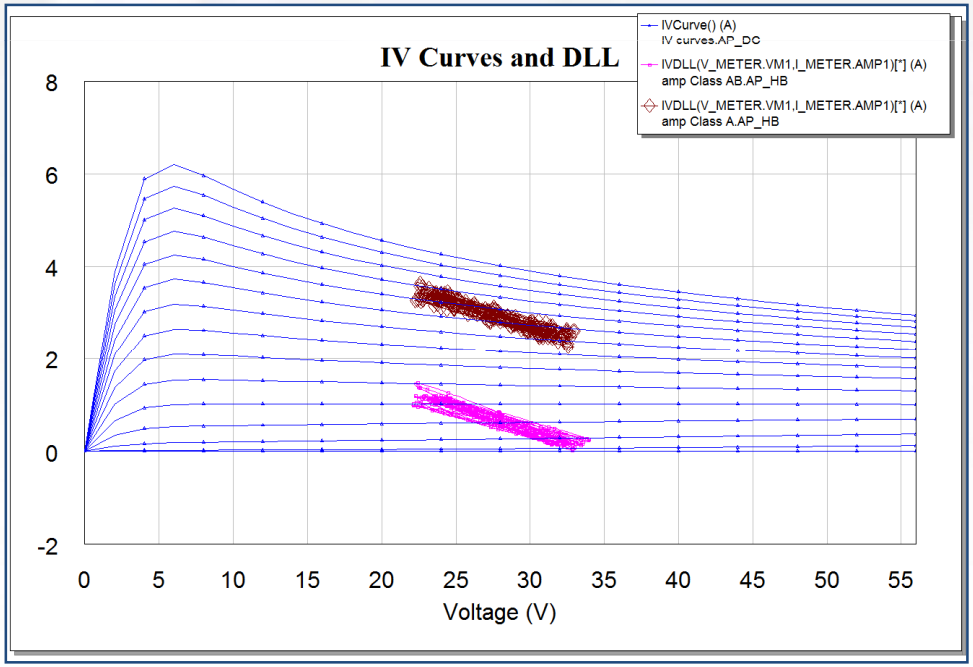

Figure 5. DLLs for Class A and Class AB

- Figure 6 shows the DLLs at Psat of Class A and Class AB
- Figure 7 shows Psat and PAE across the bandwidth for Class A and Class AB.
- It is obvious that they are about the same for the 2 kinds of biasing which is a prove of the validity of the design method

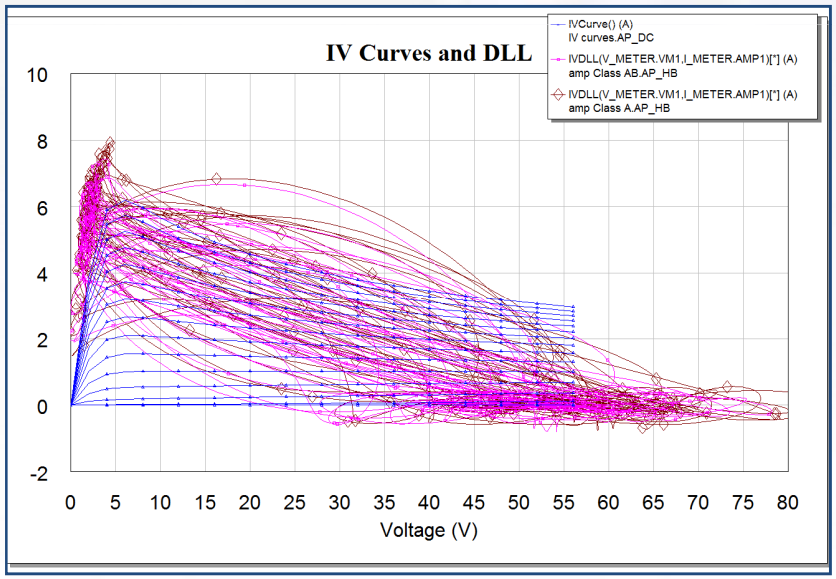

Figure 6. DLLs for Class A and Class AB at Psat

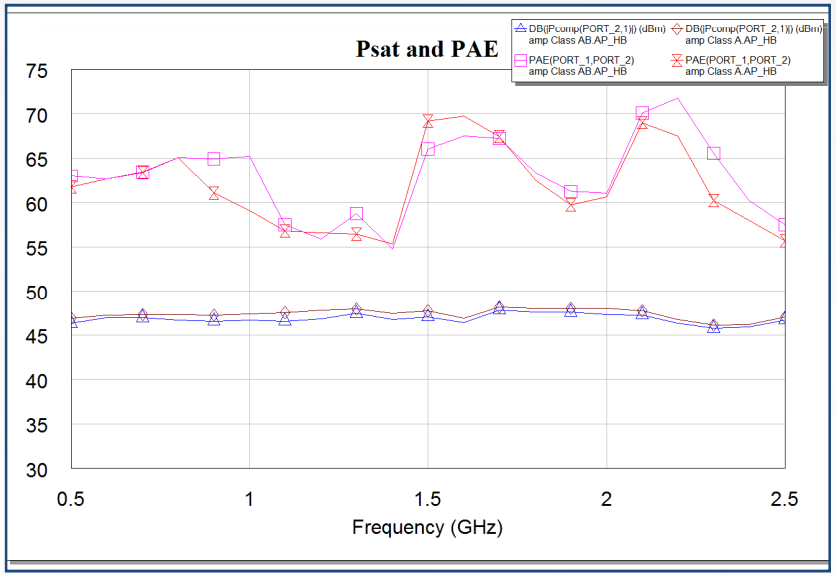

Figure 7. Psat and PAE for Class A and Class AB

- Two copies of the designed stage are connected in parallel with hybrid couplers to form a balanced output stage.
- Two consecutive driver stages are designed next. These stages are based on a Cree GaN HEMT, for which a non-linear model is available, and a GaAs HFET for which only *S*-parameters at a Class A biasing point are available.
- The *S*-parameters of the GaN transistor (extracted in Microwave Office) and the *S*-parameters of the GaAs transistor are used in MultiMatch to create linear models for these transistors. With the voltage and current boundaries defined, the *power parameters* and the synthesis facilities are used to design the two driver stages to provide maximum power and flat gain across the bandwidth.

- The simulated results of the MultiMatch design are shown in Figure 8 and 9.

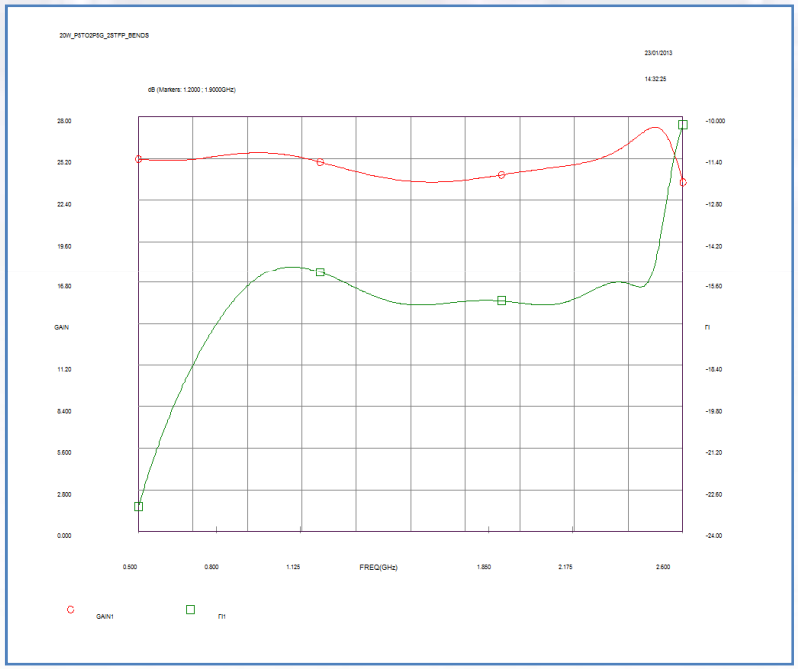

Figure 8. Gain and RL

FREQUENCY (GHz)	REFERENCED MAXIMUM LINEAR OUTPUT POWER (dBm) (Gwp (dB)) Stage 1	Stage 2	Amplifier
500.00000E-3	39.01 (-23.81E-3)	46.99 (21.22)	39.01
600.00000E-3	38.93 (-25.00E-3)	46.52 (19.61)	38.93
700.00000E-3	38.79 (-26.73E-3)	46.37 (18.38)	38.79
800.00000E-3	38.73 (-28.71E-3)	46.23 (17.44)	38.73
900.00000E-3	38.71 (-30.85E-3)	44.74 (16.73)	38.71
1000.0000E-3	38.74 (-33.11E-3)	43.69 (16.21)	38.74
1.10000	38.79 (-35.45E-3)	43.03 (15.86)	38.79
1.20000	38.87 (-37.89E-3)	42.75 (15.66)	38.87
1.30000	38.97 (-40.44E-3)	42.85 (15.60)	38.97
1.40000	39.08 (-43.11E-3)	43.38 (15.67)	39.08
1.50000	39.17 (-45.92E-3)	43.91 (15.87)	39.17
1.60000	39.06 (-48.90E-3)	42.84 (16.17)	39.06
1.70000	38.95 (-52.10E-3)	42.10 (16.58)	38.95
1.80000	38.85 (-55.57E-3)	41.76 (17.05)	38.85
1.90000	38.76 (-59.39E-3)	41.90 (17.53)	38.76
2.00000	38.70 (-63.65E-3)	42.65 (17.93)	38.70
2.10000	38.65 (-68.50E-3)	44.24 (18.15)	38.65
2.20000	38.62 (-74.16E-3)	44.98 (18.04)	38.62
2.30000	38.61 (-80.96E-3)	44.08 (17.49)	38.61
2.40000	38.59 (-89.48E-3)	44.13 (16.50)	38.59
2.50000	38.55 (-0.10)	41.61 (15.13)	38.55

Figure 9. Pre-clipped power for each stage and the full amplifier

- In Figure 9 stage 1 is the output stage and stage 2 is the input stage of this two-stage driver.

- The schematic in Figure 10 was imported into Microwave Office from MultiMatch. The *S*-parameters of the two transistors were replaced with the non-linear model for the Cree GaN transistor and the linear model for the GaAs HFET.
- Voltage and current meters were placed across the intrinsic generators and an M-probe at the output of the GaAs transistor.

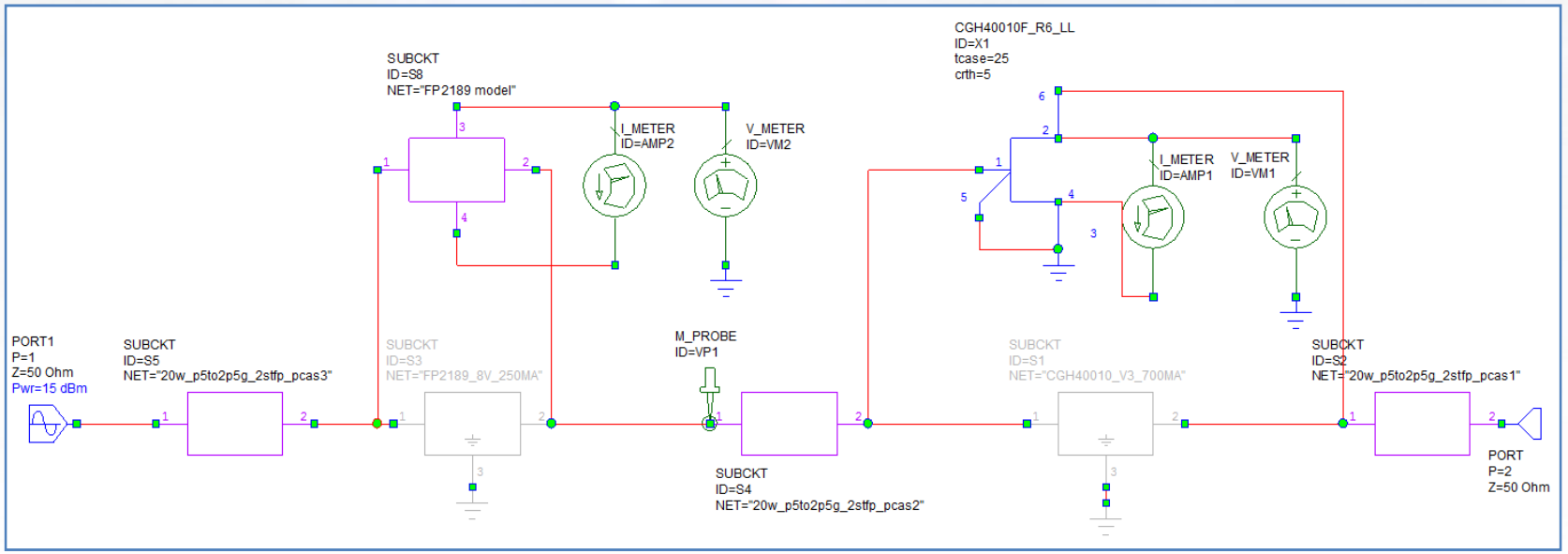

Figure 10. Driver schematic in Microwave Office

- In Figure 10 the non-linear model was used to simulate the I/V-curves and the DLLs of the GaN transistor stage across the bandwidth.
- Also superimposed over them in the lower left corner are the boundaries that define the pre-clipped maximum voltage and current swings of the GaAs transistor. The DLLs are shown inside these boundaries. These load-lines were simulated by using the harmonic balanced simulator and the linear model of the transistor.
- The input power levels were selected/tuned so that the DLLs of the GaAs transistor stage just reached the hard clipping boundaries.

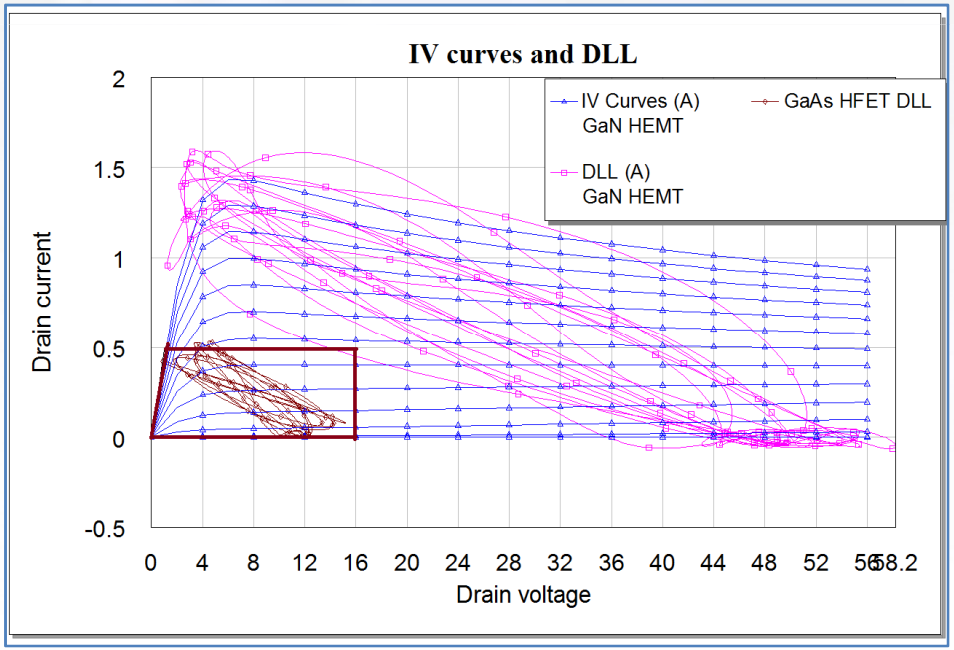

Figure 10. Driver schematic in Microwave Office

- From Figure 10 it could be seen that when the GaN transistor is already in deep compression the GaAs transistor has just started to compress.
- The pre-clipped output power is typically 0.5-1dB below P1dB.
- It is obvious that the GaAs stage has sufficient power to drive the GaN stage.

- Figure 11 shows the overall power gain, input RL and the overall output power and also the power at the output of the GaAs transistor measured by the M-PROBE in Figure 10.

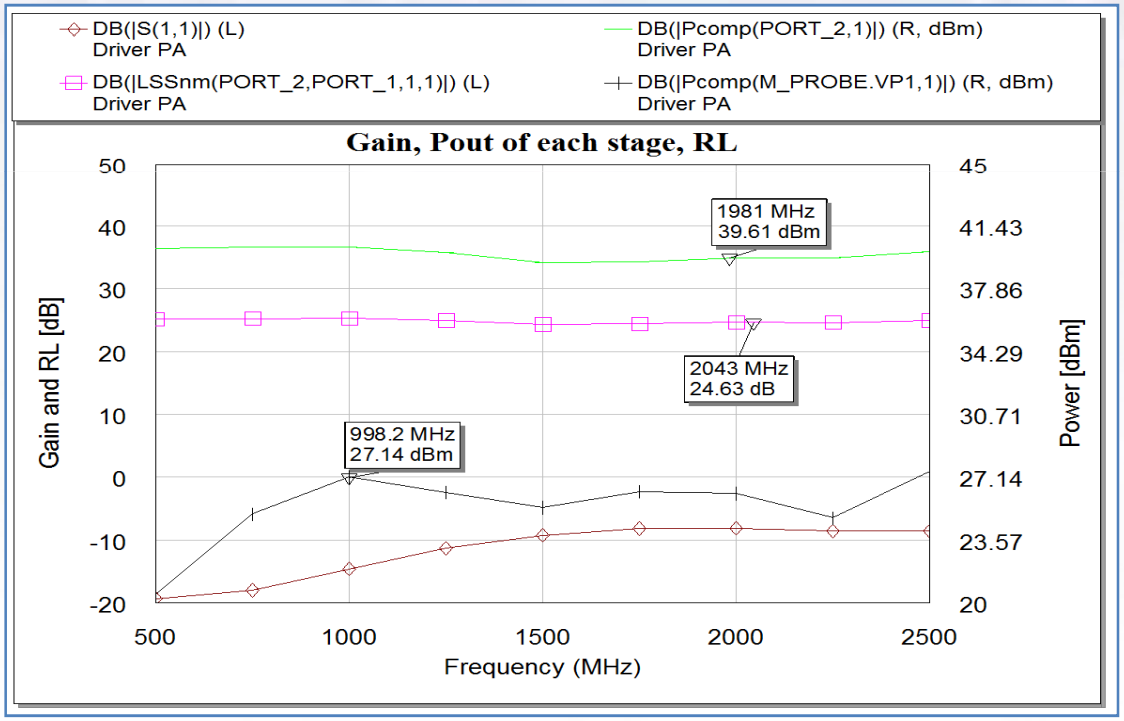

Figure 11. Power and gain performances of the 2 stage driver

- The linear model of the GaAs transistor was extracted from the *S*-parameters in a special facility in MultiMatch. It is also possible to do this in Microwave Office.
- For the GaAs transistor the only data available was the *S*-parameters, and after using them to extract a linear model, the harmonic balanced simulation was used to simulate and predict the pre-clipped maximum output power (Class A).

- This method of simulating the DLL and the pre-clipped output power is also very useful when it is important to provide proper loading to each cell of a multi-cell transistor, or when multiple transistors are connected in parallel, as is typically done in MMIC power amplifiers.
- Optimization for the correct DLL is much faster when linear models are used. This is important because the networks are typically very complex and the input networks also need to be optimized to provide equal drive.
- Typically the MMIC design kits provide linear and non-linear models. Optimizing the initial circuit by using the linear models and then only checking the final results by using the non-linear models provides for a better and faster, and, arguably, a more accurate design approach.
- The optimum load-line for maximum output power can also be optimized relatively fast using the non-linear model of the transistor if the input power for the simulation is low.

- The method of harmonic balance simulation of the DLL using the linear model could also be used to extract the optimum load impedance for maximum output power of Class A amplifiers and, arguably, Class AB amplifiers.
- Figure 12 shows a schematic with which this could be done. It uses a linear transistor model driven by tuneable power source, an impedance tuner at the output and a Gamma probe to place the impedance of the tuner on the Smith Chart.

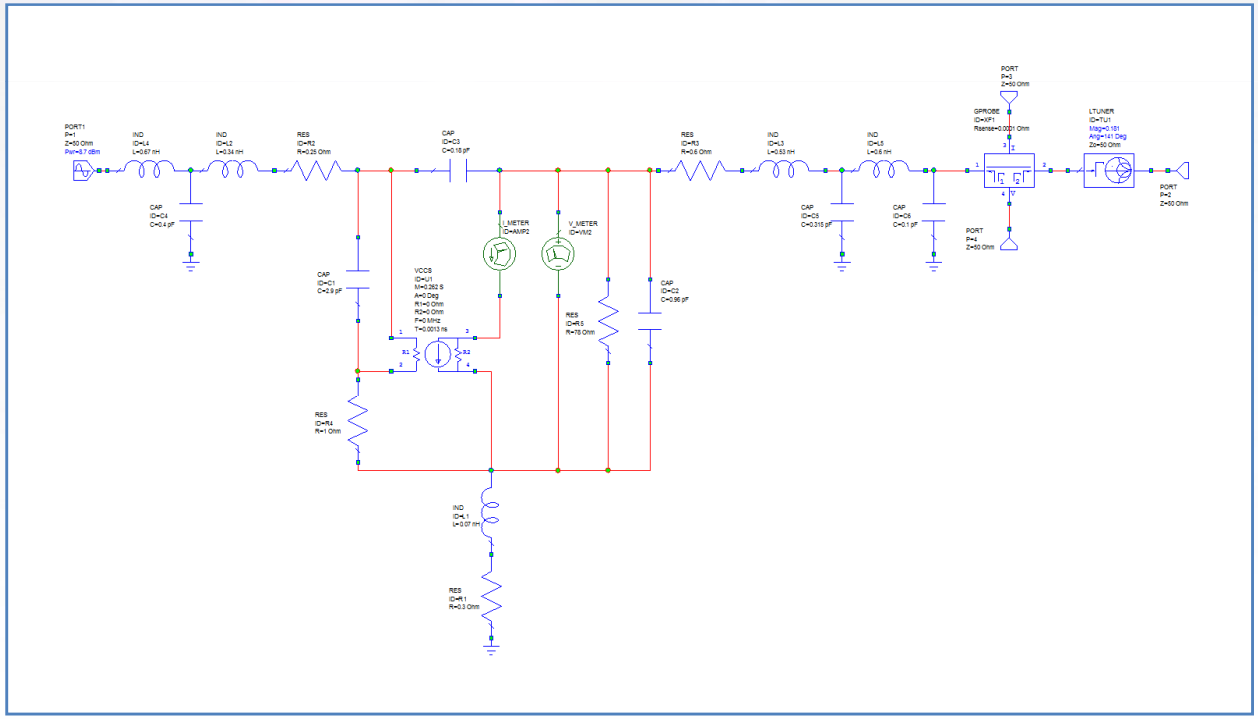

Figure 12. Optimum Load Impedance Extraction Schematic

- Figure 13 and 14 illustrate the process of extracting the optimum load impedance. Impedances for any other power below the maximum can also be found.
- Extracting full load-pull data and contours is instantaneously quick with the *power parameters* in MultiMatch.

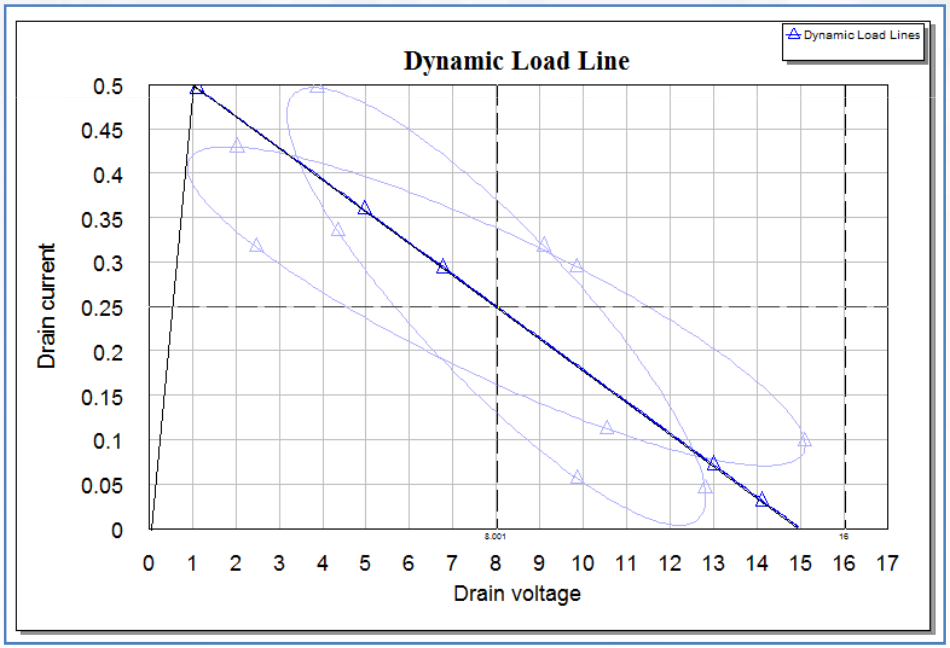

Figure 13. Tuning for optimum DLL

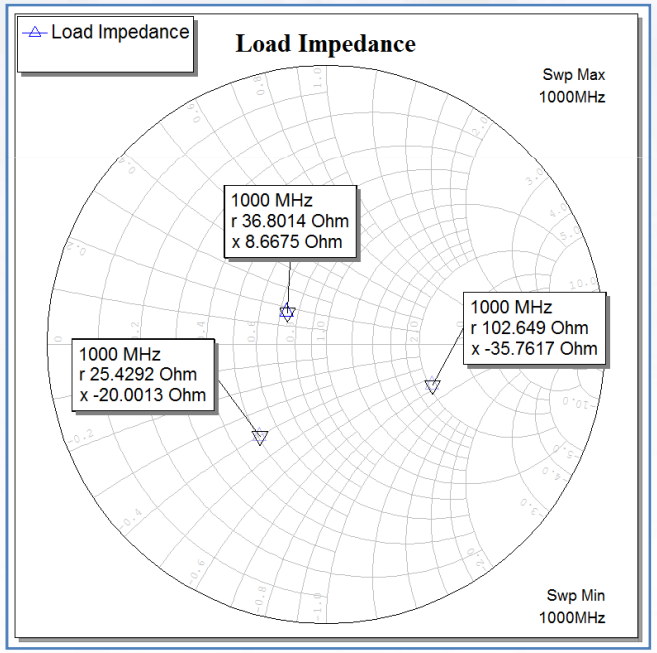

Figure 14. The load impedance corresponding to the optimum DLL

- But let's not forget what happened with the design of the amplifier discussed earlier.
- The results of the final design are presented in Figures 15 though 19 and they speak for themselves.

Figure 15. Photo of the 0.5-2.5GHz 50W amplifier

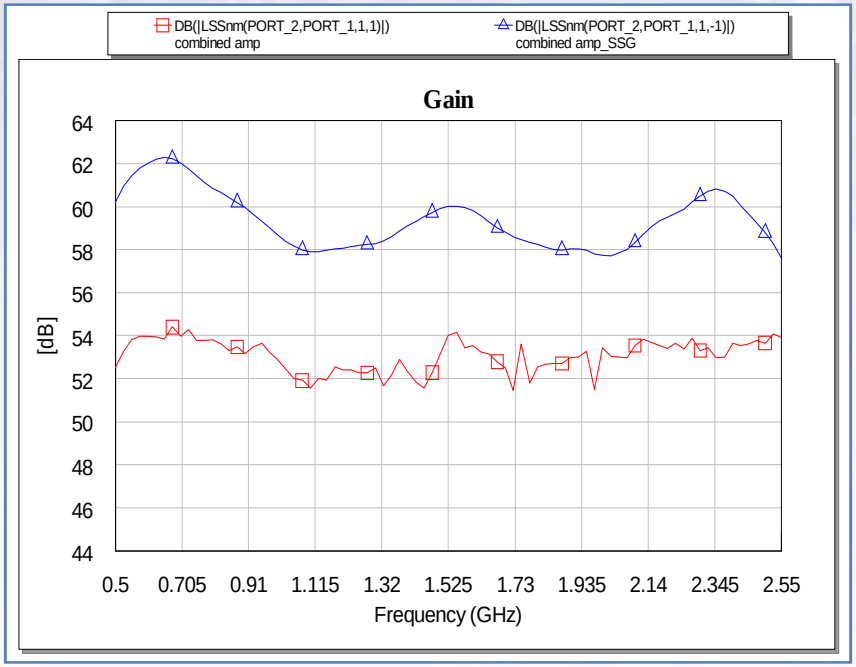

Figure 16. The simulated small-signal and large-signal power gain

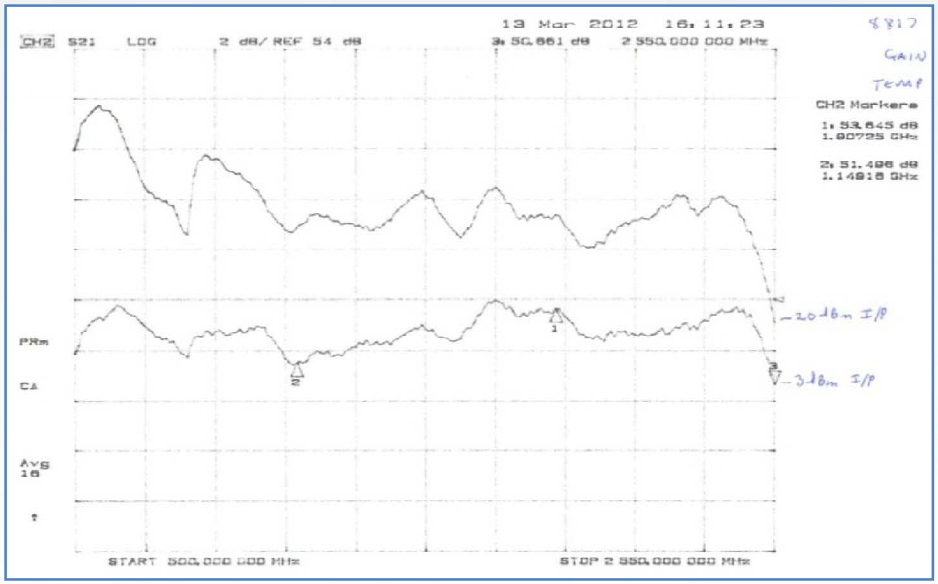

Figure 17. The measured small-signal and large-signal power gain

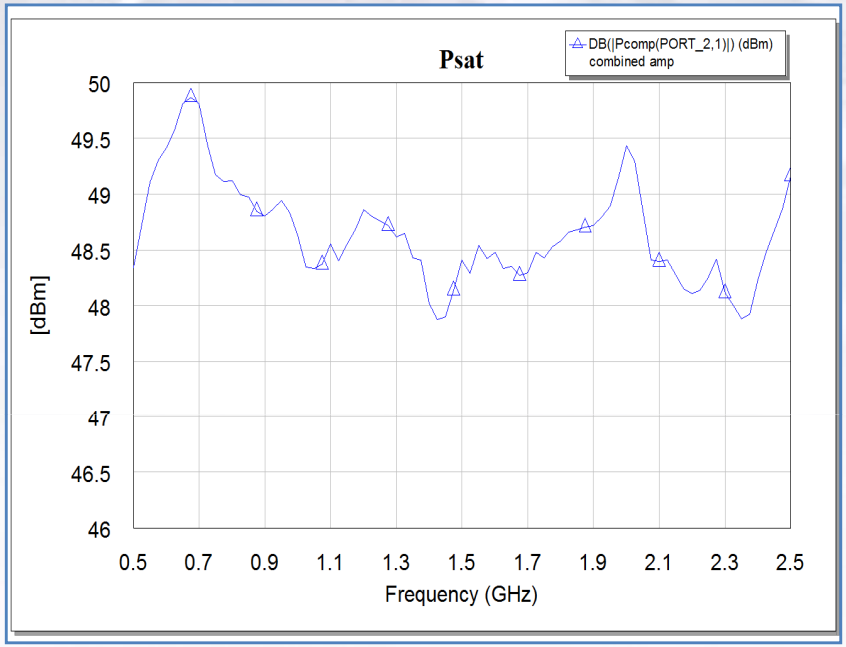

Figure 16. The simulated Psat

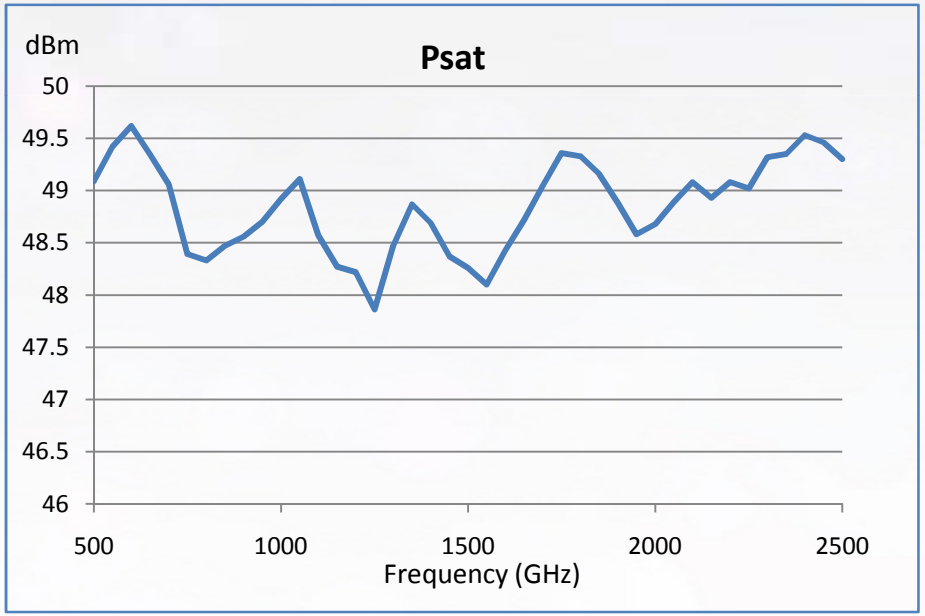

Figure 16. The measured Psat

Final comments

- A method was described for designing and simulating amplifiers for maximum power using harmonic balance simulation when the only available data are the *S*-parameters of the transistors.
- The method is widely applicable, from low-noise amplifiers to high power amplifiers, from narrowband to multi-octave bandwidth amplifiers, or everywhere where it is important to know and design for the power deliverable by any of the stages of an amplifier when non-linear transistor models are not available.
- It is very helpful even when the non-linear models are available.

- Pieter Abrie's *power parameters* approach is a fast and versatile method, but it exists only in MultiMatch Amplifier Design Wizard.
- If the *power parameters* method is incorporated in the general simulators it will compliment the described above method and, in general, dramatically enhance the design RF/microwave amplifiers.
- While it is desirable to incorporate the *power parameters* in the general-purpose simulators, the MultiMatch synthesis techniques and procedures are also required.
  - These are the only real-frequency and real-world synthesis techniques available in a commercial software product.
  - Their incorporation will provide unprecedented levels of productivity and creativity in the design of matching networks from inside the general simulators.

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To the providers of linear and non-linear models of RF/microwave transistors:

- Please provide access to the voltage and current across the intrinsic generator of the transistor models.
- It is obvious that this opens much deeper level of insightfulness and adds more versatility to the design methods and approaches.

1. Cripps, S.C., “A Theory for the Prediction of GaAs Load-Pull Power Contours”, *IEEE-MTT-S Int’l. Microwave Symposium Digest*, 1983, pp 221-223.
2. Steve C. Cripps, “GaAs FET Power Amplifier Design”, Matcom, Inc., Technical Note 3.2
3. Cripps, S.C., *RF Power Amplifies for Wireless Communications,* Artech House, 1999, ISBN 0-89006-989-I.
4. Abrie, Pieter L.D., *Design of RF and Microwave Amplifiers and Oscillators*, Artech House, 2009, ISBN 978-1-59693-098-8
5. *MultiMatch Amplifier Design Wizard*, Pretoria: Ampsa (Pty) Ltd.; http://www.ampsa.com.
6. Ivan Boshnakov, Anna Wood, Simon Taylor. “RF & Microwave Solid State Power Amplifier Design is a Speciality”, *ARMMS,* April 2012
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