

Power Amplifier Design using Discrete GaN Transistors – Extending Frequency Bandwidth

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Introduction

The design of power amplifiers for narrow frequency bandwidths is well understood and many designs, papers and application notes are available to support this. Proven techniques are utilised in order that these designs can be easily realised. But, when a design requires the bandwidth to be extended, such as that presented in this example from 2 to 6GHz, certain amplifier parameters are compromised. The power added efficiency may be degraded as well as the overall gain. The required output power may not be delivered and device stability may also be compromised as well as device linearity. In this paper, a design is presented, where the frequency bandwidth has been extended between 2 to 6GHz. The simulations performed and techniques used during the design process are discussed, in order to present a stable final design, with a focus on delivering the maximum available output power for the given bandwidth. But more importantly what compromises have had to be made in order for this to occur. The final design will be tested using CW signals.

The Design Process

FET Curve-DC Analysis

As with a typical narrowband power amplifier design, initial analysis on the device chosen for the design must be performed. These include measurements to determine the optimum DC load line, in order that the FET may be biased in its most linear region. A typical schematic to determine the DC load line is as shown in **Figure 1**. In this design the FET chosen has a typical V_d (drain voltage) range of up to 40V and a typical V_g (gate voltage) range operating down to -4.5V. These parameters are entered in to the schematic of **Figure 1**. The results of this DC sweep are shown in **Figure 2**.

From the plot of **Figure 2**, we can determine that the optimum area to bias the transistor for our design, where the available, drain voltage is 30V. The area circled in green is where we need to bias the transistor to ensure linear DC operation of the transistor. Operating in this region ensures the transistor is operating in a 'typical Class A' mode, whereby minimal distortion of the applied signal should occur. A marker (m1) placed at the top of the area, indicates the current drawn at the drain and the devices power consumption, for the applied value of V_g , in this case -2.3V at 30Vd. This is the minimum (negative voltage!) that we would like to apply at the gate during operation. However, -2.3V applied at the gate would exceed the transistors maximum power dissipation (35W at CW). Therefore this value must be backed off to ensure the transistor doesn't burn out. The ideal quiescent current (I_{dq}) is 200mA, for the chosen FET, therefore adjustment of the V_g , must be made

to ensure this happens. This means the device must be operated in class AB to ensure any power derating requirements are achieved.

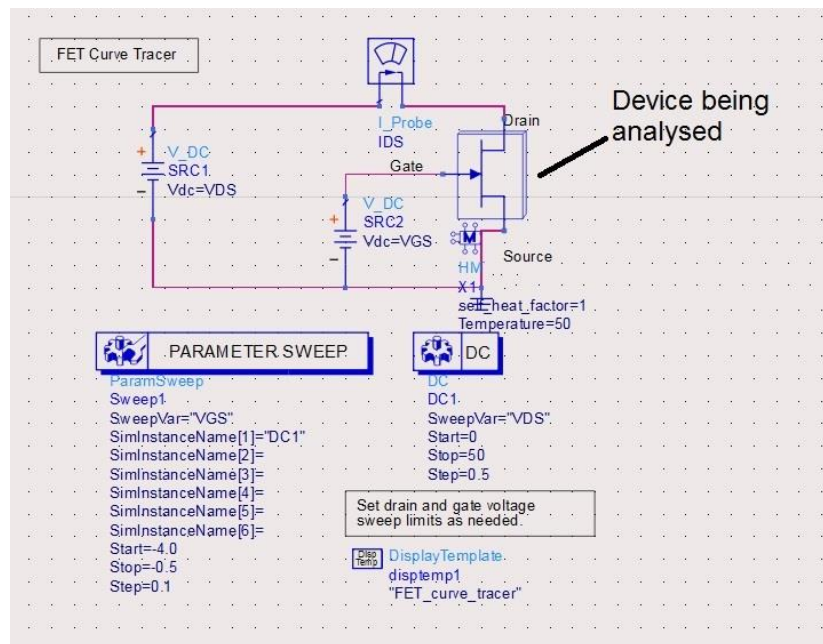
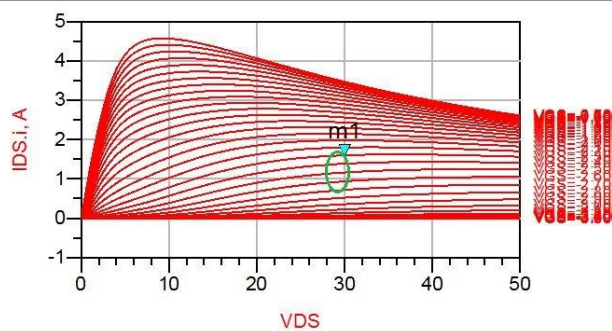


Figure 1 – DC Analysis of FET

FET Bias Characteristics

Use with FET_curve_tracer Schematic Template



Values at bias point indicated by marker m1.
Move marker to update.

m1
VDS=30.000
IDS,i=1.600
VGS=-2.300

Figure 2 – DC Analysis Results

FET Stability

The next stage of the design process is to perform some stability analysis on the FET. As the required operating frequency is from 2 to 6GHz, the transistor must be stable in operation down to DC, in order that it doesn't destroy itself without any signal or very low frequency signal applied at its input. For the type of transistors used in power amplifier designs, the low frequency gain is usually very high, compared to the rest of the devices operating bandwidth. Therefore, steps must be taken to ensure these areas of the band are controlled, without being too detrimental to the rest of the operating band. The initial schematic for this is shown in **Figure 3**. The stability is measured using 4 methods within ADS and the initial plot is shown in **Figure 4**.

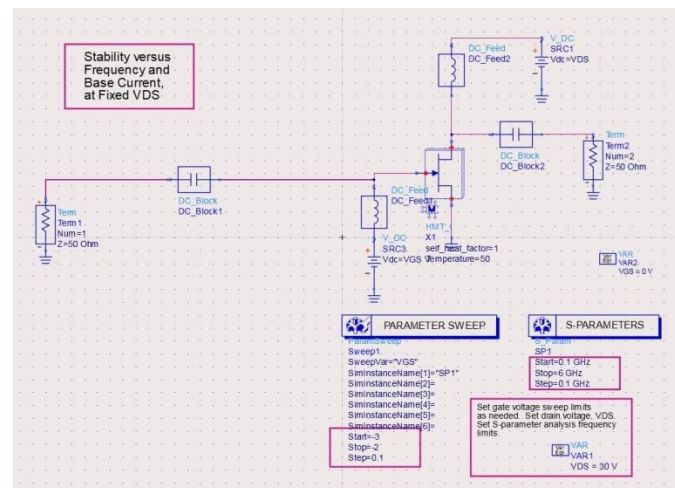


Figure 3 – FET Stability Analysis Schematic

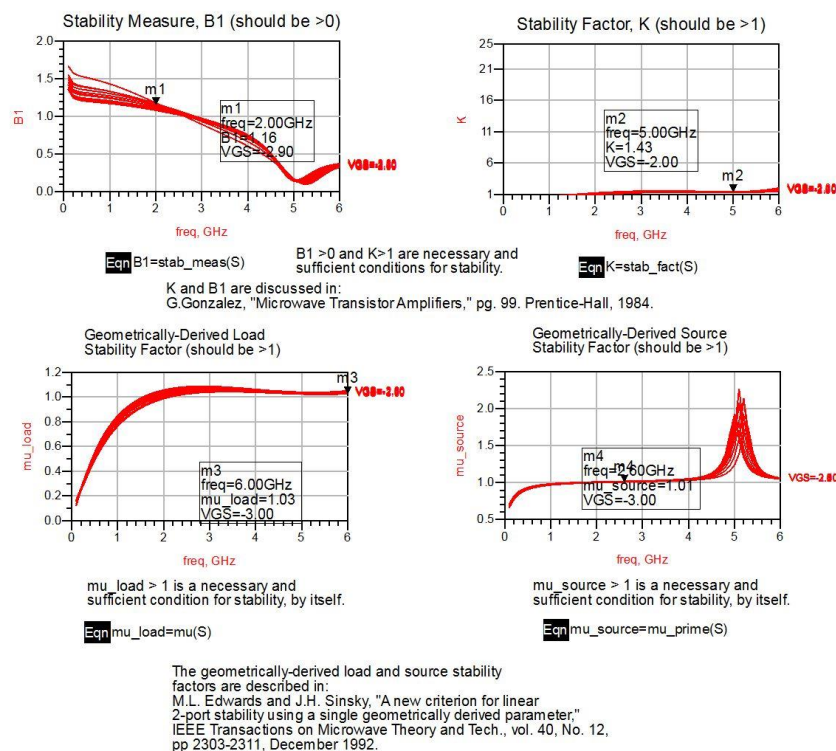


Figure 4 – FET Stability Analysis Schematic, Initial Plot

Stability versus Frequency and Base Current, at Fixed VDS

Stability analysis is performed at a fixed VDS. The schematic shows a common-source MOSFET amplifier with the following components and parameters:

- Gate Bias Network:** A voltage divider consisting of a series resistor $R7$ and a shunt capacitor $C20$ to ground. The gate voltage is $V_{GS} = 3.0V$. The MOSFET model is `MOSFET_180_01`.
- Gate Matching Network:** A series capacitor $C13$ and a shunt resistor $R6$ to ground. The gate voltage is $V_{GS} = 3.0V$.
- Drain Matching Network:** A series capacitor $C21$ and a shunt resistor $R8$ to ground. The drain voltage is $V_{DS} = 5.0V$.
- Load Network:** A series capacitor $C22$ and a shunt resistor $R9$ to ground. The load voltage is $V_{L} = 5.0V$.

PARAMETER SWEEP

Parameter sweep is performed on the gate voltage V_{GS} . The sweep range is from 3.0V to 5.0V, with a step size of 0.1V. The sweep is performed at a fixed VDS of 5.0V.

S-PARAMETERS

S-parameter analysis is performed at a fixed VDS of 5.0V. The analysis is performed at a frequency of 1 GHz, with a step size of 0.1 GHz. The analysis is performed for a gate voltage V_{GS} of 3.4 V.

Stability Measure, B1 (should be >0)

Graph 1: B1 vs freq, GHz. The y-axis ranges from 0.0 to 1.0. The x-axis ranges from 0 to 6 GHz. A box indicates parameters for curve m1: $m1$, freq=2.00GHz, $B1=955$, $VGS=-2.00$. A red curve shows B1 starting at 0, peaking at ~0.95 at 2 GHz, and then decreasing. A red arrow points to the right with the text $VGS=-2.00$.

Stability Factor, K (should be >1)

Graph 2: K vs freq, GHz. The y-axis ranges from 0 to 25. The x-axis ranges from 0 to 6 GHz. A box indicates parameters for curve m2: $m2$, freq=5.00GHz, $K=1.47$, $VGS=-2.00$. A red curve shows K starting at 0, peaking at ~22 at 0.5 GHz, and then decreasing. A red arrow points to the right with the text $VGS=-2.00$.

Geometrically-Derived Load Stability Factor (should be >1)

Graph 3: μ_{load} vs freq, GHz. The y-axis ranges from 1.0 to 1.5. The x-axis ranges from 0 to 6 GHz. A box indicates parameters for curve m3: $m3$, freq=5.00GHz, $\mu_{load}=1.03$, $VGS=-3.00$. A red curve shows μ_{load} starting at 1.0, peaking at ~1.45 at 1.5 GHz, and then decreasing. A red arrow points to the right with the text $VGS=-3.00$.

Geometrically-Derived Source Stability Factor (should be >1)

Graph 4: μ_{source} vs freq, GHz. The y-axis ranges from 1.0 to 2.5. The x-axis ranges from 0 to 6 GHz. A box indicates parameters for curve m4: $m4$, freq=2.60GHz, $\mu_{source}=1.12$, $VGS=-3.00$. A red curve shows μ_{source} starting at 1.0, peaking at ~2.3 at 5 GHz, and then decreasing. A red arrow points to the right with the text $VGS=-3.00$.

Equations and Notes:

- $\text{Eqn } B1 = \text{stab_meas}(S)$
- $\text{Eqn } K = \text{stab_fact}(S)$
- $\text{Eqn } \mu_{load} = \mu(S)$
- $\text{Eqn } \mu_{source} = \mu_{\text{prime}}(S)$

Notes:

- $B1 > 0$ and $K > 1$ are necessary and sufficient conditions for stability.
- K and $B1$ are discussed in: G.Gonzalez, "Microwave Transistor Amplifiers," pg. 99, Prentice-Hall, 1984.
- $\mu_{load} > 1$ is a necessary and sufficient condition for stability, by itself.
- $\mu_{source} > 1$ is a necessary and sufficient condition for stability, by itself.

References:

- M.L. Edwards and J.H. Sinsky, "A new criterion for linear 2-port stability using a single geometrically derived parameter," IEEE Transactions on Microwave Theory and Tech., vol. 40, No. 12, pp 2303-2311, December 1992.

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Load-Pull

The next stage of the design is probably the most difficult of the early design phase. Load-pull analysis must be performed to determine what the optimum load and source impedances need to be, to ensure good power delivery at the transistor's output. Normally, for a narrowband design, the load-pull analysis is performed at the band centre. However, for a broadband amplifier, this operation needs to be performed at intervals across the operating frequency band, from 2GHz to 6GHz. The frequency points chosen were 2, 3, 4, 5 and 6GHz, i.e. points at 1GHz intervals. More points can be chosen. However, this process of the design requires lots of computing resources and can take a while, depending on how the harmonic measurements are defined, i.e. the more harmonic content that needs to be measured, the slower the analysis.

It's worth noting, that load-pull analysis should also be performed for the frequencies outside of the operating bandwidth. This is not to ensure we have the optimum impedances for good power delivery, but to determine the optimum impedances to attenuate and make stable, our design at particularly the lower frequencies. In this design instance, they were also performed at 1.5GHz and 500MHz.

The schematic shown in **Figure 7** was used throughout the design and manipulated for each of the project design frequencies.

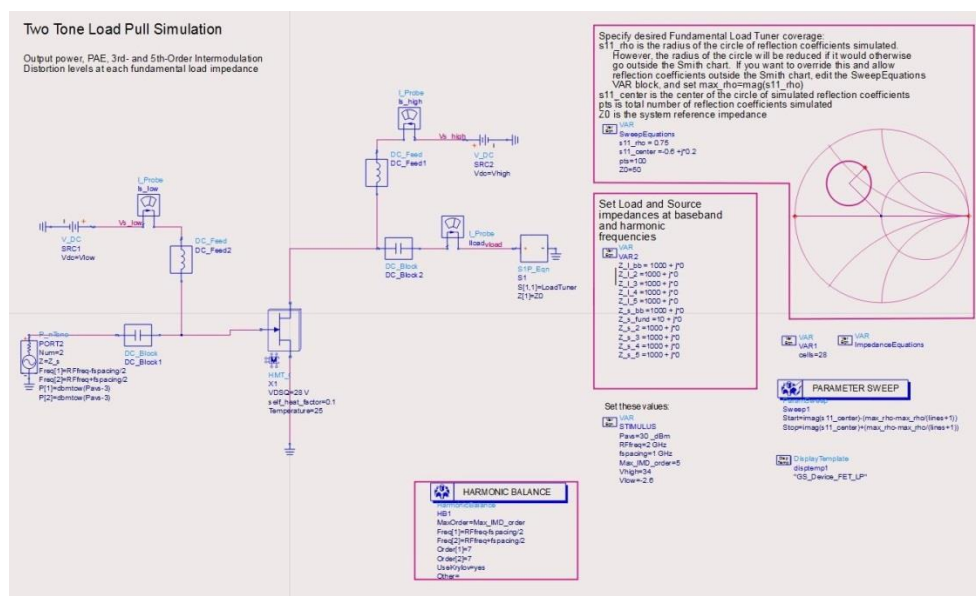


Figure 7 – Load-Pull Schematic

The data generated from the load-pull analysis typically generated within ADS, is in the format shown in **Figure 8**. The area of particular interest is marked in the blue circle. Moving the marker within the region marked in red, starred lines, adjusts the PAE (power added efficiency), delivered power in dBm, harmonic levels (you may not need these) and importantly, the required impedance to meet these values. The impedances are stated in polar format. This helps to determine whether the actual designed elements need to be inductive or capacitive, relative to where they are on the Smith chart.

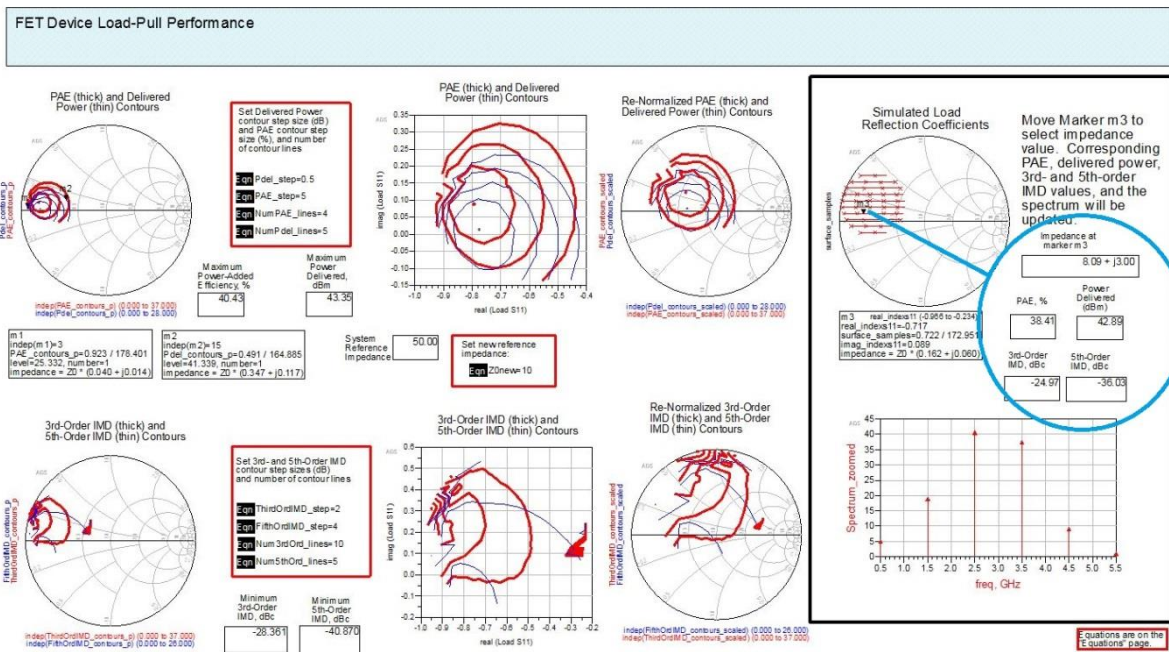


Figure 8 – Load-Pull Analysis Data

Schematic Build

For each frequency, the optimum impedance value is then converted to a real impedance value, in Ohms. The polar impedance values will still be needed. However, at this point we can start to build our initial schematic, as in **Figure 9**, using electrically ideal elements. Each element, for our design, is configured to the optimised impedances. The out of band impedances may not be required, but still worth noting, in case the final design is not stable enough when placed back into the FET stability analysis. The ideal elements are made to be 'tuneable'. This is quite useful, as the calculated impedances will need adjustment when they are all placed together within the schematic. The ideal impedance at one frequency may not be ideal at a different frequency, so again the impedances will need some tuning. However, using the tuneable elements, including the gate voltage (Vg), it's easier to perform this within the schematic, **Figure 10**.

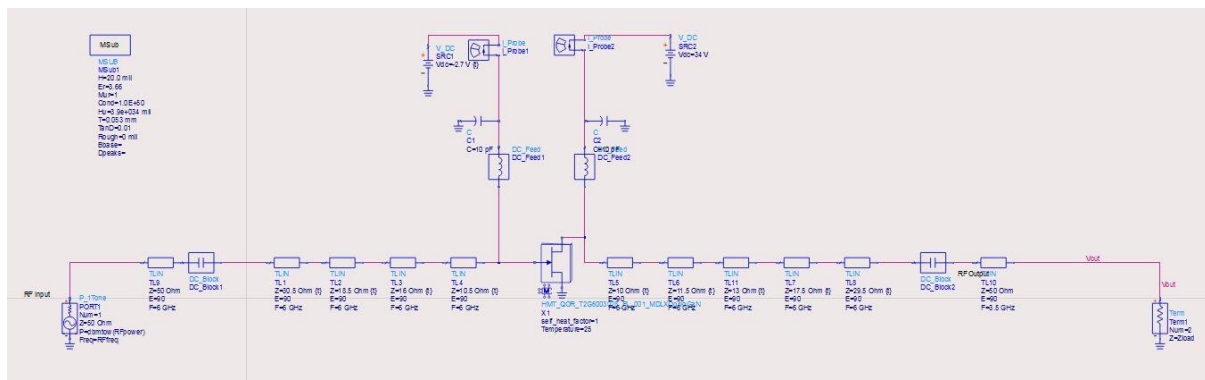


Figure 9 – Initial Schematic

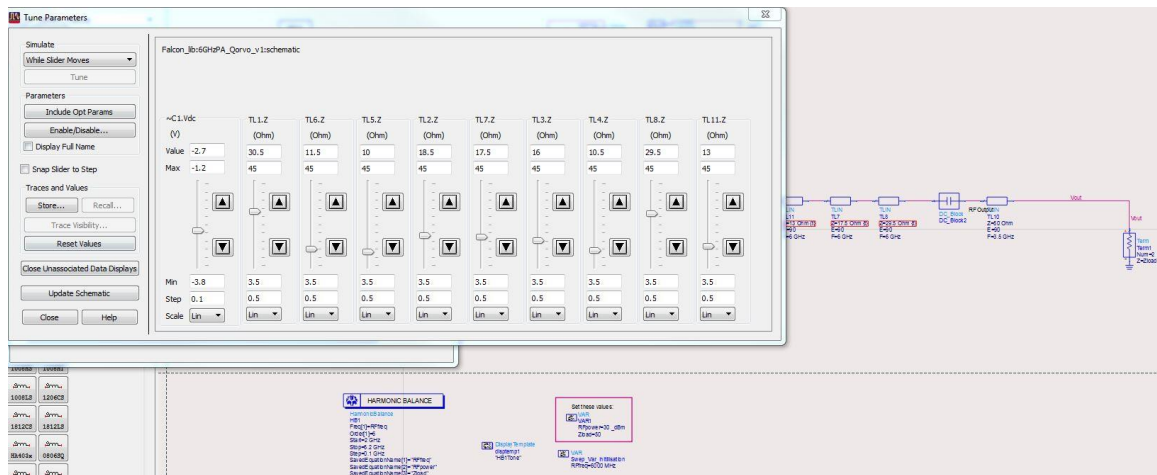


Figure 10 – Tuning Elements

As we are designing to achieve power, a plot of the simulated output power over frequency can be obtained, **Figure 11**. **Figure 11** is the initial plot, which isn't very flat over the frequency range. The FET chosen for this design can deliver 30W (44.7dBm), pulsed at 10% duty cycle, so the CW data shown in **Figure 11**; isn't too bad in that respect. The tuning elements are then adjusted to achieve a flat a response as possible, or a slope added. Additional impedance transform elements are added or taken away. It must be remembered that the greater the number of elements, the greater the loss is, through the circuits at the FETs input and output.

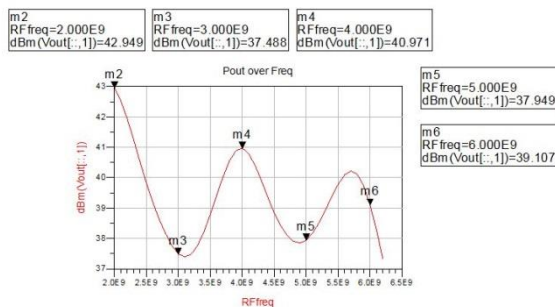


Figure 11 – Initial Pout over Frequency

The schematic is gradually built up, with any additional components, including the gate and drain biases, which are simulated along with schematics drawn up for these. Whilst these are drawn separately, a flat schematic of the design is shown in **Figure 12**. Only the final iteration of the design is shown here, along with the final simulated results for a single FET, in **Figure 13**.

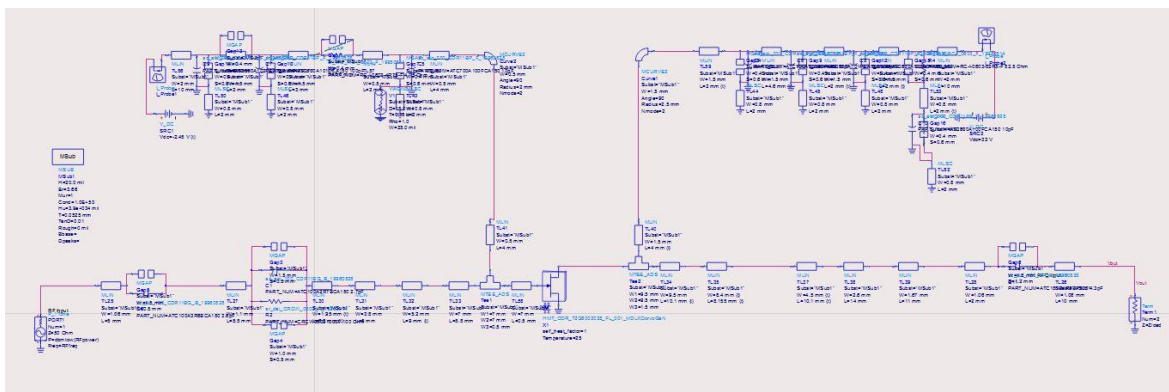


Figure 12 – Final Schematic for Single FET

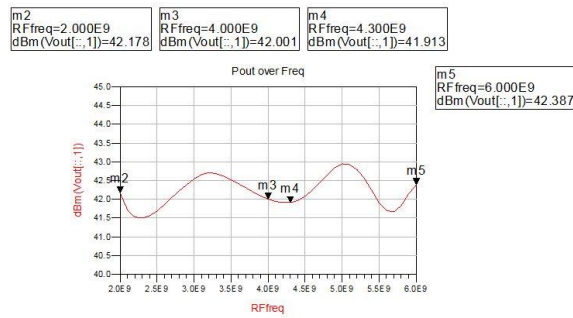


Figure 13 – Single FET Pout over Frequency

The final design schematic is then put back into the FET stability analysis circuit, to ensure that all the circuit elements have not adversely affected the FETs stability.

Balanced Design

The desire for further power led to a balanced design, where the model is shown in **Figure 14**. This schematic contains other components added to the design, in order to achieve the balanced design. Two 90-degree hybrid couplers were utilised and s-parameter models for these are included within the non-linear model. The simulated power output and current drawn is shown in **Figure 15**.

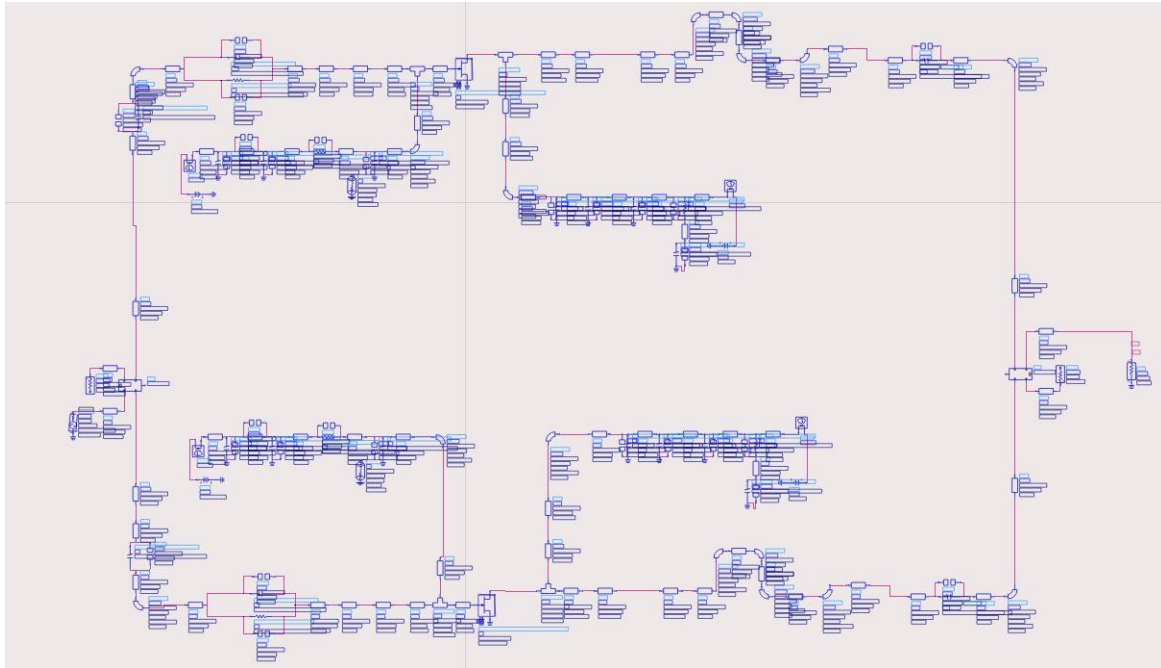


Figure 14 – Balanced FET Design

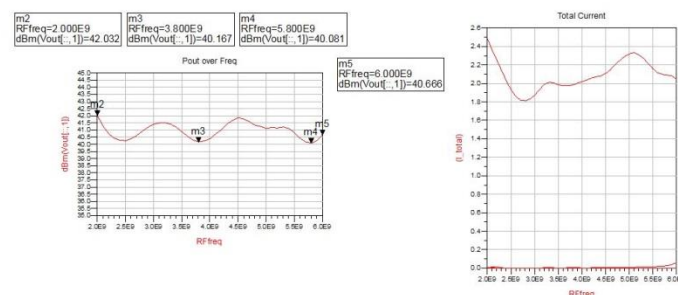


Figure 15 – Power Output with Drain Currents for both FETs

The simulated data shows we have achieved just over 41.5dBm (14W) power output, nominally across the 2-6GHz range, with a total I_{ds} of around 2.1A, using a 30V DC supply. The simulation is driven using a power input of 27dBm (0.5W). We have achieved a PAE (power added efficiency) of 21.43% nominally across the range. The nominal gain is around 14.5dB for both FETs.

This means that around 78.5% of the input power is lost as heat. The power dissipated by the devices is $(63W + 0.5W) - 14W = 48.5W$. Therefore each device dissipates $48.5W/2 = 24.25W$ which is below the device's specified maximum 35W at CW.

Steps will need to be taken to ensure that the FETs are not driven with too high an input power and/or to reduce the gate bias voltages during test. A good thermal platform to allow the FETs to dissipate the heat to; will also be required.

Prototype Circuit

A prototype of the balanced design was manufactured and placed on a heatsink, capable of sinking in excess of 200W, along with a large fan. The layout was done in ADS, shown in **Figure 16**, with the actual circuit shown in **Figure 17**. The two FETs were mounted directly to an aluminium base plate, without the use of a thermal interface material, i.e. no thermal paste, solder or graphite sheet. The base plate was hand finished prior to mounting, to ensure as smooth a surface as possible, to enable direct mounting to take place.

The measured Pout and Current data are shown in **Figure 18**.

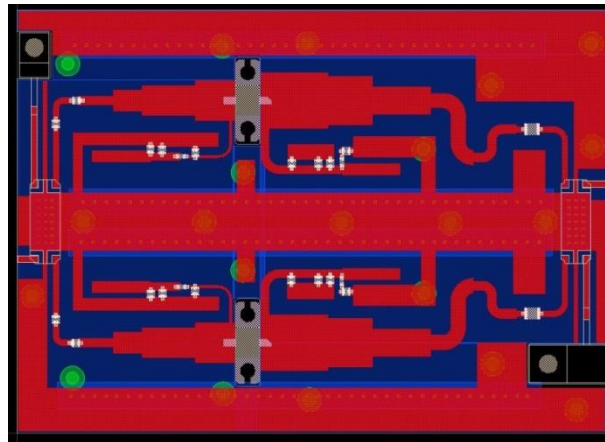


Figure 16 – ADS Layout

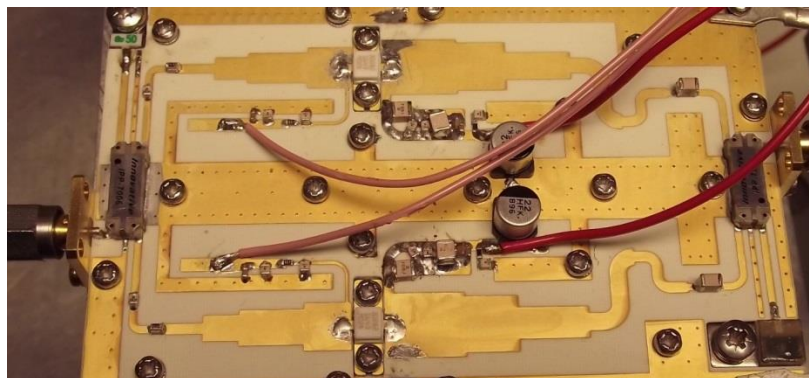


Figure 17 – Prototype Circuit in Test Jig

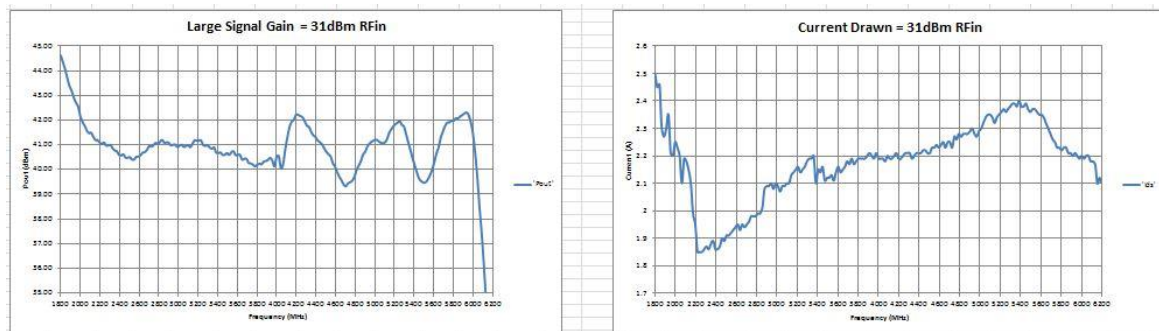


Figure 18 – Measured Data from Prototype

Conclusion and Further Work

We have designed a power amplifier that operates from 2-6GHz, capable of generating approximately 41.5dBm (14W) across the band....Just!

This has been achieved using proven load-pull, FET stability and DC analysis, just as would have been applied to a narrow band design. Only here, the load-pull techniques were repeated over a number of frequencies. The Keysight ADS software, allowed us to use sliders, in order that we could 'tune' each impedance element, to ensure that individual impedances derived for a single frequency, were then not too adversely affecting other frequencies. Where this was the case, other elements were added or removed and further tuning performed. Whilst this was iterative, the majority of this element of the design was achieved within a day.

The main downside to extending the bandwidth using the chosen FETs were; that the PAE was too low. Greater than 30% would have been good across the band. This resulted in too much heat being generated as wasted energy, requiring a large heatsink to ensure the FETs didn't burn out (although they still got very hot!). This also meant that we had to drive the PA harder, 31dBm actual power versus the modelled 27dBm. This in turn, means we would likely kill the FETs had we continued testing, as this would have resulted in the FETs getting hotter and hotter, as we tried to achieve more power.

The overall gain was a reasonable 10.5dB. A good target would have been around 10dB. We achieved a little more.

Given the achieved results, it's likely that we would choose a different FET, to achieve more power. Preferably a device that was better able to deliver CW power than pulsed.

Acknowledgements

Keysight ADS (Advanced Design System) for the simulation and analysis software,
<https://www.keysight.com/find/eesof-technicalreference>

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