Intrinsic Cree GaN HEMT Models allow more accurate waveform engineered PA designs

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Summary

- Advantages of GaN HEMT Technology
- Overview of Large-Signal GaN HEMT Models
- Waveform Engineering of GaN HEMT PA's
  - ❑ Actual Current Generator and Drain Voltage Waveforms
- Example of Harmonically terminated narrow band PA
  - ❑ Effect of parasitics in packaged transistors on true device waveforms
- Example of Determining VSWR Robustness for a Single-Ended PA
- Example of Class F Doherty PA
  - ❑ Carrier and Peaker Waveforms/Load-lines at Crest and 7.5 dB OBO
- Conclusions

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Advantages of GaN HEMT Technology

Summary of GaN HEMT Advantages

- Wide bandgap semiconductor materials like GaN HEMTs have potential to operate at power densities many times higher than Si-LDMOS, GaAs FET, and silicon carbide (SiC) devices
- High power density is an important factor for high power devices enabling smaller die sizes and more easily realized input and output matching networks
- GaN HEMTs have other advantages:
  - High breakdown voltages (200+ volts)
  - High saturated electron velocity
  - Good thermal conductivity
  - Low parasitic capacitances and low turn-on resistances
  - High cut off frequencies
- Proven high reliability (>10 million hours) and excellent field FIT rates (<10)

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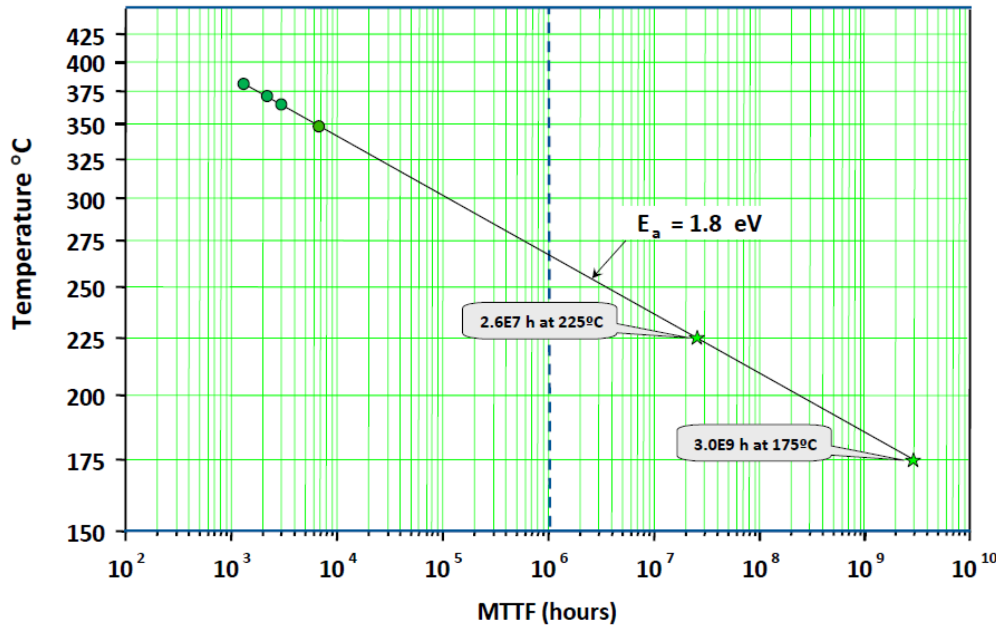
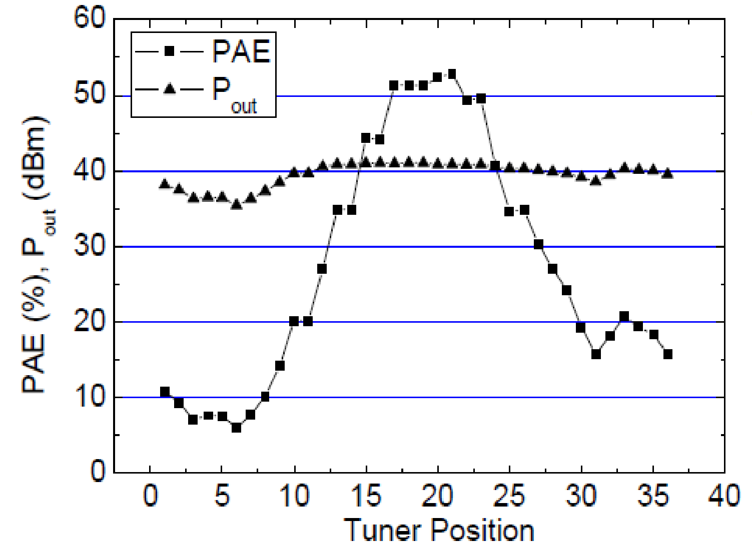
Reliability and VSWR Robustness of GaN HEMTs



MTTF at 225 deg C Channel Temperature is >20 million hours

Robustness data from Fraunhofer Institute



Most GaN transistors are specified to withstand a 10:1 output mismatch at fully rated output power. Worst case in example above shows PAE of 7% and a maximum channel temperature of 278°C but device does not fail

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Overview of Cree Large-Signal GaN HEMT Models

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Models for GaN HEMTs

- Large signal models are available for all Cree GaN HEMT transistors
  - Agilent's ADS and AWR's Microwave Office are fully supported
- Highly accurate with excellent history of design pass successes
- Enable complete DC and RF simulations
- Models include self-heating (presently single-pole thermal time constant)
- Model library is regularly updated
- Latest model library revision uses Verilog A code and includes 0.4μm and 0.25μm gate length transistor models
- 6 port capability is being added to all models so that true "intrinsic" drain currents and voltages at the current generator are available
  - In addition C_{DS} and package parasitics are "removed"
- Many marketing reference designs can be provided

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Models for GaN HEMTs

- Equivalent-circuit based approach
  - Relatively simple extraction
  - Process sensitive based on individual elements
  - Simple implementation using commercial harmonic balance simulators
- Significant historical information for model basis and validation
- Non-linearity introduced as required by element
  - Drain current source is dominant non-linearity
  - Gate current formulation includes breakdown and forward conduction
  - Voltage variations of parasitic capacitances derived from charge formulations
- Model data fit extends over drive, frequency, bias, and temperature
- Many hundreds of successful hybrid and MMIC designs

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Model Schematic

R
R3
R=0.01 Ohm

pncap3
X15
sc=sc
scf=scf
cg1=cgd pF
cg2=0.6
cg3=0.1
vgg0=-21 V

SDD6P
SDD6P1
I[1,0]=(vg)/5e8
I[2,0]=id1
I[3,0]=(_v3)*gdsc
I[4,0]=(_v4)*gmc
I[5,0]=-vd*idt
I[6,0]=(vdf)/5e4
C[1]=
Cport[1]=

Drain current

SRL
SRL4
R=(rd/(sc*scf)) Ohm
L=(ld/sc+ld1/(sc*scf)) nH

SRL
SRL1
R=(rg/sc+rg1/(sc*scf)) Ohm
L=(lg/sc+lg1/(scf*sc)) nH

Port
P1
Num=1

R
R5
R=1e6 Ohm

pncap3
X12
sc=sc
scf=scf
cg1=cgs pF
cg2=cg2
cg3=cg3
vgg0=vgg0 V

VCVS
SRC1
G=1

C
C7
C=1.0 uF

C
C9
C=(cds*sc*scf) pF

Port
P2
Num=2

R
R6
R=1e6 Ohm

R
R1
R=(ri/(sc*scf)) Ohm

Port
P4
Num=4

Port
P5
Num=5

vd1g

Thermal resistance

SRL
SRL3
R=(rs/(sc*scf)) Ohm
L=(ls/sc) nH

R
R2
R=rth Ohm

C
C8
C=30.0 nF

Port
P8
Num=8

- Based on 13-element MESFET model (Fager-Statz)
- ADS version shown using non-linear equation-based elements

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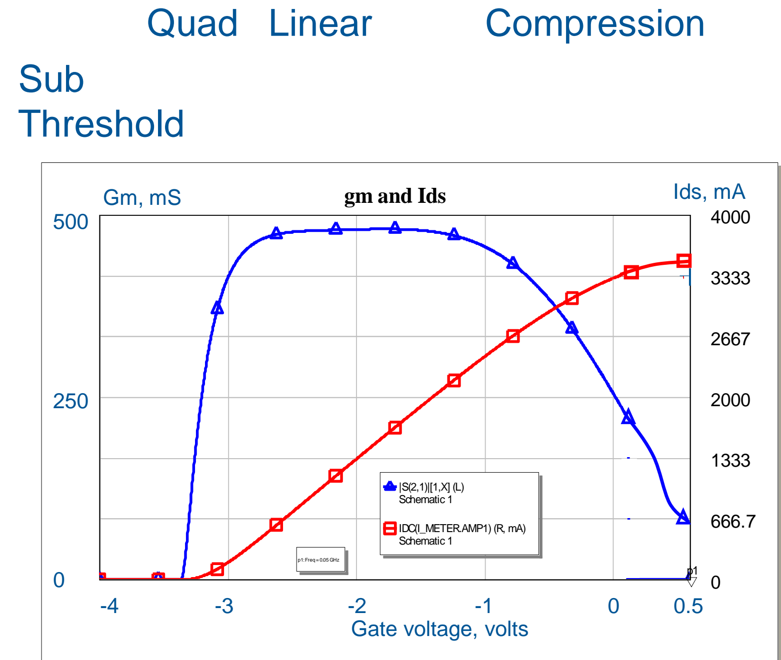
More details on Cree GaN HEMT Model

- Most FET models implement a gate current-control characteristic that transitions from the sub-threshold region to the linear gate control region directly, without treating the intermediate region, called the quadratic region. Fager et al. implemented an equation and new parameters to fit the quadratic region. This leads to better agreement with measured IMD and other nonlinear characteristics.
- Gate charge is partitioned into gate-source and gate-drain charge. Each charge expression is a function of both V_{DS} and V_{GS}. Using charge partitioning, it is possible to fit most GaN HEMT capacitance functions and observed charge conservation.



Blue is DC transconductance
Red is drain current

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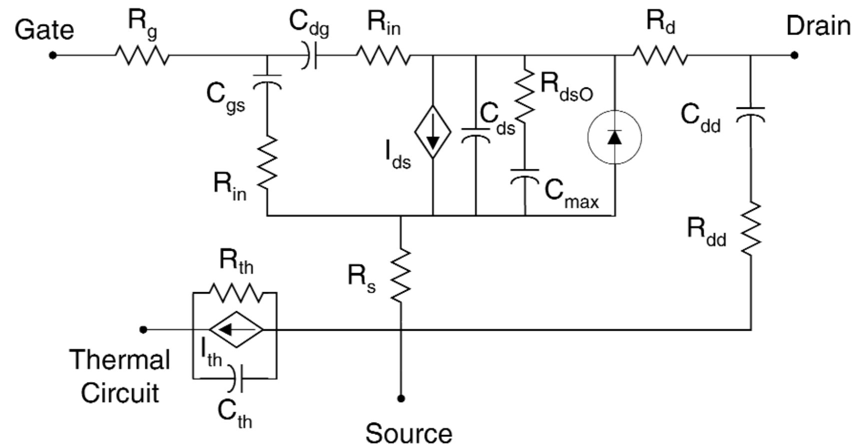
More details on Cree GaN HEMT Model



- The model includes new capacitance functions as well as modeling of the drain-source breakdown and self heating.
- The model has four ports, with the extra port providing a measure of the temperature rise. The voltage between the external thermal circuit port and the source node is numerically equal to the junction temperature rise in degrees C. This occurs because the current source in the thermal circuit is numerically equal to the instantaneous power dissipated in the FET and the resistance, R_TH is numerically equal to the thermal resistance. The RC product of the thermal circuit is the thermal time constant.
- The model addresses the sharp turn-on knee in GaN HEMTs leading to the accurate prediction of IMD sweet spots in Class A/B operation.

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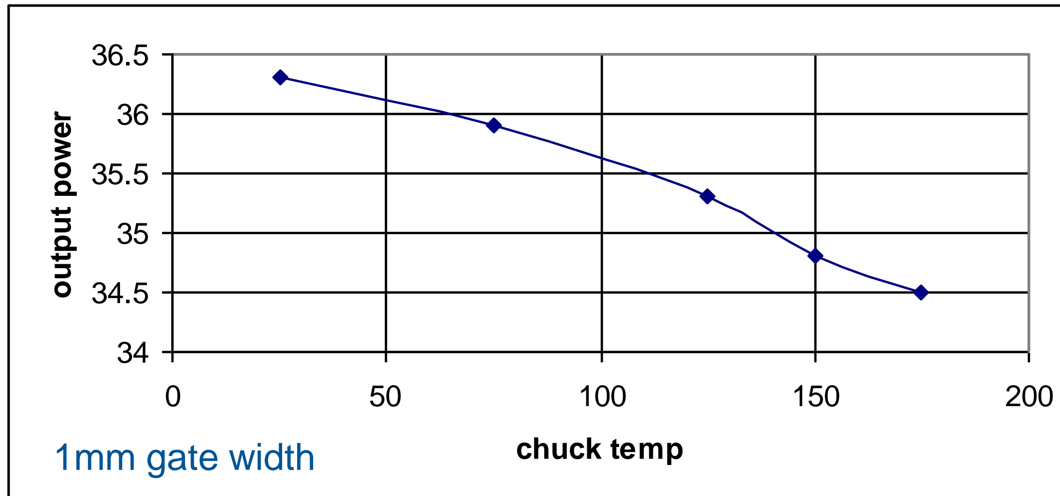
Temperature Dependence – Self-heating



- Drain current is only temperature dependent model element
- Drain current scales to provide -0.1 dB/10°C reduction in power for current-limited load-line
- Self-heating included using a thermal resistance – calculated from finite element analysis of die and package.
- Thermal performance due to package needs to be included where appropriate

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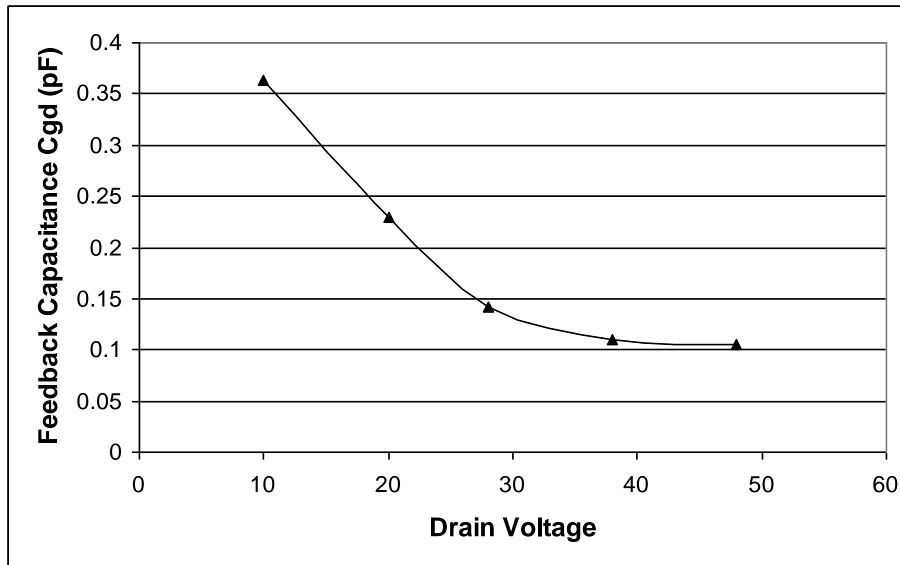
Feedback Capacitance - C_{GD}



- Feedback capacitance is a strong function of drain voltage
- Inclusion of this effect necessary to fit small-signal data
- Non-linearity changes harmonic generation from the model – effects efficiency and linearity predictions
- Output Capacitance C_{DS} is linear – no voltage dependence (weak anyway)

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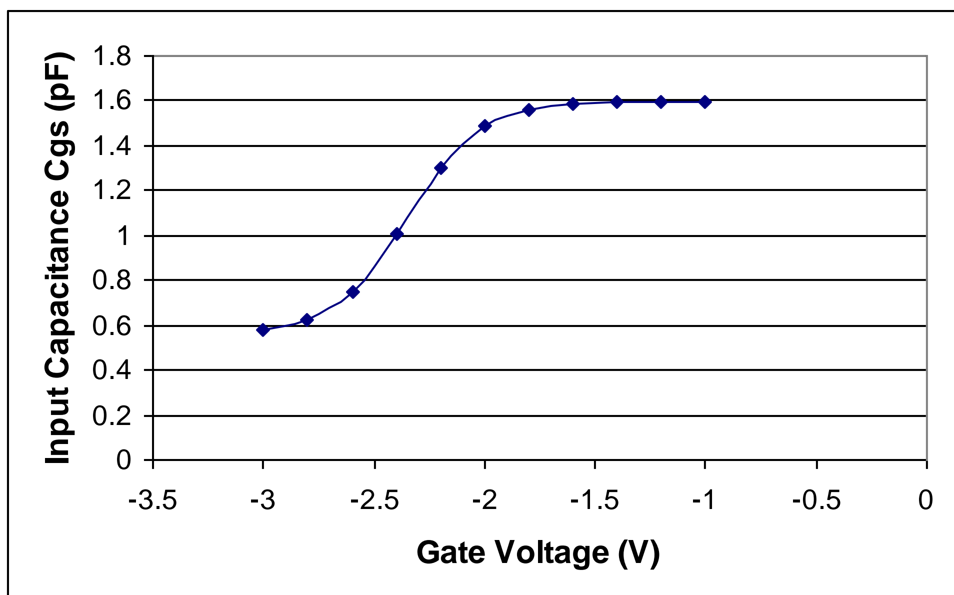
Input Capacitance - C_{GS}



- Input capacitance is a strong function of gate voltage
- C_{GS} is also a function of drain voltage, but this non-linearity is not included at present
- The gate-voltage non-linearity also effects model's harmonic generation

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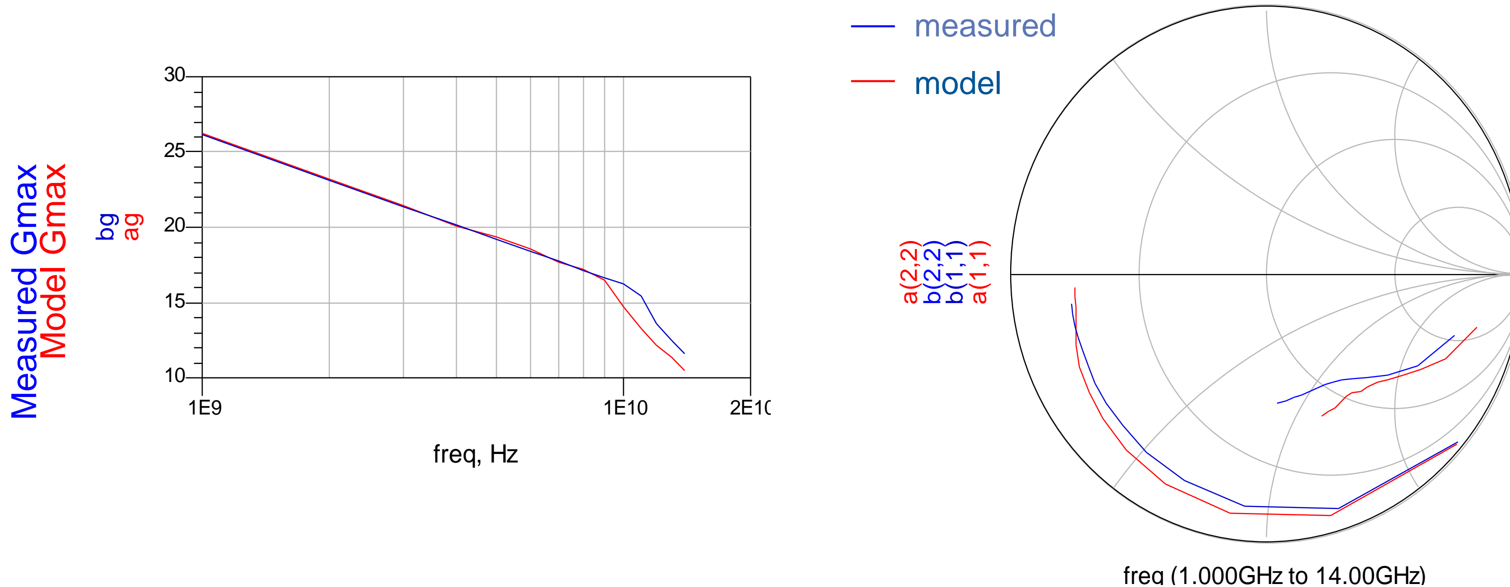
GaN HEMT Model - Small-Signal



- On-wafer S-parameters of 0.5 mm HEMT – 25°C baseplate
- Major challenge of modeling for high power circuits – scaling from reasonable test cell to large periphery output stages – successfully implemented for scaling factors >100:1
- Non-linear model fits small-signal parameters over a range of bias voltages
- All measurements performed using 1% duty cycle, 20μs pulsed bias to control thermal effects

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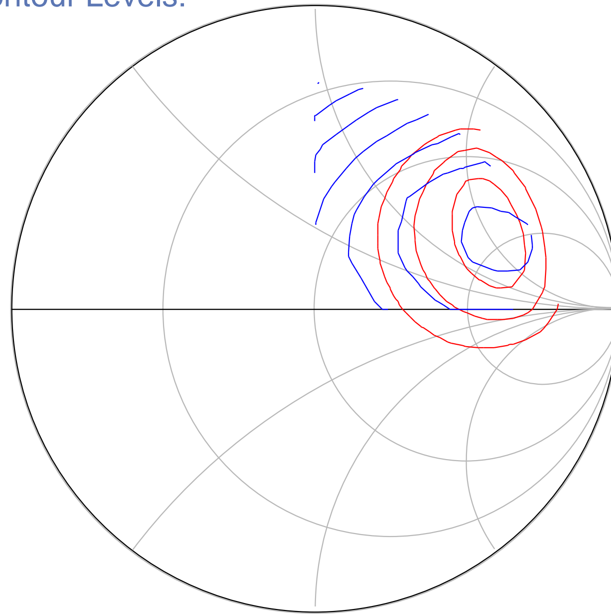
GaN HEMT Model - Large-Signal



- On-wafer load-pull of 0.5 mm HEMT
- Measured at 3.5 GHz, V_{DS}=28V, Id~25%IDSS, 25°C chuck temperature
- PAE contours not used for modeling due to sensitivity to harmonic loading
  – PAE verified using hybrid amplifier measurements

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Waveform Engineering of GaN HEMT PA's

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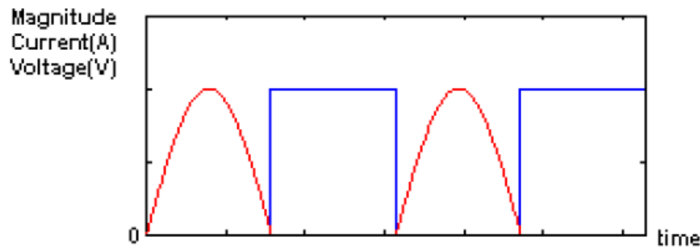
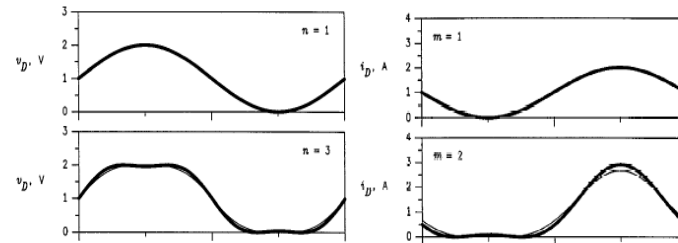
Summary

- Depending on the Class of amplifier being designed the drain voltage and current waveforms of an RF driven GaN HEMT need to be in exact anti-phase for maximum DC to RF conversion efficiency
- In many cases optimum efficiency will be provided when the voltage is a square wave and the current is a half sine-wave in anti-phase (Class F) or the voltage is a half sine-wave and the current is an anti-phase square wave (inverse Class F)
- Perfect half-sinusoids and square waves require an infinite number of signal harmonics
- Practically 3 harmonics is a limit both from device physics as well as amplifier realization viewpoints



Ideal Class F Red is Current



"Practical" Class F (3 harmonics)

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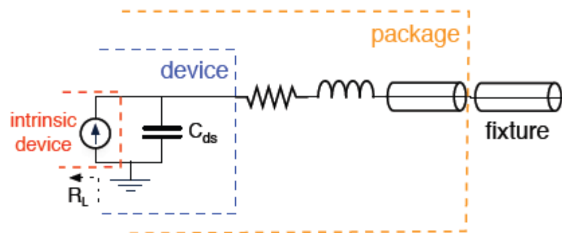
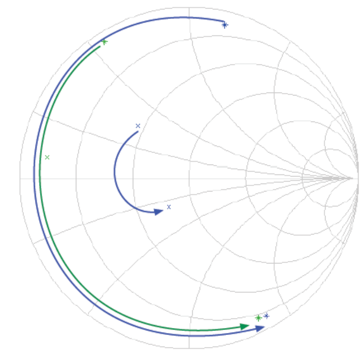
Waveforms at the Current Generator Plane

- In many cases where packaged GaN HEMTs are being employed in PA designs the waveforms presented at the package planes DO NOT REPRESENT the waveforms at the actual transistor current generator
  - Package parasitics etc. effectively provide impedance transformation and phasing networks (with their own losses etc.) to the true transistor current generator plane.
  - Attempts (some successful) have been made to “de-embed” package equivalent circuits, die level capacitive parasitics etc. from the large-signal models provided by some of the GaN HEMT vendors
  - Cree is now deploying new large-signal transistor models, with a total of 6 ports (gate, drain, source, current generator, drain voltage and channel temperature sense) providing a true “intrinsic” model





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Example of Harmonically Terminated Narrow Band PA

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High Efficiency S-Band Radar PA

- 3 Harmonic Tuned 120 watt PA utilizing Cree CGH40120F packaged transistor
- Ideal harmonic tuners used on input and output of device. Quiescent Drain Current set to 1A at a drain voltage of 28 volts
- “Intrinsic” 6 port model used

HBTUNER2
ID=TU2
Mag1=0.89
Ang1=-168.1 Deg
Mag2=1
Ang2=206.5 Deg
Mag3=0.9753
Ang3=-41.56 Deg

V_PROBE
ID=VP1

I_METER
ID=AMP2

DCVS
ID=V1
V=-2.86 V

CGH40120F_R6_LL
ID=X1
tcase=25
crth=1.5

3:Bias

PORT
P=2
Z=50 Ohm

3:Bias

I_METER
ID=AMP3

V_METER
ID=VM2

DCVS
ID=V2
V=28 V

PORT_PS1
P=1
Z=50 Ohm
PStart=0 dBm
PStop=42 dBm
PStep=1 dB

HBTUNER2
ID=TU1
Mag1=0.9537
Ang1=-161.9 Deg
Mag2=0.8104
Ang2=-132.2 Deg
Mag3=0.9982
Ang3=111.4 Deg

I_METER
ID=AMP1

V_METER
ID=VM1

Intrinsic Voltage Meter

Intrinsic Current Meter

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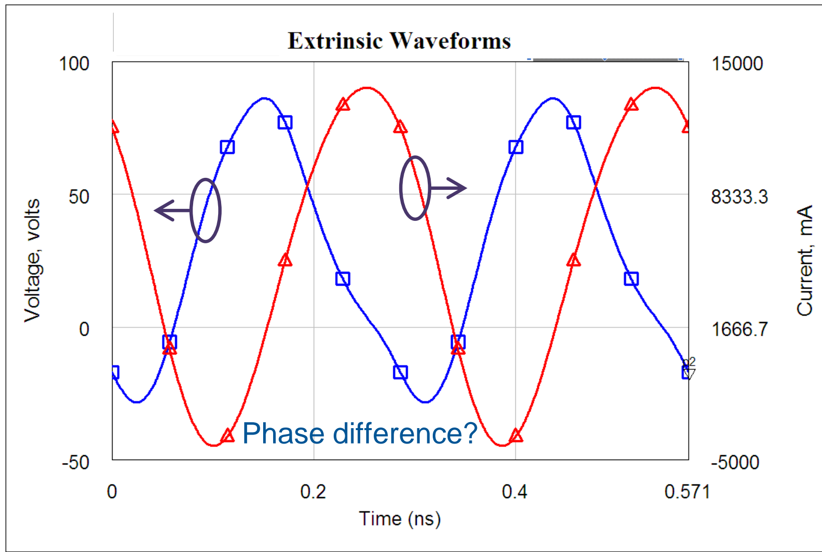
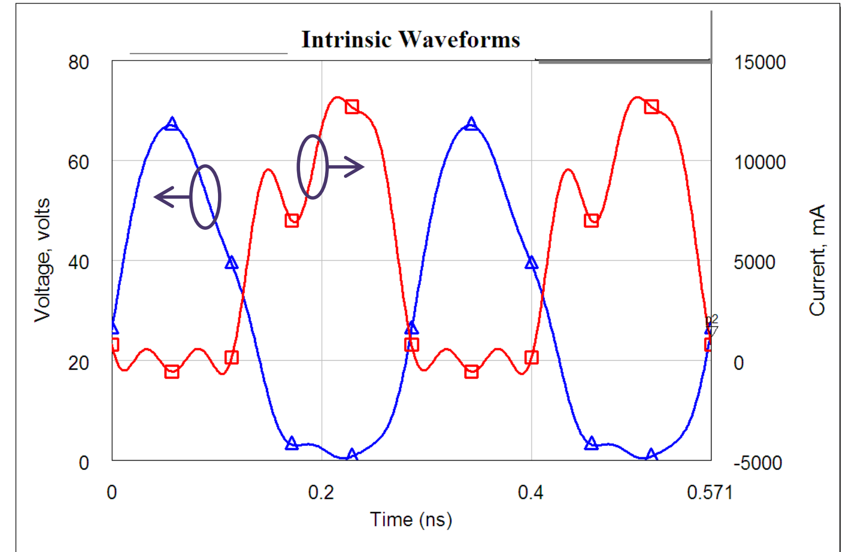
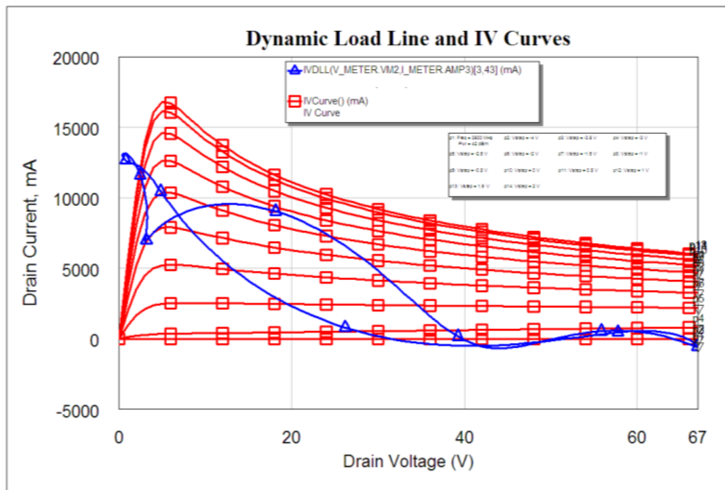
Comparison of Waveforms at "correct" and "incorrect" reference planes



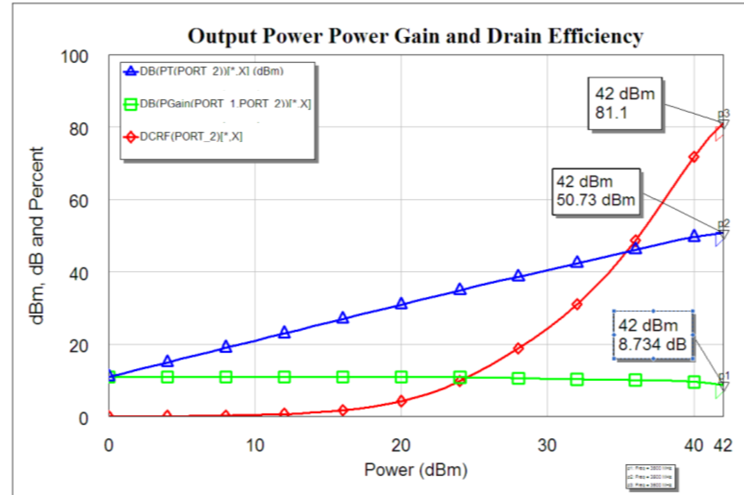
Note current goes to -4.2A at package planes!



Intrinsic current is close to zero at minimum!



Dynamic Load Line at full output power



Greater than 80% efficiency

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Example of Determining VSWR Robustness for a Single-Ended PA

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Using Intrinsic Ports to assess VSWR Robustness of PA Design

- There are three major reasons why GaN HEMTs may fail under VSWR Mismatch conditions
  - Excessive RF Drain Voltage
  - Excessive RF Drain Current
  - Excessive Channel Temperature
- As will be shown in the following example a nominal 28 volt GaN transistor (CGH40025F) operated into a 10:1 VSWR (any phase) can have an instantaneous drain voltage (at the die level) that exceeds 100 volts.
  - Clearly the relevant technology needs to support a typical drain breakdown voltage of 120 to 150 volts

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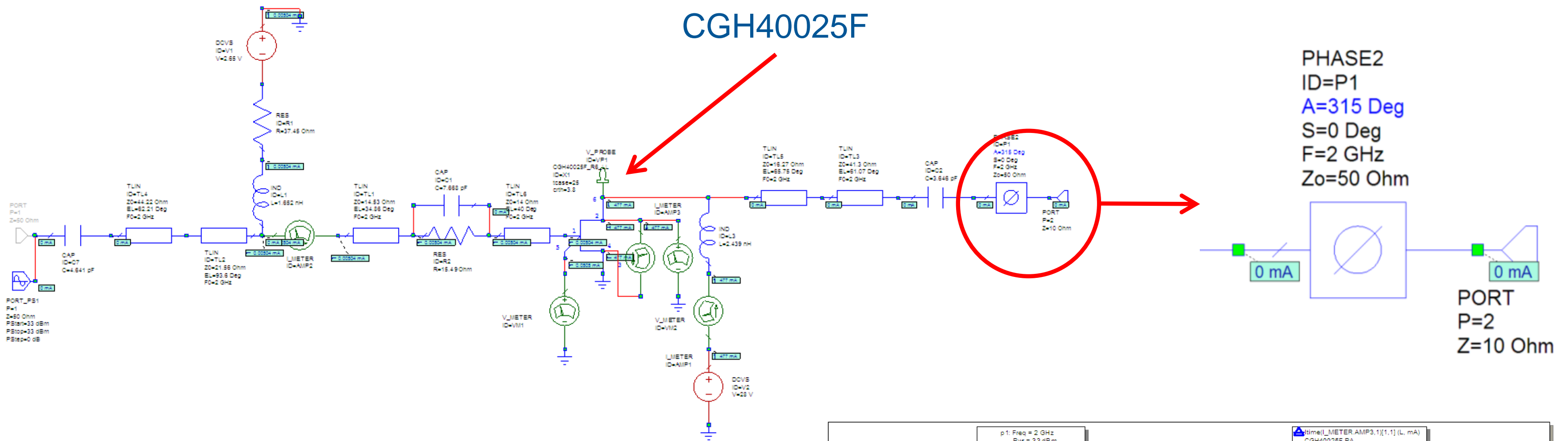
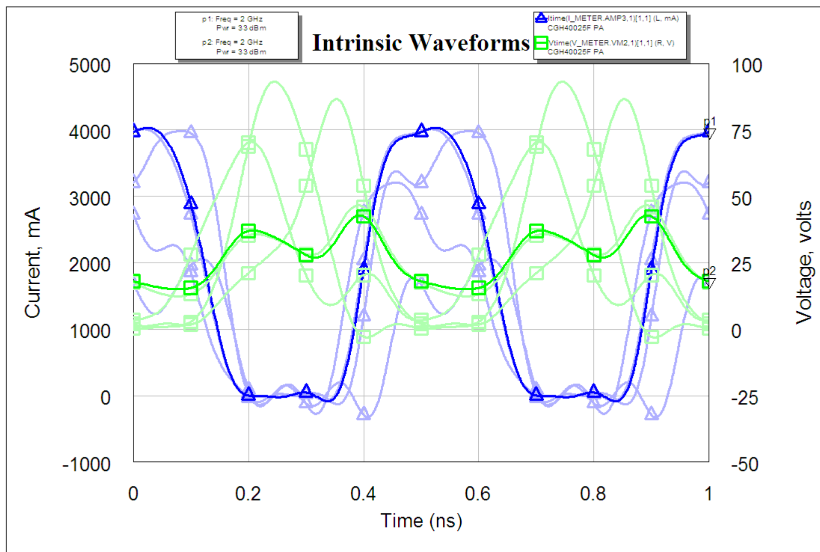
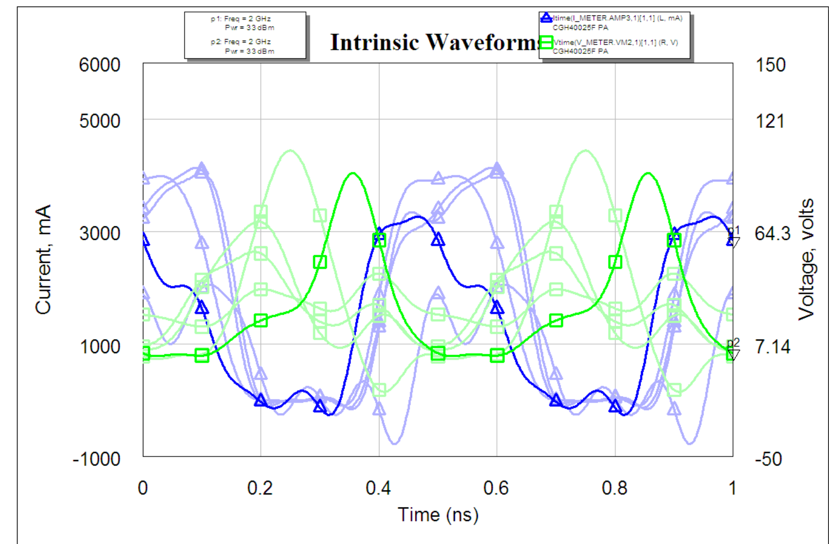
Output VSWR Robustness (1) – Drain Voltage and Current







10:1 VSWR Peak Drain Voltage = 105 volts (Vds=28 volts)

5:1 VSWR Peak Drain Voltage = 93 volts (Vds=28 volts)

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Output VSWR Robustness (2) – Channel Temperature

Temperature Rise

0.4257 ns
159.7 V

Vtime(V_METER.VM1,1)[1,1] (V)
CGH40025F PA

p1

2 GHz PA using CGH40025F

p1: Freq = 2 GHz
Pwr = 33 dBm

Degrees C: 0, 50, 100, 150, 200

Time (ns): 0, 0.2, 0.4, 0.6, 0.8, 1

Cree GaN HEMT Maximum Channel Temperature is recommended at 225°C. So under 10:1 VSWR maximum case temperature should not exceed 65°C at continuous full output power.

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Example of Class F Doherty PA

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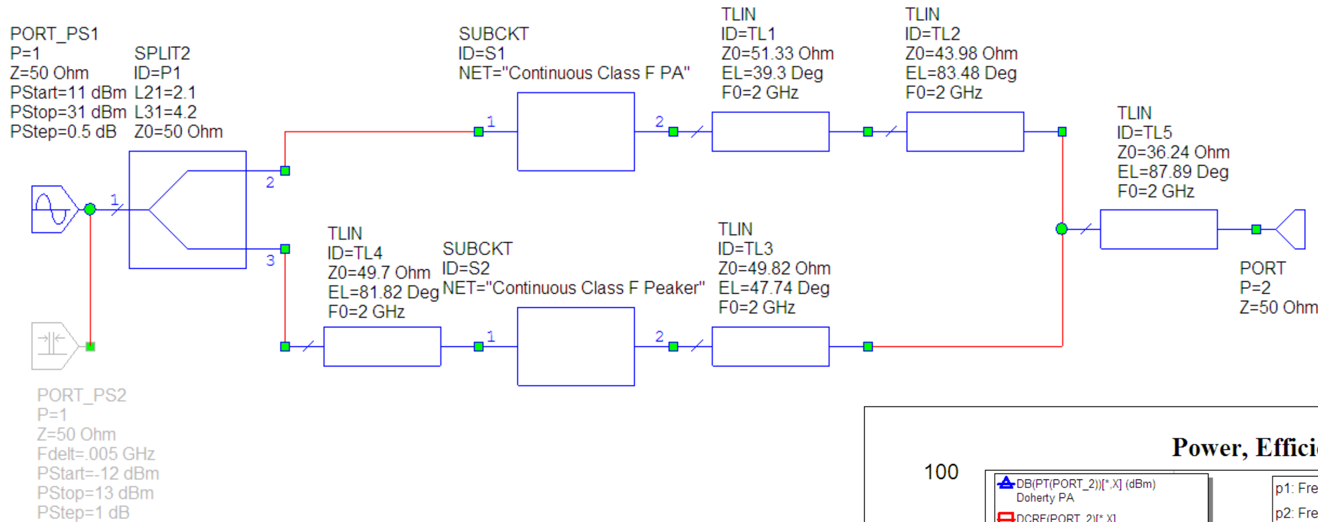
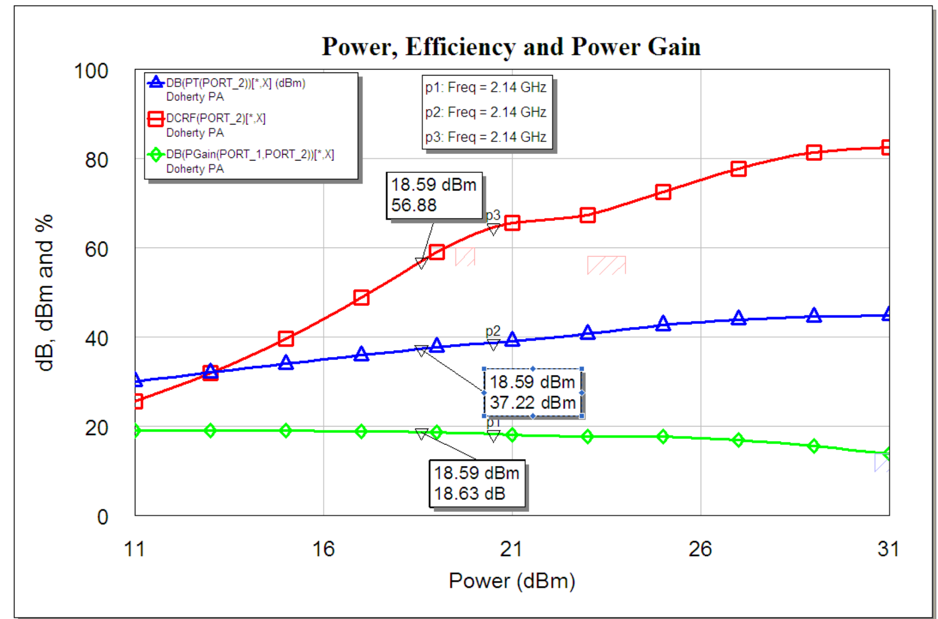
Basic Doherty PA Circuit and Performance at 2.14 GHz



- Unequal split two-way Doherty
- Employs two CGH40010F transistors
- 5 watts Pave at 7.5 dB OBO
    - Ideal for Small Cell Telecoms
- > 56% drain efficiency with 18 dB gain at 2.14 GHz
- Each amplifier (main and peaker) based on Class F design



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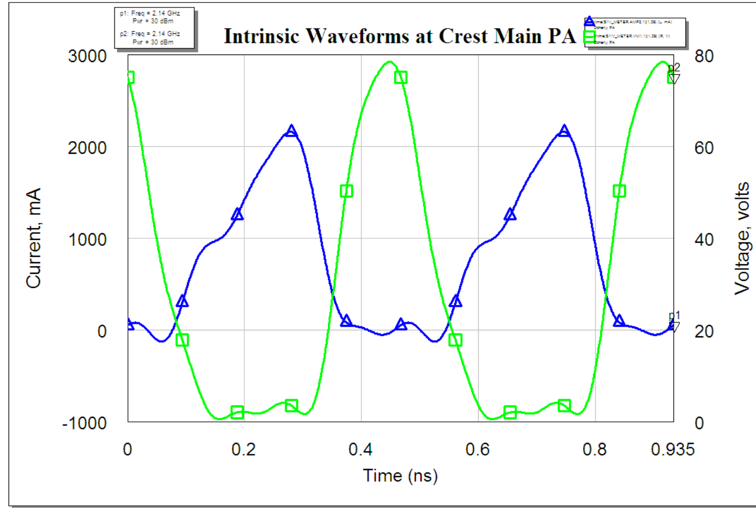
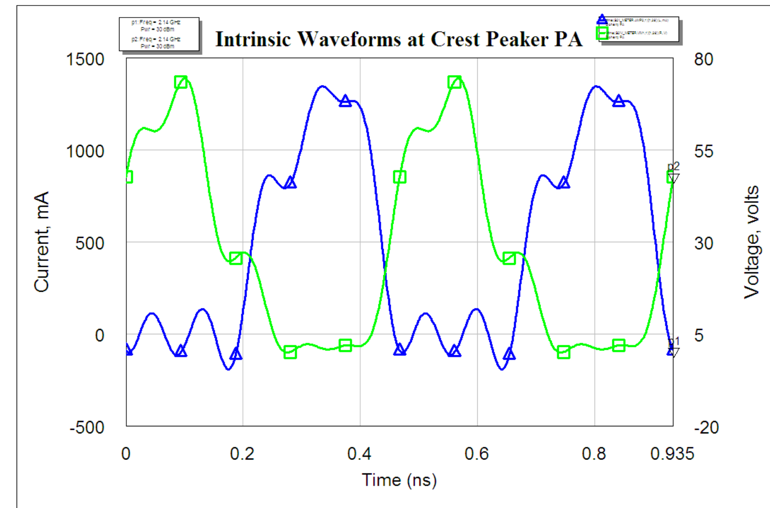
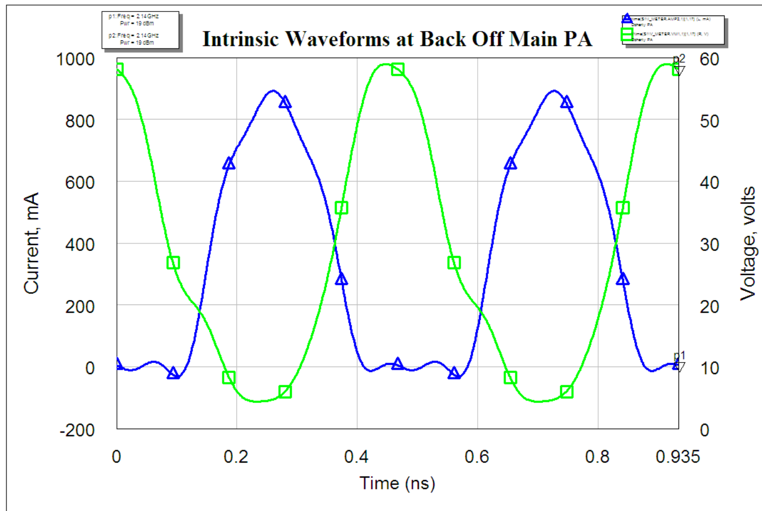
Intrinsic Waveforms of Main and Peaker Amplifiers



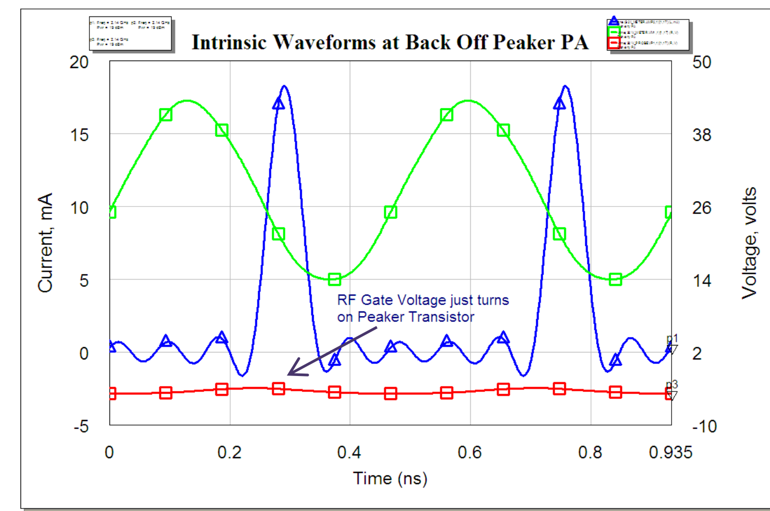
Main PA Waveforms at Full Power



Peaker PA Waveforms at Full Power



Main PA Waveforms at 7.5 dB OBO



Peaker PA Waveforms at 7.5 dB OBO

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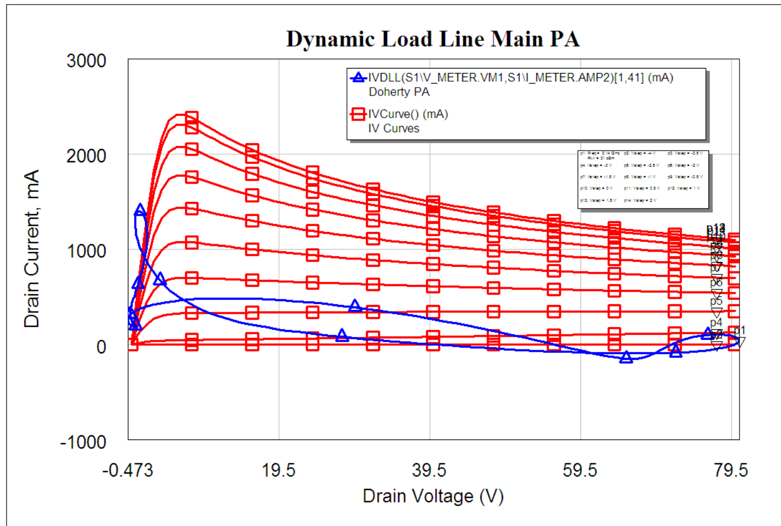
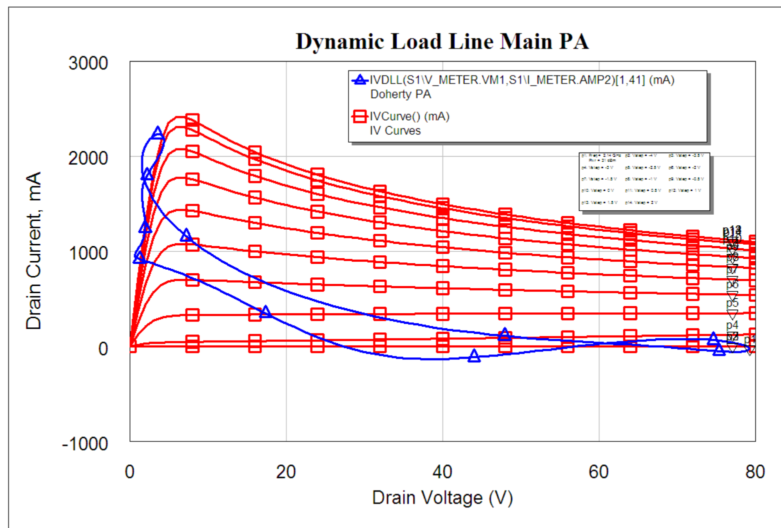
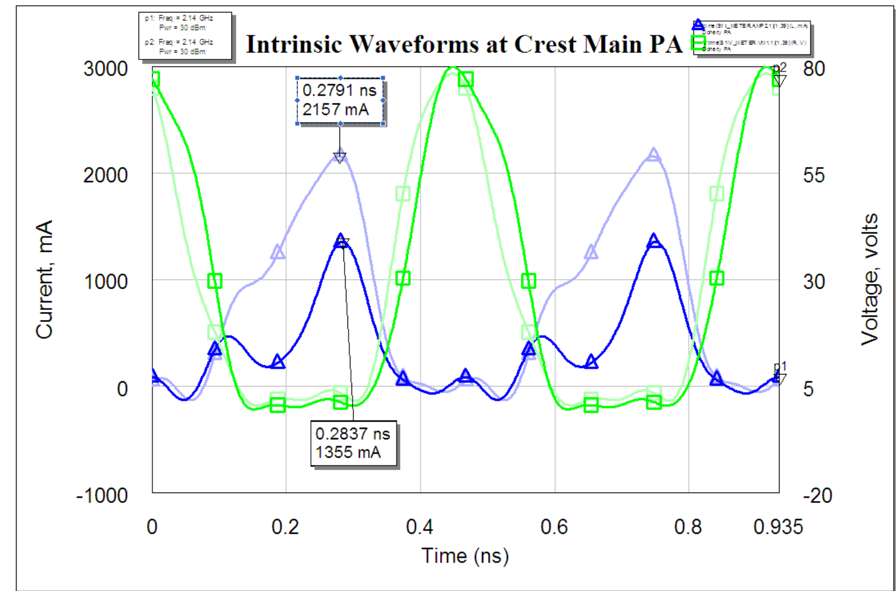
Peaker Amplifier Load-Pull on Main Amplifier





The effect of active load pull from the peaker PA on the intrinsic dynamic load-lines of the main PA

The effect of active load pull from the peaker PA on the intrinsic drain waveforms of the main PA



To the authors' knowledge this is the first published example of such a time domain simulation

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Conclusions

- Cree Large-Signal Models for GaN HEMT transistors have been extended to include 6 port functionality
  - Drain, Gate, Source
  - Intrinsic Drain Current
  - Intrinsic Drain Voltage
  - Temperature Sense
- Additional "intrinsic" ports allow easy and accurate inspection of "true" drain voltages and current waveforms
  - Useful for waveform-engineered amplifiers
  - Useful for "continuous" Class E and F simulations allowing maintenance of high efficiency and acceptable linearity over wide bandwidths
  - Additional design ability to check for PA ruggedness
  - Allows waveform engineering for 2 and N-way Doherty PA's

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