A Broadband LNA Design in Common-Source Configuration for Reconfigurable Multi-standards Multi-bands Communications

Sunday C. Ekpo, Rupak Kharel and MfonObong Uko

Department of Electrical & Electronic Engineering, Manchester Metropolitan University, Manchester, M1 5GD, UK.

scekpo@ieee.org; S.Ekpo@mmu.ac.uk

***Abstract*—The design of broadband low noise amplifiers (LNAs) for reconfigurable and real-time multi-standard multiband RF/microwave transceiver requires a holistic design trade-off for a given active device configuration. The common-source configuration generally yields moderate gain, narrow bandwidth and compensated stability for the lowest noise figure response. This paper presents a novel single-ended LNA topology that achieves high gain, broadband and very low noise in the common-source configuration. The pseudomorphic high electron mobility transistor process technology was utilised over the C- and K-band frequencies. The GaAs-based active device libraries came from two different foundries. The simulation results show that the reported circuit topology yielded gain and noise figure responses of 37.6 dB and 0.5 dB (over 4–8 GHz); and 30 dB and 1.0 dB (over 18–21.6 GHz). The minimum stability factor was higher than 4 at the respective centre-design frequencies and the in-band ripples were 5% (C-band) and 4% (K-band) relative to the 3 dB communication threshold. These results enable the reported broadband LNA to accommodate a wide dynamic range for multi-process technologies. The presented LNA designs can combine multi-band direct-conversion RF transceiver with embedded field programmable gate array processing to provide a multi-standard radio solution for reliable and cost-effective capability-based communication solutions.**

***Index Terms*—adaptive, amplifier, broadband, circuit topology, low noise, multi-standard transceiver, reconfigurable, satellite, real-time communication.**

I. Introduction

THE proliferating multi-standard broadband provisioning across various heterogeneous networks has presented a new challenge for the wired and wireline communication devices design. For both space and terrestrial communications, advances in receiver font-end components and subsystems active device technologies have continued to revolutionise their adaptive, reconfigurable and real-time (RT) capabilities [1–5]. Multi-standard RF/microwave transceiver systems have continued to attract global research interests following the need to satisfy the stringent requirements of the various wired and wireless communication standards [1, 2, 4].

The need to eliminate individual filter and off-chip matching components per radio standard has fueled the global research interests in reconfigurable receiver front-ends [4, 6]. Future-generation wireline and wireless communication systems will be expected to support wireless services convergence, intercontinental roaming and seamless ubiquitous broadband applications using various radio access technologies (including 2G, 2.5G, 3G, 4G and 5G) [7–11]. Compared with a typical single-standard transceiver, the technical flexibility of designing a multi-standard transceiver to satisfy the requirements of communication standards is limited by the size, cost and power dissipation. The immediate obvious solution is components footprints minimisation and a very large scale integration (including digitised analog/RF). Moreover, the power consumption and component integration thresholds of the various active device process technologies have limited the sustainable and reliable broadband performance of multi-standard transceivers. Reconfigurable RF receivers (and hence, transceivers) promise to address these concerns by providing beyond the optimal single-standard transceiver performance across multiple frequency bands with a broad dynamic range [2, 6, 9, 10]. Hence, an adaptive system-on-chip (SoC) design paradigm that satisfies the requirements of the existing and emerging communication standards is inevitable.

The low noise amplifier (LNA) sits in the receiver front-end of communication transceiver systems. The primary

objective of a reconfigurable RF system design usually involves a multiphysics design, modelling, simulation and validation of adaptable transceiver subsubsystems for multipurpose applications. This approach encompasses active and adaptive semiconductor devices technologies and parameters investigations; RF transceiver topology and system design characterisations; subsystems thermal analysis; distributed and discrete passive components qualification; and packaging constraints verification [1, 2, 6, 12]. This has resulted in the delivery of high bandwidth and RT data, voice and video contents over different transmission media. The applications of broadband RF/microwave receivers include satellite communications, mobile communications, internet of things/everything, sensor networks, multimedia infotainment, RT data acquisition, telecommunications and wearable devices [11–15]. The design trade-offs for these expanding applications depend largely on the active device technology and subsystem design configuration.

This paper is organised as follows. Section II focuses on the communication receivers design requirements and trade-offs. Section III explains the various monolithic microwave integrated circuit (MMIC) low noise amplifier design topologies. The broadband LNA designs in common-source configuration using the pseudomorphic high electron mobility transistor process technology and GaAs-based active devices from two foundries are presented in section IV. The simulation models, results and discussion are stated in section V. Section VI concludes this paper.

II. Communication Receiver Front-end Design

Space and terrestrial communications systems depend on monolithic and discrete semiconductor components with low noise figures (NFs) and contributions for high sensitivity and excellent broadband performance [14–17]. The C- (4–8 GHz) and K- (18–21.6 GHz) bands are broadband frequency ranges utilised for cellular and satellite communications [14, 15]. Designing low noise amplifiers for a reliable radio receiver performance operating in these bands requires an objective consideration of the receiver subsystem topology and process technology with recourse to the useable bandwidths (UBs) and the centre-design frequency, f_d. For the C-band, the useable bandwidth is 4 GHz and the value of f_d is approximately 5.7 GHz. Similarly, the K-band has an UB of 3.6 GHz and a f_d of approximately 19.7 GHz. Performance trade-offs are usually investigated to understand the practical challenges evident in the design, fabrication, measurement and deployment of LNAs [16–18]. The key LNA performance variables spanning device- and board-levels variables are characterised with recourse to the noise parameters associated with the LNA design.

The system noise temperature of space satellite and terrestrial receivers consist of the effective antenna noise temperature, the effective cable noise temperature and the effective receiver noise temperature. Mathematically, this is given in by:

$$T_s = \frac{T_a}{L_c} + T_t\left(\frac{L_c - 1}{L_c}\right) + T_o(F - 1) \quad (1)$$

where
T_s = effective system noise temperature, K
T_a = effective antenna temperature including all external noise, K
T_t = thermodynamic temperature of the cable, K
T_o = standard reference temperature, 290 K
L_c = input cable loss factor
F = noise figure for the receiver defined at the terminals as a linear ratio

A LNA design for broadband communications systems requires an intelligent trade-off of design parameters for an optimal performance. While low noise figure and high linear (or power) gain are the key performance indicators, an ideal broadband system design has zero ripple (absolute gain flatness) and reflections. Thus, typical specifications for communication systems include a less than 3 dB in-band ripple and very low voltage standing wave ratios [1, 16]. These are essential requirements for adaptive and RT multi-standard communications (such as in satellite systems that must swap between networks and missions) [11, 13, 15].

To achieve an appreciably high gain, very low noise performance and negligible reflections at the input and output of a cascaded wideband LNA system is needed. This requires an enormous system tuning and/or optimisation to arrive at the signal reception specifications for the LNA. Furthermore, negligible in-band ripples (that is, a nearly constant gain broadband LNA) can be achieved by connecting external circuit elements that optimise the frequency-dependent forward linear gain (S_{21}). Two key techniques commonly used are: [1, 2, 6, 12, 16]

- Negative feedback; and
- Selective mismatch of the input and output circuitry.

While gain and noise figure trade-offs of a stage are recommended for gain flatness over the operating frequency range, the effect of the source impedance (or admittance) on these two LNA parameters is worth giving credence. Computer-aided design tools abound for enhancing easy analysis and/or synthesis of LNA design elements and networks. A typical MMIC LNA performance is assessed based on the noise parameters associated with it. Noise parameters enable the process of tuning the LNA source admittance with recourse to its noise characteristics. The noise figure estimating relationship is given by:

$$NF = 10\log\left(F_{\min} + \frac{R_n}{\mathrm{Re}(Y_{source})}\left|Y_{source} - Y_{opt}\right|^2\right) \quad (2)$$

where
Y_{opt} = the normalized input admittance in siemen (S) for a minimum noise factor, F_{min}. To obtain the optimal noise performance, the complex conjugate of Y_{opt} must be connected at the LNA input;
F_{min} = the minimum noise factor at which $Y^*_{source} = Y_{opt}$; minimum noise figure = $NF_{min} = 10\log(F_{min})$;

R_n = the equivalent noise resistance which indicates the sensitivity of the noise figure to the deviation between Y_{source} and Y_{opt};
Y_{in} = the normalized input admittance for maximum power transfer; and
Y_{source} = the normalized source admittance presented to the LNA input.

The input and/or output LNA performance reference admittances and impedance matching networks are normalised to $Y_o = (50\ \Omega)^{-1} = 0.02$ S. A reference plane within a RF receiver subsystem chain enables side-by-side parametric comparisons. It represents a particular point within the RF receiver that is set to a particular impedance (typically 50 Ω) through a system calibration or by definition [16–18].

The parameters of the receiver subsystem sensitivity [1, 2, 16] for optimising LNA performance are defined as follows:

$$NF_{sys} = 10\log\left(F_{sys}\right) = 10\log\left(F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}}\right), dB \quad (3)$$

$$P_{rin} = kT = 10\log\left(BW\right) + NF_{sys}, dBm \quad (4)$$

$$[P1dB]_{input} = [P1dB]_{output} - G_{sys} + 1, dBm \quad (5)$$

$$SFDR(P_{in} = P_{blkr}) = [P1dB]_{input} - IMD3(P_{in} = P_{blkr}), dB \quad (6)$$

where NF_{sys} is the cascaded NF of the receiver subsystem referred to the input of the receiver; F_n, the noise factor of each consecutive stage within the receiver subsystem chain; G_n, the linear gain of each consecutive stage within the receiver subsystem chain; P_{rin}, the noise floor for the input sensitivity of the receiver; kT, the thermal noise density (with a value of -174 dBm/Hz at room temperature); BW, the bandwidth of the receiver signal; $P1$ dB, the input/output signal power that corresponds to 1 dB gain compression; G_{sys}, the system linear gain; SFDR ($P_{in} = P_{blkr}$), the spurious-free, dynamic range with the largest expected blocker signal power present at the receiver referred-input; and IMD3 ($P_{in} = P_{blkr}$), the third-order cross-modulation product generated within the receiver when the largest expected blocker (P_{blkr}) signal power is present at the input of the receiver.

Equations (3) and (4) indicate that the forward transmission gain of the receiver must be obtained as a trade-off between the overall receiver system noise figure (NF_{sys}) and the $P1$dB compression point (which defines the input dynamic range).
From (4), an excessive LNA signal gain degrades the input dynamic range of the receiver. However, (3) indicates that a high enough gain is required for the LNA NF to dominate the cascaded NF. Furthermore, (4) suggests that a narrow receiver bandwidth and a low NF are required for setting the noise floor for receiver sensitivity. This requirement should be satisfied with recourse to the level of degradation the target signal would experience. The minimization of the receiver NF should be carried out with recourse to the application requirements since an improved receiver NF can enhance the receiver performance and communication range.

MMIC LNA designs at RF/microwave and millimetre-wave often require smaller devices. Most GaAs foundries have provided standard HEMT models spanning large periphery devices including 80 μm, 120 μm and 200 μm. These standard models are developed based on the measured S-parameters (DC to 50 GHz) and measured noise parameters (DC to 40 GHz). Standard devices are often scaled and extrapolated to achieve smaller device geometries for microwave and millimetre-wave applications. Scaling equations can be used to scale the gate width of the active devices. However, only gate widths from 75 % to 125 % of the original gate width yield valid models with scaling equations. For instance, the, TriQuint's TQP13N process was used for the presented designed and fabricated K-band MMIC LNA design. It comprises a low-cost 150 mm wafer and optical lithography 0.13 μm pHEMT process. The gate widths of the stages are 4 x 35 μm (first stage), 2 x 50 μm (second stage) and 5 x 50 μm (third stage). These device sizes were selected because they provided good impedance matching and broadband characteristics for the entire K-band. The circuit topology adopted was a single-ended architecture with a common-source stage for low noise and moderate gain performance. The input matching circuit was designed to give the minimum achievable noise factor.

Most of the published simulated and measured MMIC LNA design data for active devices spanning the RF/microwave and millimetre-wave frequencies have chosen and/or recommended the single-ended architecture for low noise communications applications [1, 2, 6, 16, 19–24]. The prevailing active device configuration for low noise applications is common-source or common-gate. An et al have designed and fabricated a 1.5 to 2.5 GHz MMIC LNA using the ETRI (electronics and telecommunications research institute) library [21]. The simulation results differ from the measured responses by less than 20 % for both the amplifier gain and the noise figure. This difference is attributed to the process variations. MMIC LNAs characterisations which cover the Q (40–44 GHz)- and V (58–65 GHz)-bands have been carried out using a 0.15 μm GaAs-based pHEMT process. The results of the simulated and measured MMIC LNAs compare very favourably over the frequency bands of interest. Except in the magnitude of the Q-band, the simulated and measured gain and noise variations are approximately 1 dB. Furthermore, Aneja and Kumar have designed and measured a pHEMT-based ultra-wideband (UWB) (3.1 to 10.6 GHz) LNA [23]. The simulated and measured gains of the UWB are approximately 9 dB. The simulated and measured output and input reflection coefficients are benchmarked at -10 dB for wired and wireless communications applications. However, designing the nominal LNA's reflection coefficient (S_{11}) to be only approximately -10 dB can cause the amplifier to fail to meet its matching specifications in the process corners. Hence, a perfect match at the input of the LNA is desirable for an optimal performance.

Sivonen et al have analysed the packaging effects in inductively-degenerated common-emitter LNAs using the single-ended and the balanced LNA topologies [12]. In the case of the balanced LNA topology, the package parasitics affect the receiver performance only through the LNA input. Unpackaged and packaged LNA cases were considered and the investigation was based on the transducer power gains (TPGs) and the NFs of the LNA in both cases. They found out that the TPGs and

NFs of the unpackaged and the packaged LNA for the single-ended LNA topology were approximately equal. Similarly, the TPGs and NFs of the unpackaged and packaged balanced LNAs with the same power consumption, active device size, emitter inductance and load resistance were analysed to be approximately equal. Furthermore, the authors concluded that the packaging does not worsen the properties of the inductively-degenerated amplifier. Lu et al have also investigated the effects of packaging on a CMOS LNA and focused on the flip-chip and wirebond packages as their case studies [20]. The study also involved modelling the ground proximity effects on on-chip spiral inductors in a flip-chip package. The authors reported an excellent agreement between the simulated model and the measurement (up to 20 GHz) for the CMOS LNA for a 64-pin flip-chip ball grid array (FCBGA) package and a 64-pin wirebond quad flat non-lead (QFN) package. Moreover, the authors concluded that the RF specifications could be predicted for a CMOS LNA when packaged in both packages. A chip-package co-simulation carried out by the authors was reported to achieve a good agreement with the measurement result.

III. MMIC LNA Design Topologies

The operating frequency of the MMIC determines the choice of a circuit design approach. This informs the active device and discrete components footprints integration onto a given circuit network. From the operating frequency perspective, the three main MMIC design techniques are all-transistor; lumped-element; and distributed. In terms of the input and output configurations of MMIC LNAs, three design topologies have been identified including single-ended LNA; differential input and single-ended LNA; and differential LNA [16, 19–24].

The board-level considerations for a MMIC LNA design are bias setting, stability and feedback.

1) Bias Setting

The drain current setting is used to trade-off optimal noise figure and gain.

2) Stability

Stability circles (for source and load) are used to verify the legitimacy of chosen Z_{IN} and Z_{OUT}. It is a good design to always check the stability of a design well beyond band-of-interest. The considered stability parameters are:

- Small-signal stability (k, b or μ factors); and
- Large-signal stability.

The most common causes of circuit instability are:

- Insufficient RF decoupling between the supply lines of the amplifier stages;
- Parasitic inductance in ground connections;
- Excess in-band and/or out-of-band gain;
- Insufficiently decoupled supply lines; and
- EM coupling.

To achieve a LNA circuit stability, the following methods of compensation are used:

- RF Feedback;
- Filtering to knock down excessive out-of-band gain; and
- Resistive damping: Shunt resistance across LNA output preferred over Shunt resistance across LNA input (used as a last resort). This method directly impacts the NF, gain and dynamic range of the communication receiver.

3) Feedback

- Common-source LNA: Source/Emitter degeneration

Small inductance on the source/emitter appears as real portion on Y_{IN}. This improves the stability and linearity of the LNA at the expense of the gain, especially at higher frequencies. This can move Y_{IN} and Y_{OPT} closer together on the Smith chart.

- Common-gate shunt feedback

This improves linearity and stability at the expense of gain especially at higher frequencies

- Cascode shunt RC/RLC feedback

This improves stability, gain flatness and bandwidth at the expense of gain. It moves the match for maximum gain closer to Y_{OPT}. Large reverse feedback (RFB) values improve the input voltage standing wave ratio (VSWR) without a significant impact on the NF (for $R > 1$ kΩ).

Table 1 illustrates a comparison of the three main LNA topologies commonly adopted for MMIC LNA designs. It is obvious from the LNA design topologies characteristics that the cascode gives the most stable forward transmission gain over a given operating wideband. However, the cascode topology has the highest sacrifice in terms of the receiver subsystem design complexity and its NF performance is lower than the value obtained using the common-source topology.

The designed C- and K-bands MMIC LNAs reported in this paper adopted the common-source topology to deliver an excellent input impedance matching and the lowest possible noise figure simultaneously. Given that this topology is most suitable for narrowband receiver front-end designs, an innovative design consideration was used to achieve a broadband performance and minimize the sensitivity of the MMIC LNAs to bias, temperature and component tolerances. The design was carried out to minimize the need for off-chip noise matching circuit components. The key LNA design parameters considered for matching the optimum admittance (Y_{opt}) with the input admittance (Y_{in}) are the gate finger dimension, interconnects, RF feedback, layout and package parasitics.

TABLE 1

A Comparison of LNA Topologies [16]

Characteristic	Common-Source	Common-Gate	Cascode
Noise figure	Lowest	Rises rapidly with frequency	Slightly higher than common-source
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Highest
Bandwidth	Narrow	Fairly broad	Potentially highest
Stability	Often requires compensation	Higher	Higher
Reverse isolation	Low	High	High
Sensitivity to PV, T, PS and CT.	Greater	Lesser	Lesser

*PV = process variation; T = temperature; PS = power supply and CT = component tolerance.

IV. Broadband LNA in Common-Source Design

A. C-band MMIC LNA Design

The C-band spans 4–8 GHz of the electromagnetic spectrum and satellite communications operate within this frequency band. High electron mobility transistors (HEMTs) favour LNAs design because of their excellent discrete-level performance characteristics at microwave frequencies – low noise and high forward transmission gain.

A high performance low noise amplifier with a low power consumption and appreciable gain is required for adaptive small satellite applications. In this paper, a three-stage C-band low noise amplifier was designed and simulated using the Agilent Design System software. The amplifier uses PL15-10 0.15 µm LN InGaAs pseudomorphic high electron mobility transistor (PHEMT) process technology in the simulations; it is a scalable EEHEMT1 large signal model provided by WIN Semiconductors. The various design parameters (forward transmission gain, transconductance, minimum noise figure and noise resistance) for the 4 x 75 µm PL15-10 0.15µm LN InGaAs PHEMT model are obtained at V_{gs} = -0.4 to 0.1, V_{ds} = 1 V and f = 4–8 GHz.

The first stage of a low-noise amplifier is designed (and matched) for low noise while the subsequent stages are used for gain compensation; that is, the stage increases with high gain requirement but decreases with noise level. In this paper, the first stage of the MMIC LNA was designed to present the optimum match, Γ_{opt}, over the operating frequency to the gate of the first HEMT when the MMIC input is terminated in 50 Ω. Optimum impedance was presented to the device to achieve the minimum noise figure for the first stage. Second and third stages were matched for a maximum stable gain.

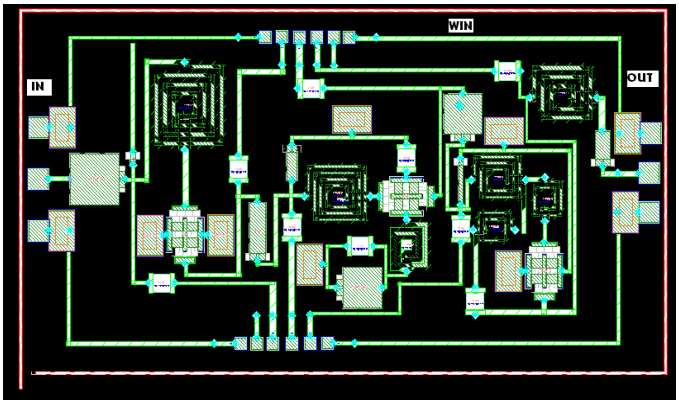
B. K-band MMIC LNA Design

The presented K-band MMIC LNA spans 18–21.6 GHz of the electromagnetic spectrum; satellite communications and radar operate within this frequency band. The K-band LNA presented in this paper is a scalable PHEMT large signal model provided by Triquint. The reported design comprises a three-stage MMIC LNA design characterised thus:

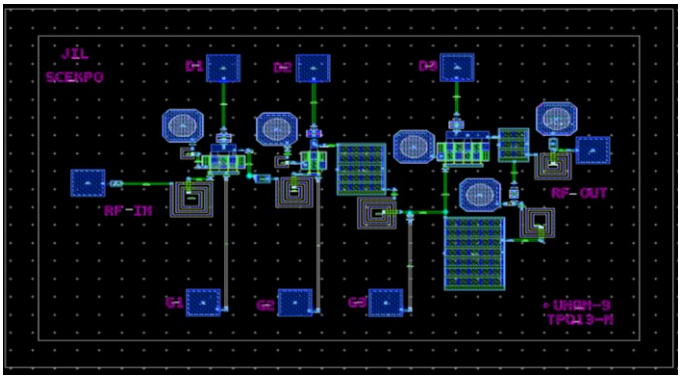
- Stage one: transistor size = Ng x W = 4 x 35 µm; source inductive feedback (for stabilisation and improved input matching of the device).
- Stage two: transistor size = 2 x 50 µm; interstage matching network was designed to transform the output impedance of stage one transistor to the optimum input impedance of stage two transistor.
- Stage three: transistor size = 5 x 50 µm; parallel feedback (for stabilisation and gain flatness); the output matching circuit was designed to transform the output impedance of stage two transistor to 50 Ω.

The first stage of a low-noise amplifier is designed (and matched) for low noise while the subsequent stages are used for gain compensation; that is, the stage increases with high gain requirement but decreases with noise level. In this report the first stage of the K-band MMIC LNA was designed to present the optimum match, Γ_{opt}, over the operating frequency (18–21.6 GHz) to the gate of the first HEMT when the MMIC input is terminated in 50 Ω. Optimum impedance was presented to the device to achieve the minimum noise figure for the first stage. The second and third stages were matched for the maximum stable gain.

The input and output matching networks employed were *L* series and *C* parallel elements. Inter-stage coupling capacitors were used to couple the three stages together of both broadband LNA designs. The first stage was designed for low noise while the last two stages were designed for maximum gain and high power reception capability.



(a) C-band



(b) K-band

Fig. 1. Layout of the designed C- and K-bands MMIC LNAs

The layouts of the designed C- and K-band MMIC LNAs are depicted in Figs. 1(a) and 1(b) respectively. The size of the C–band LNA chip is 1.5 x 0.8 mm and that of the K-band LNA chip, 0.85 x 1.35 mm. Thus, the K-band MMIC LNA is approximately 96% of the size of the C-band LNA chip.

V. Simulation Results and Discussion

The single-ended input and single-ended output MMIC LNA topology is sufficient for multi-standard, multiband communications applications. This was utilised in the CSC for the broadband MMIC LNA designs reported in this paper. The results of these designs indicate that the useable bandwidth is wideband and this is required for space and terrestrial communications applications. For instance, the input reflection coefficients of both C- and K-bands are well below the -10 dB threshold for telecommunications and wireless communication

applications. Moreover, the in-band gain ripple is less than 3 dB. The forward transmission gains of the LNAs were optimised to improve the receiver sensitivity and selectivity. The stability factors for the MMIC LNAs were obtained with recourse to the fabrication and/or process defects and the specified performance requirements. Furthermore, different LNA topologies were designed, modelled and simulated and their respective average DC power consumptions assessed. The realisation of each topology was validated with recourse to the limitations of the foundry components. A trade-off of the various topologies was used to meet the design and fabrication requirements for the final MMIC LNA circuit using real components. The presented C-band MMIC LNA circuit gives good forward gain and noise responses and thus a circuit of choice; its performance meets the design requirements for wireless communications applications over the operating band.

The design specifications for the C-band MMIC LNA are stated in Table 2. The s-parameters and power consumption performances for the simulated C-band MMIC LNA circuit are shown in Tables 3 and 4 respectively. The minimum stability factor of this topology up to cut-off frequency is 2.2. The forward gain (S_{21} = 37.6 dB) is almost constant over the characterised frequency range. Moreover, the input (S_{11}) and output (S_{22}) reflections at the resonant frequency are -15.2 dB and -24.3 dB respectively. The noise figure (NF (dB)) maintains a broadband response with 0.5 dB at 6 GHz and a maximum value of 0.64 dB at 8 GHz. The isolation (S_{12}) response is below -55 dB over the entire C–band.

The drain currents are well below the maximum allowable value; I_{d1} = 52.11 mA, I_{d2} = 15.58 mA and I_{d3} = 50.85 mA.

Noise resistance, R_n, of a device indicates how fast the noise figure degrades as Γ_s moves away from Γ_{opt}. The average 3.4 Ω noise resistance obtained with the lumped elements topologies reveals that the noise figure factor is less sensitive to the source impedance, thereby enhancing the circuit design.

The design specifications for the K-band MMIC LNA are stated in Table 5. The s-parameters and power consumption performances for the simulated K-band MMIC LNA circuit are shown in Tables 6 and 7 and Figs. 2 to 7. The forward gain of the K-band MMIC LNA (S_{21} = 30 dB) is almost constant over the characterised frequency range (Fig. 2). Moreover, the input (S_{11}) (Fig. 3) and output (S_{22}) (Fig. 2) reflections appreciably satisfy the design requirements over the band with the values at the resonant frequency being -19.9 dB and -15.0 dB respectively. The isolation (S_{12}) response is good; it is below -50.3 dB over the entire K–band (Fig. 5). The noise figure (NF (dB)) (Fig. 6) maintains a broadband response with 1.0 dB at 19.8 GHz and a maximum value of 1.2 dB at 21.6 GHz. Furthermore, the minimum stability factor (Fig. 7) of this topology up to cut-off frequency is 3.9 and the noise resistance, 9.6 Ω. This is promising for reliable and cost-effective capability-based communication solutions (including cellular networks and high speed integrated RF-fibre/free space optics signal reception and distribution systems).

In this paper, the source inductive feedback (which is similar to the inductively-degenerated amplifier) and common-source configuration (CSC) (which is similar to the common-emitter configuration) were adopted for the single-ended broadband LNA topology.

Given the perfect match of the LNA input and the high stability factor achieved, it is expected that the simulated, unpackaged/fabricated and packaged performances of the reported designed LNAs would have a rather good agreement; this is further supported by the presented literature on the inductively degenerated common--source configuration. For a 50-Ω RF input (SMA), the combined tuning range of a multi-standard receiver front-end subsystem deploying the presented broadband MMIC LNA designs would be 4–8 GHz and 18–21.6 GHz; this yields a combined multimode multi-band receiver bandwidth of 7.6 GHz.

TABLE 2
C-BAND LNA DESIGN PARAMETERS AT CENTRE-DESIGN FREQUENCY

Design Parameter	Response at 6 GHz
S_{11} (dB)	≤-10
S_{12} (dB)	≤ -40
S_{21} (dB)	30–40
S_{22} (dB)	≤ -10
NF (dB)	≤ 1
R_n (Ω)	3.44
K	≥ 1
In-band Ripple (dB)	≤ 3

TABLE 3
C-BAND LNA CIRCUIT PERFORMANCE AT CENTRE-DESIGN FREQUENCY

Design Parameter	Response at 6 GHz
S_{11} (dB)	-15.2
S_{12} (dB)	-59.5
S_{21} (dB)	37.6
S_{22} (dB)	-24.3
NF (dB)	0.50
R_n (Ω)	3.44
K	6.1
In-band Ripple (dB)	1.90

TABLE 4
DC POWER CONSUMPTION OF THE C-BAND MMIC LNA CIRCUIT

Circuit	DC Power Consumption (mW)		
	Stage 1	Stage 2	Stage 3
LNA	52.1	15.6	50.9

In terms of satellite communication applications, the presented broadband LNAs would cover the frequency bands that are utilised for public-switched voice and data communications, internet trunking and backhauling (C-band); and two-way interactive consumer broadband and military networks (K-band). Various multi-standard receiver architectures have been implemented for various wireless standards and radio access technologies. The two main conventional implementations are the independent RF front-ends design per radio standard and the

shared RF front-end design supporting all the allowable radio standards.

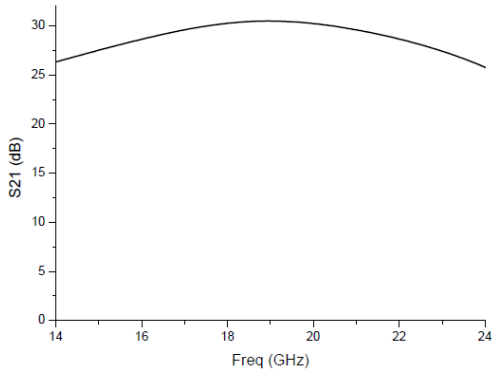


Fig. 2. Forward transmission gain of the K-band MMIC LNA circuit

TABLE 5
K-BAND LNA DESIGN REQUIREMENTS AT CENTRE-DESIGN FREQUENCY

Design Parameter	Response at 19.8 GHz
S_{11} (dB)	≤ -10
S_{12} (dB)	≤ -40
S_{21} (dB)	>25
S_{22} (dB)	≤ -10
NF (dB)	≤ 1.5
R_n (Ω)	≤ 5
K	≥ 1
In-band Ripple (dB)	≤ 3

TABLE 6
K-BAND LNA CIRCUIT PERFORMANCE AT CENTRE-DESIGN FREQUENCY

Design Parameter	Response at 19.8 GHz
S_{11} (dB)	-15.0
S_{12} (dB)	-50.3
S_{21} (dB)	30.3
S_{22} (dB)	-19.9
NF (dB)	1.0
R_n (Ω)	5.2
K	4.9
In-band Ripple (dB)	1.3

TABLE 7
DC POWER CONSUMPTION OF THE K-BAND MMIC LNA CIRCUIT

Circuit	DC Power Consumption (mW)		
	Stage 1	Stage 2	Stage 3
LNA	22.95	18.54	59.50

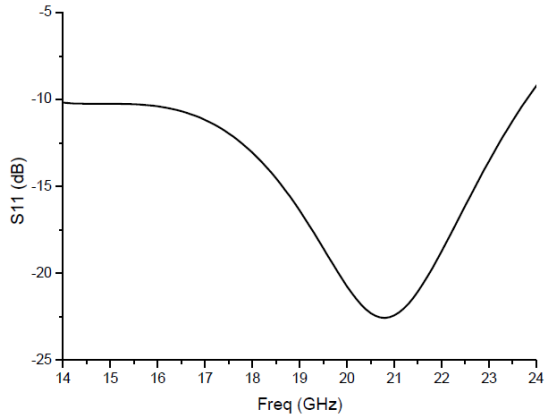


Fig. 3. Input reflection coefficient of the K-band MMIC LNA circuit

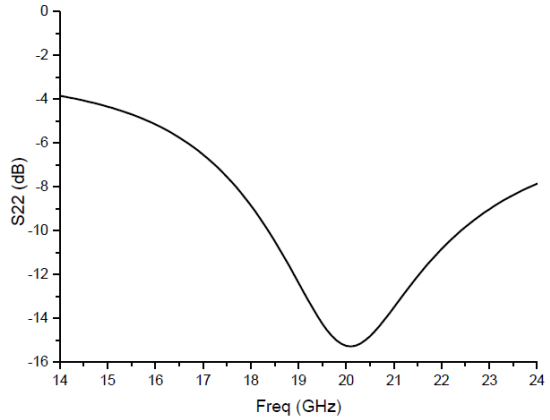


Fig. 4. Output reflection coefficient of the K-band MMIC LNA circuit

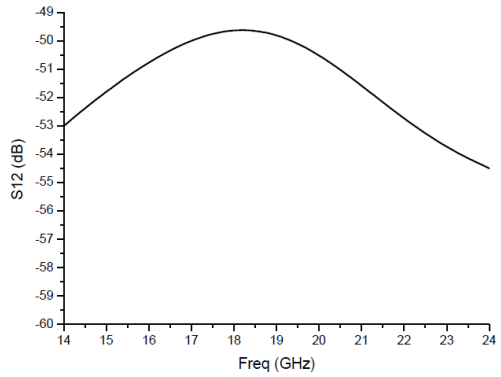


Fig. 5. Isolation of the K-band MMIC LNA circuit

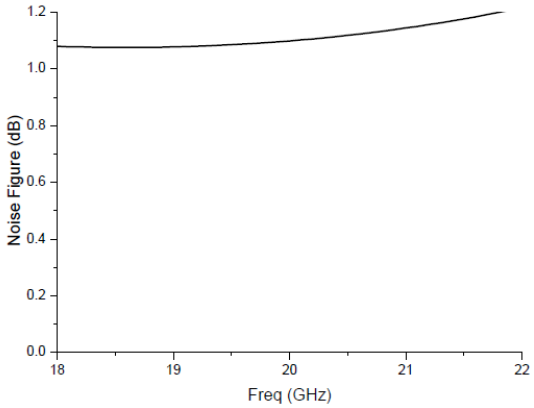


Fig. 6. Noise figure of the K-band MMIC LNA circuit

In each multi-standard operation, a trade-off of the size, weight, power consumption and cost is carried out to accommodate the target wireless standards of interest. The penalty for adopting the independent RF front-ends design is increased size, weight, power consumption and cost. The shared RF/analog front-end chain (after the LNA) design enables the reuse of receiver subsubsystems and reduces the component footprints. Generally, design considerations such as the IF architecture and the dynamic range requirement influence a multi-standard receiver implementation. An ideal multi-standard receiver is the software-defined radio (SDR) – a software-based single path receiver with a single electronic chip that adapts its operation to the RF environment. Thus far, no multi-standards receiver (with a single path or multiple/hybrid paths) that covers 10.1 GHz bandwidth has been reported. Simultaneous low power overhead and high reactivity are the key reconfiguration metrics (RMs) targets [6].

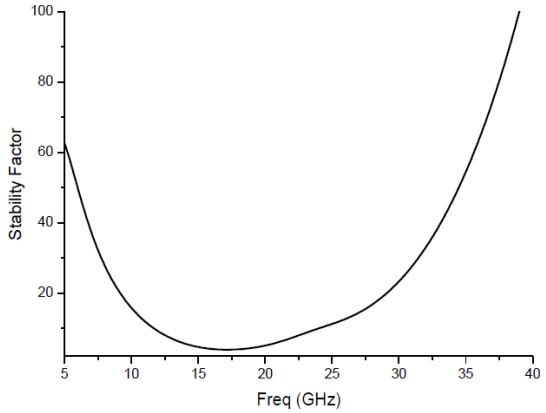


Fig. 7. Stability factor of the K-band MMIC LNA circuit

Moreover, the type of receiver architecture that is adopted in the design determines the receiver subsystem integration. For highly integrated multi-standard receiver designs, low-IF and direct conversion (with a zero-IF and simple baseband circuit) are the prevailing architectures. The low frequency error performance and high analog-to-digital converter (ADC) sampling speed requirement determine the application of each architecture. Consequently, direct conversion is suitable for radio standards with wideband signals while the low-IF is good for wireless standards with narrowband signals. Moreover, the dynamic range margin for a RF receiver is determined by the maximum input signal, sensitivity and interference levels. This requirement is more constraining for the multi-standard receiver because the power levels for the trio dynamic range margin parameters vary with the communication standards. For instance, the sensitivity and maximum input signal levels of the WCDMA and IEEE 802.11b are -107 dBm and -10 dBm respectively. Ideally, a multi-standard receiver that covers these two wireless standards would have to operate with a dynamic range of 97 dB. This dynamic range threshold can be achieved by controlling the forward transmission gains of the LNA and the baseband amplifier [2, 6]. Also, this would require a 32-bit ADC. Hence, the need for a reconfigurable LNA as a key component of the multi-standard RF receiver front-end.

Reconfigurable RF design techniques have been developed for the implementation of adaptable receiver architectures. Though the conventional LC resonators provide optimum matching network or load impedance performance within a narrowband of interest, they yield poor multi-band responses. This LC resonator circuit limitation is obviated by implementing innovative design methods such as centre-frequency tuning, concurrent tuning and wideband design. Of the three multi-standard design methods, the most appealing for multimode multi-band broadband receivers is the centre-frequency tuning using a switchable passive network (SPN) [6].

The switchable passive network approach has been extensively researched and validated for reconfigurable RF design implementations [2, 6, 9, 10, 14]. Most of the published works have focused on the digital complementary metal oxide semiconductor (CMOS) process technology as the active device technology. The digital CMOS process node is forecasted to shrink by a factor of two every 18 months; this enables more complex digital logic and application functions to be integrated for a significantly reduced overall solution cost. The SPN has been utilised for the design of the matching network and LC tank for the mixer and voltage-controlled oscillator (VCO) of a CMOS-based 2–6 GHz reconfigurable LNA [6]. It combines switched capacitor and inductor arrays to design a switchable matching network and hence, optimise the flexibility of a reconfigurable RF receiver front-end design. Besides the switchable matching network method, other reported circuit techniques for CMOS LNAs designs include concurrent multi-band LNAs, wideband resistive-feedback topologies and common-gate amplifier (which uses a positive feedback loop to provide a simultaneous switchable input impedance matching and output load resonance via a switchable on-chip inductor). These all have their limitations and require system design trade-offs. For instance, the conventional SPN's switches in the input nodes lower the LNA noise performance. Also, the switchable on-chip inductor alone is limited by discontinuous tuning and large power consumption.

For the presented C- and K-band LNAs, an integrated SPN with metal oxide semiconductor (MOS)-varactor tuning technique [14] is recommended for the implementations of the GaAs-based and hybrid GaAs/CMOS-based single- and multi-process technologies. The MOS-varactor tuning is utilised in the three LNA stages of each band to achieve a programmable resonance frequency without degrading the noise figure of the LNA. This ensures that the performance merits of the combined switchable capacitor (in this case MOS-varactor) and inductor arrays are utilised. In the single-process technology case, a single input single output (SISO) antenna is utilised and a single RF/analog chain precedes the LNA. The multi-process technology case implements multiple parallel reconfigurable LNAs, multiple input multiple output (MIMO) antennas and a single RF/analog chain precedes the LNAs. The multi-process technology scenario should be implemented by combining high and low RF bands of broadband LNAs to take advantage of the reduced die area and low power consumption of optimised higher RF designs. For instance, this paper reports C- and K-bands broadband LNAs with different die sizes that scale inversely with the operating frequency band. The gains of both LNAs can be independently, successively and concurrently varied by a FPGA-based digital control signal to optimise the dynamic range margin of the multi-band receiver in real-time. Furthermore, the RT operation of the receiver front-end can be

enhanced by reconfiguring the LNA noise parameters via a FPGA-based digital channel selection.

VI. Multi-standard Reconfigurable Receiver Model

The generic approach in creating complete radio solutions is to implement a chipset comprising three major independent chips: RF/analog front-end electronics, analog baseband and digital baseband. Integrated and interfaced within these three blocks are the power management and audio codecs, power amplifier and front-end module (i.e., duplexers or transmit/receive switches). From the system design perspective, the key desirable operational requirements of multi-standard RF receivers include low cost; small form factor; minimum signal-to-noise ratio (SNR) (in worst-case channel conditions such as noise, interference and multipath); minimum bit-error-rate (BER) (in best-case channel conditions for energy-aware applications) and manageable power dissipation. These operational metrics represent a huge system-level performance demand.

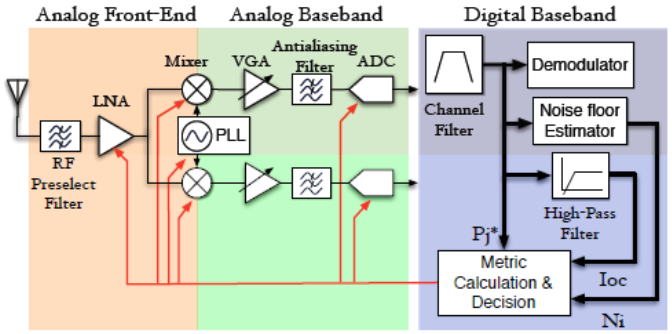


Fig. 8. Architecture of a Multi-standard Reconfigurable Receiver [2]

A multi-standard reconfigurable receiver architecture comprises reconfigurable blocks, reconfiguration metric calculator (e.g., a link quality estimator (LQE)) and reconfiguration strategy implementation algorithm [2]. With reference to Fig. 8, the reconfiguration blocks are the LNA, mixer, voltage-controlled oscillator and ADC. N_i (noise floor) and P_j* (in-channel signal power) are the RMs. Figure-of-merit (FoM) is a popular modelling approach utilised by researchers to assess a reconfigurable receiver's blocks for a given technology node. The following estimating relationships describe the FoMs for the three generic reconfigurable block models [6, 14]. The respective FoMs for the reconfigurable LNA and mixer model are stated in (7) and (8) thus:

$$FoM_{LNA}[GHz] = \frac{G[lin.]..IIP3[mW].f[GHz]}{P_{DC}[mW].(F[lin.]-1)} \quad (7)$$

where G = *power gain*; F = noise floor; *IIP3* = third order intercept point; f = operating frequency; and P_{DC} = power consumption.

$$FoM_{mixer}[dB] = 10\log\left(\frac{G[lin.]..IIP3[mW]]}{P_{DC}[mW].(F[lin.]-1)}\right) \quad (8)$$

The FoM for the reconfigurable VCO model is given by:

$$FoM_{VCO}[dBc/Hz] = 10\log\left(\left(\frac{f_c}{\Delta f}\right)^2 \cdot \frac{1}{P_{DC}[mW].L(\Delta f))}\right) \quad (9)$$

where f_c = frequency carrier in Hz; Δf = the offset frequency in Hz; $L(\Delta f)$ = noise relative to the carrier measured over 1 Hz bandwidth. The anti-aliasing filter [6] that limits the digital selection bandwidth is assumed to precede the ADC.

The FoM for the ADC is given by:

$$FoM_{ADC}[dB] = (6.02ENOB + 1.76) + 10\log\left(\frac{f_{sampling}}{P_{DC}}\right) \quad (10)$$

where ENOB = the relative number of bits; and $f_{sampling}$ = sampling frequency (Hz).

Given that the respective gain and noise figure values for each block match the source and load impedances, the overall receiver NF and IIP3 are obtained thus:

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + ... + \frac{NF_k - 1}{G_1 G_2 ... G_{k-1}} \quad (11)$$

$$\frac{1}{IIP3_{total}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + ... + \frac{G_1 G_2 ... G_{k-1}}{IIP3`_k} \quad (12)$$

where NF_k, $IIP3_k$ and G_k are the noise figure, third=order intercept point and power gain for the kth reconfigurable block respectively. The NF and IIP models define the global performance parameters of the multi-standard reconfigurable receiver with recourse to the high, moderate and low operational modes in real-time.

VII. Conclusion

The ubiquitous coverage of satellite systems and 2G to 5G radio access technologies require optimised cost-effective multi-standard multimode and multi-band transceivers. The development of a multi-standards radio is constrained by the requirements for low-cost, manageable power consumption and small footprint/form factor. In this paper, a common-source broadband LNA topology that enables the implementation of multi-standards reconfigurable receivers has been presented. The presented multimode multi-band broadband receiver front-end designs span 1.5 to 8 GHz and 18 to 21.6 GHz and the adopted RF architecture is direct conversion (zero-IF) and supports hybrid paths. In the L-, S-, C- and K-bands, various satellite applications and terrestrial wireless standards can be accommodated via a single-path RF/analog chain after the LNA. Moreover, both presented LNAs can be reconfigured using switchable passive networks to utilise the same RF/analog chain after the LNA. A hybrid path can be incorporated by providing a separate chain for each broadband MMIC LNA to enhance the dynamic range and the performance

of the integrated reconfigurable receiver front-end in real-time. In both implementations, the components footprints (and hence the size and weight), cost and power consumption are drastically reduced. The presented LNA designs can combine multi-band direct-conversion RF transceiver with CPU/field programmable gate array processing to provide a multi-standard radio solution at a fraction of the size, weight and power consumption of its competing topologies.

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REFERENCES

[1] Ekpo, S., and George, D., "4–8 GHz LNA Design for a Highly Adaptive Small Satellite Transponder using InGaAs pHEMT Technology," *Proc. 11th IEEE Wireless & Microwave Conference*. Melbourne, FL, April 2010, pp. 1–4

[2] Kim, J, Jang. Y. and Yoo, H., Design of reconfigurable RF front-end for multi-standard receiver using switchable passive networks, *Journal of Analog Integr Circ Sig Process*, Vol. 50, pp. 81–88, 2007.

[3] Ekpo, S., and George, D., "A System Engineering analysis of highly adaptive small Satellites," *IEEE Systems Journal*, Vol. 7, No. 4, Sept. 2013, pp. 642–648.

[4] Liscidini, A. and Brandolini, M., A 0.13 um CMOS Front-End, for DCS1800/UMTS/802.11b-g With Multiband Positive Feedback Low-Noise Amplifier, *IEEE Jour. of Solid-State Circuits,* Vol. 41, Issue 4, pp. 981 – 989. April 2006.

[5] Ekpo, S., Adebisi, B., George, D., Kharel, R., and Uko, M., "System-level Multicriteria Modelling of Payload Operational Times for Communications Satellites Missions in LEO," *Recent Progress in Space Technology*, Vol. 4, No. 1, June 2014, pp. 67–77.

[6] Didioui, A., Bernier, C., Morche, D. and Sentieys, O., Power Reconfigurable Receiver Model for Energy-Aware Applications, *IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), Columbus, OH, USA*, August 2013, pp. 800–803.

[7] Steer, M and Palmer, W. D., *Multifunctional Adaptive Microwave Circuits and Systems*. Raleigh: SciTech Publishing, Inc., 2009.

[8] Ekpo**,** S., George, D. and Adebisi, B., A Multicriteria Optimisation Design of SPSE for Adaptive LEO Satellites Missions Using the PSI Method, *AIAA Space Conference & Exposition,* San Diego CA, USA, September 2013, pp. 1–19.

[9] Fu, C., A 2.4 to 5.4 GHz Low Power CMOS Reconfigurable LNA for Multistandard Wireless Receiver, *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium,* 3-5 June 2007, pp. 65–68.

[10] Muhammad, K., Staszewski, R. B. and Leipold, D., Digital RF Processing: Toward Low-Cost Reconfigurable Radios, *IEEE Communications Magazine*, pp. 105-112, August 2005.

[11] Barnhart, D., Vladimirova, T., and Sweeting, M., "Satellite Miniaturization Techniques for Space Sensor Networks," *Journal of Spacecraft and Rockets,* Vol. 46*,* 2009, pp. 469–472.

[12] Sivone, P., Kangasmaa, S. and Parssinen, A., Analysis of Packaging Effects and Optimisation in Inductively Degenerated Common Emitter Low-Noise Amplifiers, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 51, No. 4, pp. 1120–1125, April 2003.

[13] Ekpo, S., and George, D., "A System-based Design Methodology and Architecture for Highly Adaptive Small Satellites," *Proc. 4th Annual IEEE Int. Systems Conference*, San Diego, CA, Apr. 5–8, 2010, pp. 516–519.

[14] Becerra-Alvarez, E. C, Sandoval-Ibarra, F and Rosa, J., A 90-nm CMOS Reconfigurable LNA for 4G Wireless Hand-Held Devices, *XIV Iberchip Workshop Puebla, Mexico*, 20-22 Feb. 2008.

[15] Ekpo, S. and George, D., A System Engineering Consideration for Future-Generations Small Satellites Design, *in Proc. First IEEE European Satellite Telecommunications Conference*, Rome, Italy, October 2012, pp. 1–4.

[16] Das, T., Practical Considerations for Low Noise Amplifier Design, *White Paper*, Freescale Semiconductor, pp. 2–9, May 2013.

[17] Agilent Technologies, Practical Noise-Figure Measurement and Analysis for Low-Noise Amplifier Designs, *Application Note 1354*, pp. 3–17, 2013.

[18] Agilent Technologies, De-embedding and Embedding S-Parameter Networks Using a Vector Network Analyzer, *Application Note 1364-1*, pp. 2–22, 2013.

[19] Jang, B., Yom, I. and Lee, S., Millimeter Wave MMIC Low Noise Amplifiers using a 0.15 μm commercial pHEMT Process, *ETRI Journal*, Vol. 24, No. 3, pp. 190–195, June 2002.

[20] Lu, K., Han, F., Horng, T., Cheng, H., Chiu, C. and Hung, C., Packaging Effects on a CMOS Low Noise Amplifier: Flip-chip versus Wirebond, IEEE Conference on Electronic and Technology, 2009, pp. 2064–2068.

[21] An, D., Rhee, E., Rhee, J. and Kim, S., Design and Fabrication of a Wideband MMIC Low-noise Amplifier using Q-matching, *Journal of the Korean Physical Society*, Vol. 37, No. 6, pp. 837–841, Dec 2000.

[22] Perez, O., Segovia-Vargas, D., Munoz, L., Jimenez-Martin, J. and Gonzalez-Posadas, V., Broadband differential low-noise amplifier for active differential arrays, *Microwave Theory and Techniques, IEEE Transactions on*, Vol. 59, No. 1, pp. 108–115, Jan. 2011.

[23] Aneja, A. and Kumar, M., Design of Pseudomorphic High Electron Mobility Transistor-based Ultra Wideband Amplifier using stepped Impedance stub Matching, *American Journal of Engineering Research*, Vol. 3, No. 3, pp. 138–143, 2014.

[24] Im, D., Nam, I. and Lee, K., A low power broadband differential low noise amplifier employing noise and IM3 distortion cancellation for mobile broadcast receivers, *IEEE Microwave and Wireless Components Letters,* Vol. 20, No. 10, pp. 566–568, Oct. 2010.